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AstroPix: A Pixelated HVCMOS Sensor for Space-Based Gamma-Ray Measurement

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ABSTRACT: A next-generation medium-energy gamma-ray telescope targeting the MeV range would address open questions in astrophysics regarding how extreme conditions accelerate cosmic-ray particles, produce relativistic jet outflows, and more. One concept, AMEGO-X, relies upon the mission-enabling CMOS Monolithic Active Pixel Sensor silicon chip AstroPix. AstroPix is designed for space-based use, featuring low noise, low power consumption, and high scalability. Desired performance of the device include an energy resolution of 5 keV (or 10% FWHM) at 122 keV and a dynamic range per-pixel of $25 - 700$ keV, enabled by the addition of a high-voltage bias to each pixel which supports a depletion depth of 500 μm. This work reports on the status of the AstroPix development process with emphasis on the current version under test, version three (v3), and highlights of version two (v2). Version 3 achieves energy resolution of $10.4 \pm 3.2\%$ at 59.5 keV and 94 ± 6 μm depletion in a low-resistivity test silicon substrate.

KEYWORDS: silicon, CMOS, gamma-ray detector, astrophysics instrumentation, MeV gamma ray

Contents

1 Introduction **1**

2 AstroPix_v3 **2**

3 Experimental Setup **7**

4 Noise Studies **9**

5 Energy Resolution **10**
5.1 Energy Calibration and Resolution 10
5.2 Impact of Depletion 12

6 Heavy-Ion Radiation Testing **14**
6.1 Experimental Setup 14
6.2 Radiation Results 15

7 Conclusion and Outlook **17**

1 Introduction

Over the past several decades, silicon strip detectors (SSDs) have been a key detector technology used in gamma-ray and cosmic-ray telescopes such as the *Fermi* Large Area Telescope (LAT) [1], the Alpha Magnetic Spectrometer (AMS) [2], and DArk Matter Particle Explorer (DAMPE) [3]. Breakthroughs in particle physics instrumentation have enabled the development of High Voltage-CMOS (HVCMOS) monolithic active pixel sensors (MAPS) [4], which have significant advantages over other silicon-based detectors (such as SSDs). MAPS have signal amplification and readout circuitsembedded in the sensor, enabling reductions in pixel power consumption without the need for a separate readout Application Specific Integrated Circuit (ASIC). The design reduces the overall mass of the detector system and limits the passive material in the active detector volume while also improving spatial resolution.

In particular for soft gamma-rays ($<$ 10 MeV), it is imperative to have two-dimensional hit location information in a single detector layer [5]. These detector capabilities make them a particularly compelling technology for future gamma-ray telescopes (see Refs. 5, 6 for more details).

AstroPix is a HVCMOS MAPS being developed for space-based mission concepts such as the All-sky Medium Energy Gamma-ray Observatory eXporer (AMEGO-X) [5]. Inspiration is drawn from the ATLASPix chip, which was designed to detect charged particles in the inner detector of the ATLAS Experiment [7]. The AstroPix project has subsequently coordinated incremental development away from the ATLASPix designs toward a final version which will be optimized for a space environment (see

Table 1). The current device under test and subject of this work is the third iteration, or AstroPix_v3. The performance of AstroPix_v1 and AstroPix_v2 has been documented in Refs. 8–11.

In addition to reviewing AstroPix_v3 operation and functionality, this work will overview noise and energy resolution performance. Current-voltage and capacitance-voltage curves are presented with discussion of sensor noise and depletion. AstroPix_v3 will be the first flight-tested AstroPix chip as the main component of a sounding rocket paylod, the Astropix Sounding rocket Technology dEmonstration Payload (A-STEP) (see Sec. 7). As such, operation and charicterization results relevant for this upcoming flight will be emphasized.

AstroPix has been tested in multiple beam environments, including with a 120 GeV proton beam at the Fermilab Test Beam Facility. A detailed report of this testing and results including the measurement and identification of minimum ionizing particles, alternate energy calibration method, and alternate measurement of depletion depth will be reported in an upcoming independent publication.

The paper is outlined as follows: Section 2 describes the AstroPix_v3 chips; Section 3 illustrates the benchtop test setup; Section 4 describes the amplitude and impact of noise and dark count rate; Section 5 details the AstroPix_v3 characterization, including calibration, energy resolution, and depletion depth; Section 6 summarizes radiation testing of AstroPix_v2 in a heavy ion beam; and finally Section 7 summarizes the work and outlines future outlook and applications of AstroPix.

2 AstroPix_v3

HVCMOS MAPS detectors were developed by Ivan Peric more than a decade ago [4] primarily for particle physics applications. The Karlsruhe Institute of Technology (KIT) ASIC and Detector Laboratory (ADL) has continued this work, advancing the technology forward [12–14]. ADL's experience with chips such as MuPix and ATLASpix inform the development of AstroPix. The design evolution over the course of several iterations has culminated in the first full-scale flight prototype chip: AstroPix_v3. An illustration of key properties of each AstroPix version, including AstroPix_v3, is shown in Table 1. For the first time, AstroPix_v3 uses the full 2×2 cm^2 reticle and features a 35×35 pixel matrix with a pixel pitch of 500×500 μm^2. A 300×300 μm^2 high voltage deep n-well (DNW) protects the embedded CMOS circuits and creates a bias junction with the p-type bulk silicon, leading to a depletion region with HV application (see Fig. 1). AstroPix_v3 uses a standard high voltage CMOS process with a deep n-well and unthinned bulk silicon wafers with a thickness of 720 μm.

The signal path is shown in Fig. 2. Each pixel contains a charge-sensitive amplifier (CSA) and comparator. For testing and comparison purposes, the first three columns feature a PMOS amplifier whereas the rest implement the standard NMOS amplifiers. These PMOS columns were found to impair data quality with higher noise rates than NMOS columns, and are not considered in this work's analysis or for future design iterations. A simplified schematic for pixel operation and timestamp generation is shown in Fig. 3.

The in-pixel comparator enables self-triggering. A Time Over Threshold (ToT) measurement gives proxy for the deposited charge by recording the duration of the signal amplitude while over a

Table 1. Parameters of ATLASPix and AstroPix.
*Analog data only ◊Median of full array response ■Theoretical value from *pn* junction model △Do not expect full depletion with test chips. See Sec. 5.2

	ATLASPix (Measured) [6, 15]	AstroPix_v1 [8]	AstroPix_v2 [8, 10]	AstroPix_v3 [11, 16, 17]	AstroPix (Goal)[5]
E_{res} (FWHM)	7.3 ± 1.2% at 30.1 keV	20 ± 7.4%* at 30.1 keV	15 ± 3% at 30.1 keV	10.4 ± 3.2%◊ at 59.5 keV	10% at 122 keV
Pixel pitch [μm]	150 × 50	175 × 175	250 × 250	500 × 500	500 × 500
Thickness [μm]	100	725	725	725	525
Depletion [μm]	48■	Not measured	Not measured	94 ± 6△	500
Dynamic range [keV]	5-32	14-122	14-80	14-200	25-700
Analog power [mW/cm^2]	120	14.7	3.4	1.06	1.0
Digital power [mW/cm^2]	40	9.9	3.75	3.06	0.5

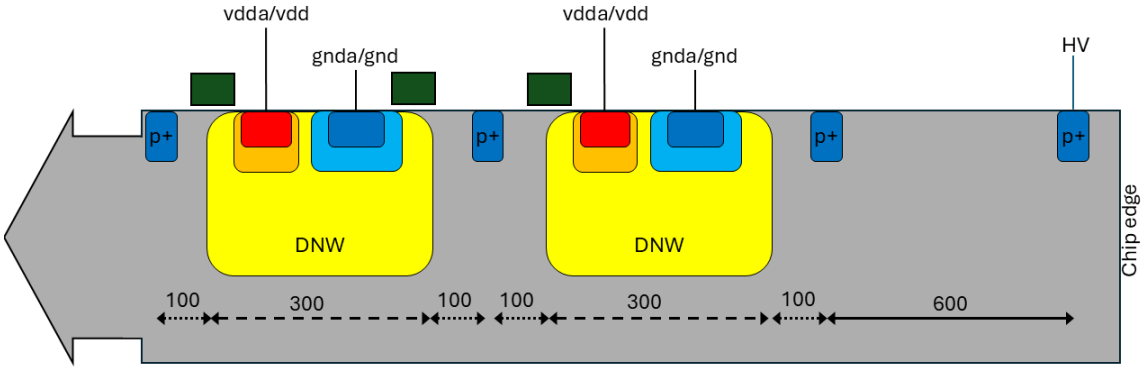

Figure 1. Cartoon of AstroPix_v3 structure, including DNWs (yellow), CMOS components (structures within DNWs), inter-pixel isolation *p*-stop (blue), and DNW guard rings (dark green). HV is delivered on the frontside to the chip edge. Drawing not to scale. Units displayed in μm.

user-defined threshold. In AstroPix_v3, a global comparator threshold value is set for the full array [1].

[1]AstroPix_v4 and subsequent versions include Tune DACs to enable individual pixel threshold setting [18].

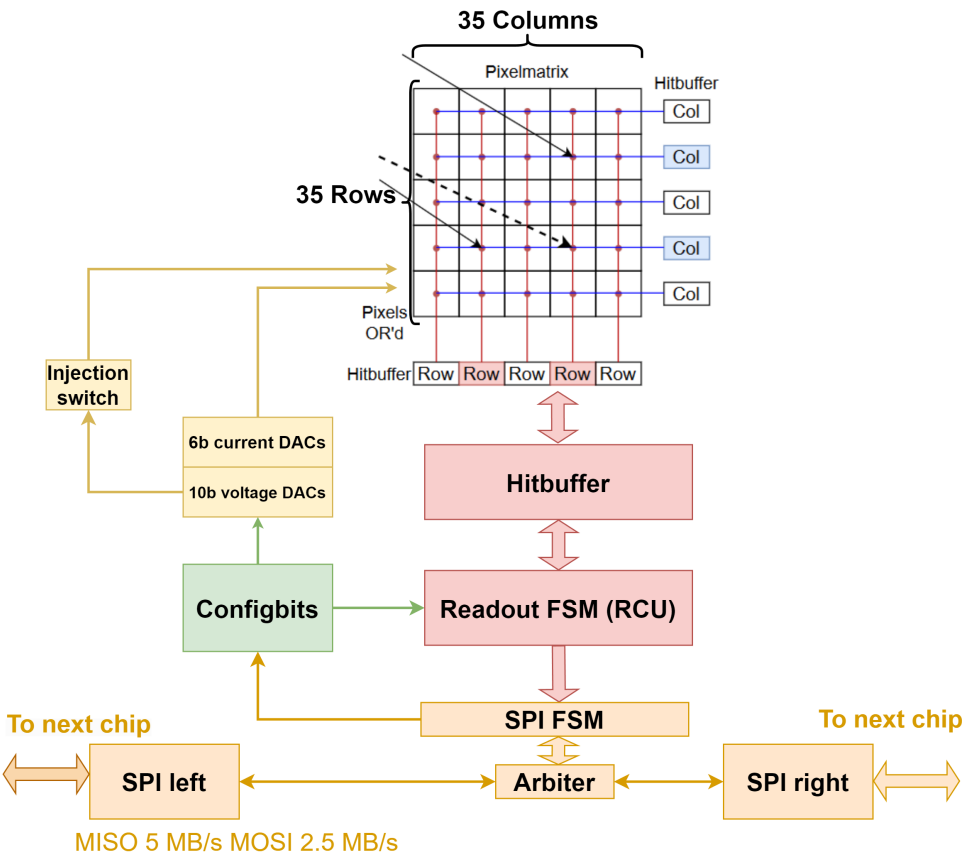

Figure 2. AstroPix_v3 signal chain with all basic blocks showing the full readout path. Hitbuffer signals interface with a readout control unit (RCU) which includes a finite state machine (FSM).

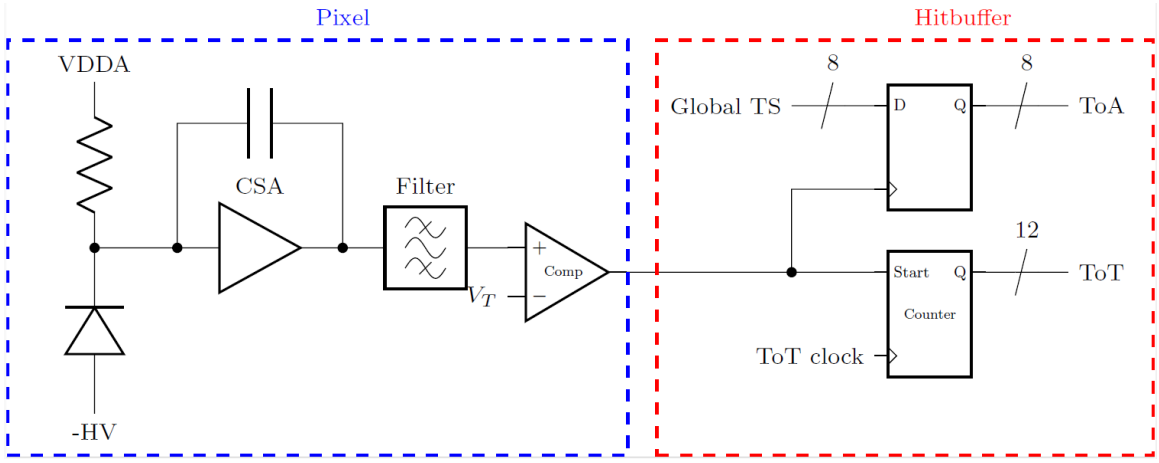

Figure 3. Simplified AstroPix_v3 operational schematic illustrating electronics within each pixel and timestamp generation within pixel buffers.

When a pixel comparator passes a signal that exceeds the threshold, the chip processes this information and lowers an 'interrupt' signal. To keep the number of readout channels low, and therefore reduce power consumption, the pixel comparator outputs per row and column are OR wired (Fig. 2). A low 'interrupt' signal indicates that data is ready for collection[2] The comparator threshold is set to achieve maximal detector efficiency by setting the lowest possible detector threshold while still minimizing triggering from noise fluctuations.

The matrix digitisation is done via 12 bit counters driven by a 200 MHz clock, implemented both per row and column to measure ToT (Fig. 2). Resulting ToT values fall within the μs range, therefore the ns-scale resolution from this clock is much smaller than the ToT noise. An 8 bit time of arrival (ToA) timestamp is driven by a 2 MHz clock (Fig. 2).

Once collected at the pixel level, the digital signal is stored in a hit buffer and ultimately read out over SPI (Fig. 3). Each digitized signal returns a 5-byte data packet - a 4 bit header for data integrity, 11 bit pixel address, 12 bit ToT, and 8 bit ToA.

In addition to digitized output, an "analog" output can also be accessed. This is sent from the in-pixel amplifier prior to the standard digitization readout path (including the in-pixel comparator) and can be read from a single pixel at a time from the bottom row of pixels (row0). The analog output signal provides an important cross-check on the energy resolution of the detector and front-end amplifier because it is not limited by the digital resolution of the readout.

Power consumption has decreased with each chip version (see Table 1). Strategies such as limiting clock distribution to the matrix periphery, optimizing the bias circuits, and increasing pixel size account for some power saving. Analog power consumption has been the emphasis of past design iterations, where 97% analog power reduction was achieved from AstroPix_v1 to the current 1.06 mW/cm^2 draw of AstroPix_v3. Future versions of AstroPix [18] will continue this trend of reduced power consumption with a renewed focus on the digital power draw. A brief discussion of the planned path forward is included in Sec. 7.

Figure 4 (left) shows a single AstroPix_v3 mounted to a carrier board. Chips are diced from the wafer as single arrays and in a 2×2-array configuration called a quad chip, shown in Fig. 4 (right) with a total area of 3.81×3.93 cm^2. This quad chip, utilizing four independent AstroPix arrays, will be the building block of larger AstroPix-based structures including A-STEP. 18% of fabricated AstroPix_v3 chips (180 chips) underwent Quality Control testing following fabrication, dicing from the wafer, mounting to a carrier board, and wirebonding. 97.1% of $200-400$ $\Omega*$cm resistivity (Okmetic) chips passed the Quality Control testing, with the few failures due mostly to low breakdown voltage. This exemplifies the scalability that AstroPix is designed for, where the formation of large format structures with straightforward integration, operation, and readout is achievable. Power is delivered to each chip in a quad-chip via custom-designed bus bars to supply the chips in parallel. Data are sent between arrays via wirebonds that enable a daisy chain and is delivered off-chip with a quasi-Serial Peripheral Interface (SPI). Quad chips of AstroPix_v3 are also under test with a suite of software and firmware developed for the readout of large arrays and multiple layers [3].

[2] AstroPix_v3 readout utilizes a Field Programmable Gate Array (FPGA) which receives and stores data by the software-based data acquisition (DAQ) system (see Sec. 3)

[3] https://github.com/AstroPix/astep-fw

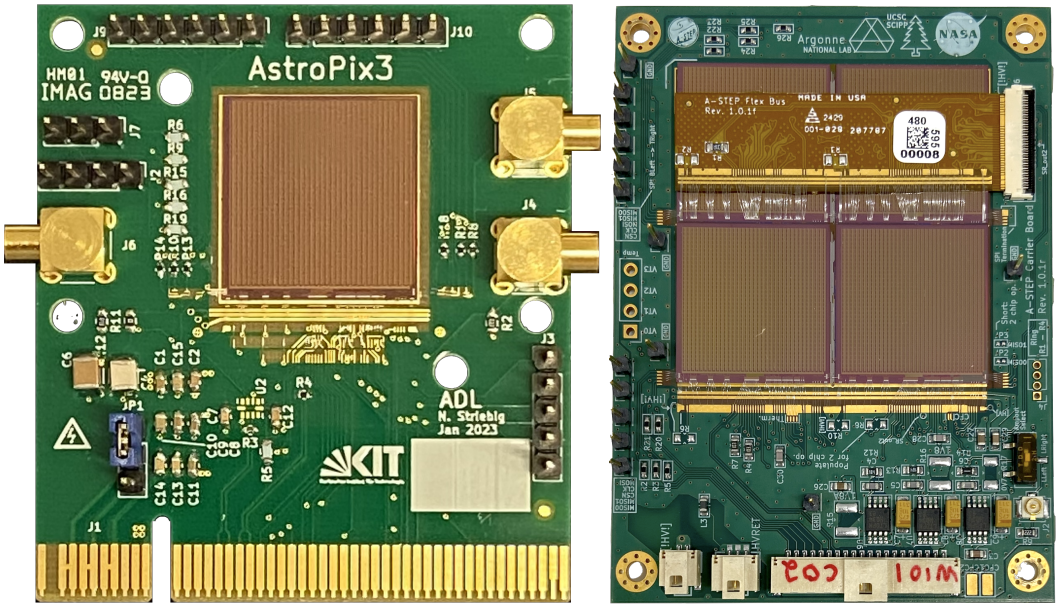

Figure 4. (left) One 2×2 cm^2 AstroPix_v3 chip mounted on a custom carrier board (right) One $\sim 4 \times 4$ cm^2 AstroPix_v3 quad chip, comprised of an array of four individual chips.

The 20 MHz SPI interface clock transmits bytes in 200 ns over two MISO lines, leading to a single chip latency of 400 ns. Larger instrument designs can daisy chain up to 32 AstroPix chips to one SPI bus, limited by available chip identification bits, which increases the per-bus latency up to 8 μs. The 2 MHz timestamp clock turns over after 128 μs, so the latency does not impact timing resolution.

All iterations of AstroPix were fabricated using TSI Semiconductors' 180 nm process and AstroPix_v3 was delivered in October 2022 [4]. The final design must deplete 500 μm and thus a global high-voltage (HV) bias is applied to a substrate contact along the chip edge on the frontside (Fig. 1). A backside bias is not utilized in order to simplify chip processing and eventual integration into large format structures. Full depletion will be achieved with a high-resistivity ($> 5000\ \Omega$*cm) silicon wafer thinned to 525 μm. Neighboring pixels are isolated by a p-stop isolation ring (blue in Fig. 1), separated by a distance of 100 μm. This large separation between the DNW guard ring (dark green in Fig. 1) and the isolation p-stop allows for operation at high voltages with breakdown occurring at -400 V. The bulk substrate between implants sustains the high voltage, creating a smooth depletion layer through the bulk without introducing inter-pixel dead space.

AstroPix_v3 was fabricated on 25 ± 8, $200 - 400$, and $25,000 \pm 8,000\ \Omega$*cm wafers provided by the TSI Foundry, Okmetic, and Topsil respectively. The highest-resistivity AstroPix_v3 chip was targeted for exploring the goal depletion depth, but the medium-resistivity chip (henseforth referred to by its manufacturer, Okmetic) will be the focus of this paper (see Sec. 5.2 for more details). The depletion value stated in Table 1 reflects this Okmetic wafer where full depletion is not expected. Further details of AstroPix characterization can be found in Refs. 11, 16, 17.

[4]TSI Semiconductors has subsequently been acquired by Bosch Semiconductor LLC and the foundry business has ceased. Subsequent iterations of AstroPix will be fabricated at a different foundry such as AMS in Austria or LFoundry in Italy.

A current-voltage (IV) curve of the biasing HV used to deplete the substrate for a representative Okmetic chip is shown in Fig. 5. Breakdown occurs between −380 V and −400 V depending on the wafer[5]. Applications of AstroPix require low power draw and a bias leakage current less than 1 μA, allowing operation of an Okmetic AstroPix_v3 chip up to −400 V. A larger bias enables more complete depletion (more details in Sec. 5.2), so the energy calibration reported in Sec. 5.1 uses a bias of -350 V which incorporates a safety margin with respect to the breakdown voltage. Otherwise, a stable bias of −150 V can be assumed for the remainder of the studies in this paper unless explicitly stated.

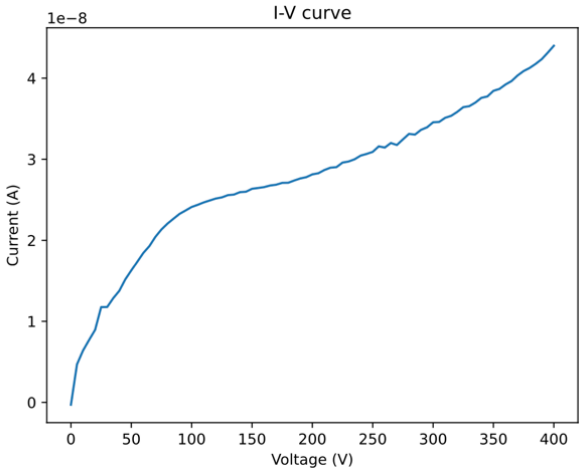

Figure 5. IV curve for AstroPix_v3 Okmetic chip (200 − 400 Ω∗cm).

3 Experimental Setup

The equipment used to test AstroPix, as shown in Fig. 6, includes a custom built GEneric Configuration and COntrol (GECCO [19]) Data Acquisition System, a NexysVideo (Xilinx Artix-7) FPGA, and a carrier board for the integration of the chips into the GECCO system (along with an oscilloscope and power supplies). Data is read off the sensor by a software-based DAQ system.

In-pixel circuitry operation can be fine-tuned through user-definable values configured through Digital-to-Analog Converters (DACs). Currents such as that fed to the source follower which sets the amplifier operating point, and voltages such as comparator voltage baseline impact signal shaping and power consumption. Initial values are set from simulation and were further optimized for performance while on the bench. Shaping the pulse width via the in-pixel band pass filter was a focus, to not limit the dynamic range given by the maximum measureable value of ∼ 20.5 μs by the 12 bit 200 MHz ToT counter. Following optimization, all testing utilizes the same set of DAC values. This can be assumed for all the results explored in this work.

[5]Breakdown occurs around −200 V with the 25 ± 8 Ω∗cm wafer.

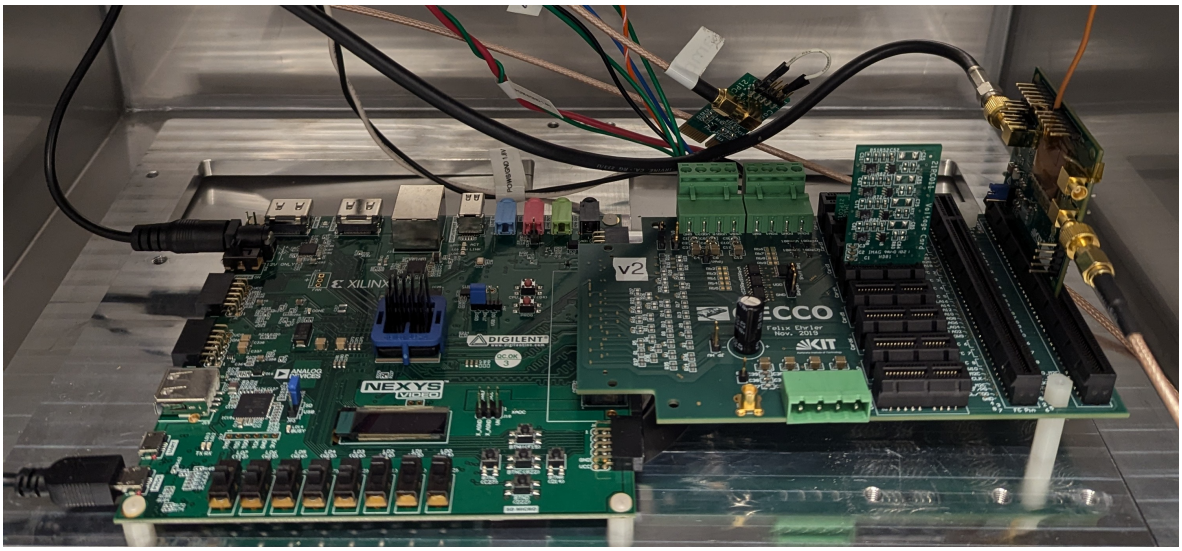

Figure 6. Experimental setup of AstroPix_v3 and supporting electronics. The AstroPix_v3 chip is mounted on the rightmost board, facing the left.

Table 2. Standard run settings for the AstroPix_v3 studies reported in this work.

Wafer name	Resistivity [Ω∗cm]	Comparator Thresh. [mV]	Bias [-V]	Max. dark count rate [Hz]
Okmetic	200-400	200	150	2

The chip can operate in “high gain" or “high dynamic range" mode, which impacts the in-pixel CSA gain. The studies in this work all operate in “high dynamic range" mode which causes bilinear output from the CSA. Therefore, a linear response through the full dynamic range is not expected.

Custom firmware [6] and software [7] allow for interfacing with the chip, properly setting clocks and configuring chip operational settings, and executing data collection and storage.

All studies in this work exclusively consider this digital data. The OR wiring results in separate hits containing row and column information. Events are considered for data analysis only if a pair of row and column hits record a timestamp within 1 clock count (5 ns) and ToT values within 0.15 μs. In this way, the response of individual pixels can be considered.

The work presented in this paper is a collection of results from a dedicated international collaboration with worldwide testing campaigns. As such, minor differences in experimental setup may be present for different tests presented here. Unless explicitly stated in a section, the settings in Table 2 can be assumed for all studies in this work.

Additional settings include operation in ‘high dynamic range‘ gain mode, optimized voltage and current DAC settings, and disabling of the first three pixel columns with PMOS amplifiers.

[6] https://github.com/AstroPix/astropix-fw
[7] https://github.com/AstroPix/astropix-python

4 Noise Studies

'Noise' hits occur when particles from background sources interact with the detector, such as cosmic ray interactions or naturally occurring background radiation. Fluctuations in the electronics can also trigger a comparator readout, even without a particle interaction. This is a 'dark count' and is measured as a rate, the dark count rate (DCR). The goal of these studies are to determine the percentage of pixels which are sensitive within the dynamic range, understand the dark count rate at different thresholds, and set an optimized threshold voltage such that DCR is minimized.

The analog baseline, as read off the amplifier from selected pixels, shows random fluctuations up to 50 mV over a nearly constant baseline. This constant noise floor is due to detector electronics and consists of shot noise from the sensor diode, and thermal and flicker noise from the electronics. The latter two sources are thought to be sub-dominant, as they carry a dependence on capacitance and the AstroPix_v3 pixel capacitance is roughly 1 pF. Large fluctuations with a low rate are likely noise from the environment in which the sensor is operated. The dark count rate can be mitigated during data collection by setting the comparator threshold higher than 50 mV above baseline. A 22.1 keV photopeak from cadmium-109 is visible in measurements made in Sec. 5 with a 200 mV threshold, so the 50 mV fluctuations can be disregarded and do not impact the dynamic range. The impact of increasing threshold on DCR is shown in Fig. 7.

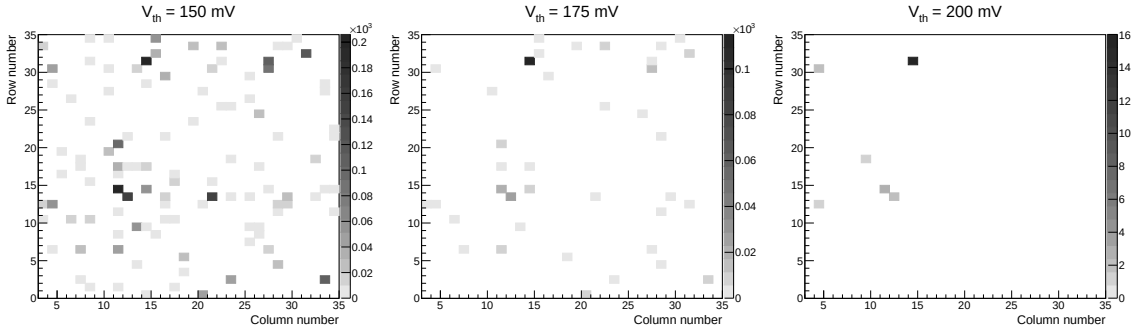

Figure 7. Dark count hit map for an Okmetic chip at different comparator thresholds with no disabled pixels. The z-axis shows the number of hits per pixel over 5 s integration time.

Threshold values of 200 mV still allow the detection of 25 keV signals as required in Table 1 (see Section 5 for details). With nominal operational settings, $< 0.5\%$ of pixels per array are too noisy for data collection and must be masked (their comparators disabled).

The variation in dark count rate also illustrates a degree of variation between pixels within the same array. Process variations and device mismatch lead to this natural variation in amplifier gain, leading to pixels responses varying $20 - 35\%$. Individual-pixel calibration therefore is required to correct for this variation. Section 5 outlines this calibration strategy and its results.

The in-pixel comparator does not collect sub-threshold hits. Studies in Ref. 6 show that charge sharing between pixels does not induce above-threshold hits in neighboring pixels. However, the threshold is set to maximize the dynamic range and has been shown (in Sec. 5) to enable measurement below the 25 keV requirement. In this way, some degree of charge splitting can be accounted

for provided that there is enough to trigger a neighboring comparator operating at this low global threshold. Simulation studies are planned to investigate the potential impact of charge sharing and its effect on energy resolution.

The studies of this section illustrate that DCR can be reduced to tolerable rates with AstroPix devices. This can be done by carefully setting a global threshold which minimizes DCR while still providing measurements within the required dynamic range of 25 – 700 keV and identifying and masking noisy pixels with large DCRs. These noisy pixels have no geometric dependence within the array and have not shown induced charge sharing. With the optimal operation described here and standard run settings from Table 2, a single AstroPix_v3 array measures a total DCR below 2 Hz. This measured rate is acceptable for future AstroPix applications including A-STEP and large-format future-observatories such as AMEGO-X. Additionally, future AstroPix versions are expected to decrease DCR with the ability to set thresholds at an individual pixel level [18].

5 Energy Resolution

A high bias voltage enables more complete depletion and in general more efficient charge collection. Here we consider an energy calibration conducted at −350 V bias, as described in Ref. 16. The current draw off the bias line is ∼ −50 nA[8].

5.1 Energy Calibration and Resolution

The energy calibration procedure is described in detail in Ref. 16, and is applied to one Okmetic chip. After masking 8 noisy pixels, measurements of radioactive sources including Cd-109, Ba-133, Am-241, and Co-57 were made. Photopeaks could be identified from individual pixel spectra between 22.2 – 122 keV. A feature indicative of a Compton edge at around 220 keV was present in the data. Calibration curves for each pixel relate the expected photopeak energy and the mean measured ToT with a function of the form

$$y = a * E + b * [1 - \exp(-E/c)] + d \ ,$$

where E is the true photopeak energy and y is the uncalibrated ToT value. The functional form involves a low-energy linear component and higher-energy exponential decay. This form is motivated by the in-pixel charge-sensitive amplifier which operates in two different gain regimes, creating a bilinear gain structure. The amplifier saturation effect is also reflected. One example calibrated pixel is shown in Fig. 8 and compared to an example pixel from AstroPix_v2. The difference in slope is due in part to differences in front-end amplifier tuning. Figure 9 shows a calibrated Am-241 spectrum for all 996 calibrated pixels after individual pixel calibration. The 59.5 keV photopeak is clearly visible. Further work is underway to determine its source, though it is expected to be artificial.

When considering one 35×35 array, 92.4% of pixels achieve the low-energy floor requirement of 25 keV sensitivity. 44% of pixels meet the energy resolution requirement of 5.9 keV at 59.5 keV

[8]The IV curve from this study is shown in Fig. 5.

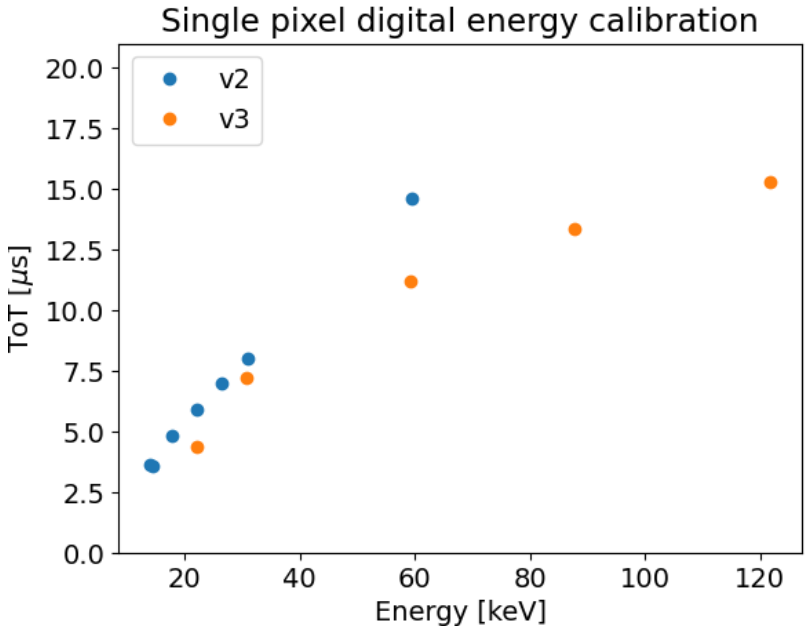

Figure 8. Calibration curves of Okmetic AstroPix_v2 and AstroPix_v3 with one example pixel off each chip. Data sets and further discussion is considered in [16].

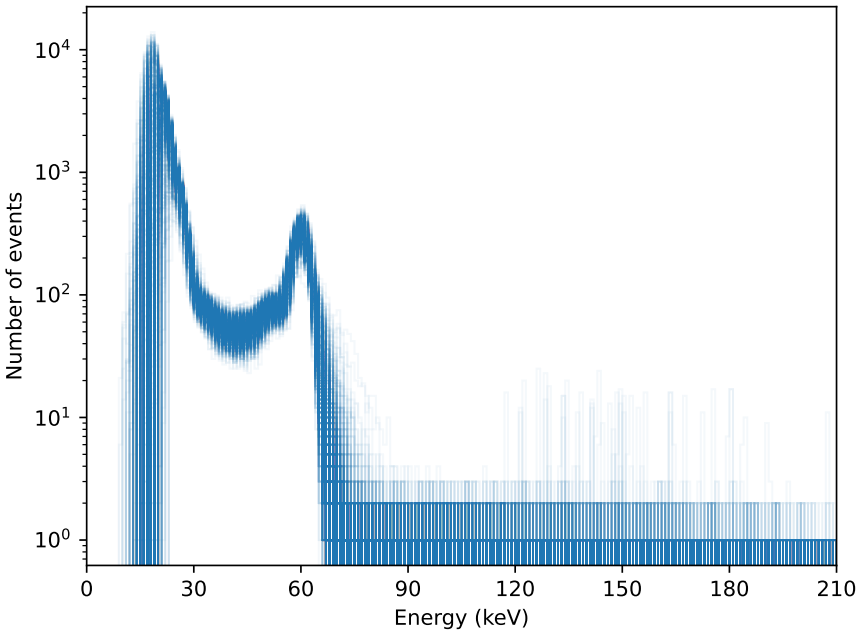

Figure 9. Calibrated Am-241 spectra from all 996 calibrated pixels, overlaid.

with a median full-width half-max (FWHM) of 6.2 keV (10.4%). The lack of a confident feature identification at ~ 220 keV makes the measured dynamic range 14 – 200 keV.

The high-end of the dynamic range is hindered in AstroPix_v3 due to incomplete depletion (see Section 5.2) and amplifier saturation. Simulations of the amplifier in “high dynamic range" mode showed that its output amplitude saturates at ~ 250 keV. This is consistent with observations which saw maximum energies (that could not be fully calibrated) of ~ 220 keV. A subsequent iteration of AstroPix implements test pixels with a dynamic feedback capacitance realized with an NFET device [20], which displays no saturation at energies over 700 keV while maintaining performance through the full dynamic range. Additionally, more ToT bits are allotted to prevent a dynamic range loss due to overflow in the digitization step in future versions.

5.2 Impact of Depletion

The highest-resistivity AstroPix_v3 design (25000 ± 8000 Ω∗cm) was targeted for exploring the goal depletion depth of 500 μm within a −100 V bias range. The two other resistivities are included for comparison with previous generations and consideration for further studies. The different depletion depths expected for each wafer resistivity is shown in Fig. 10.

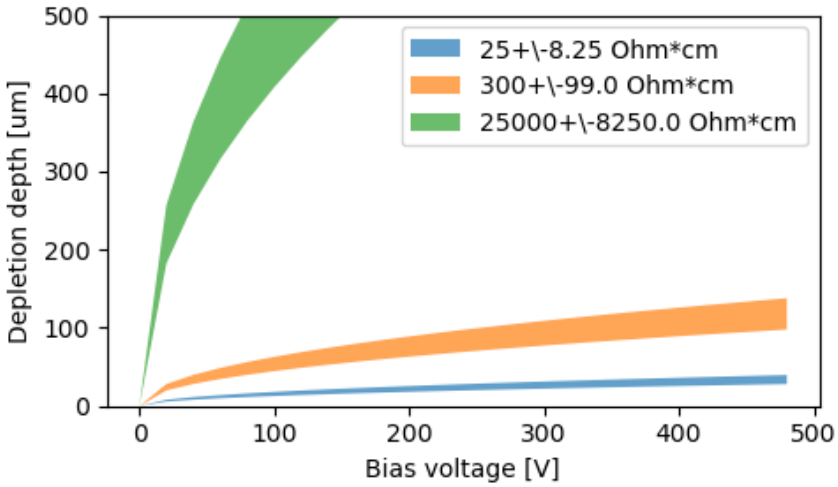

Figure 10. Theoretical achievable depletion of AstroPix_v3 substrates [21].

However, this high-resistivity substrate could not be thoroughly tested due to a high leakage current. An inherent voltage gradient coupling through conductive mounting to the test board contributes to a low breakdown voltage of < -1 V, but isolating the backside does not resolve the high current. The cause of this current is an active area of investigation.

Detector capacitance plays an important role in the readout system performance. By design, it is connected to the input of the charge-sensitive amplifier. The amplifier noise is a monotonically increasing function of the capacitance. Therefore, reducing the capacitance through higher bias reduces noise, in addition to increasing the ionization efficiency by augmenting the depletion region.

A capacitance-voltage (CV) curve of the 200 – 400 Ω∗cm Okmetic substrate is shown in Fig. 11. Notably, the function shape at low voltages is different from the linear dependence of $1/C^2$ on bias voltage. We attribute this to the depletion area development. At near-zero bias the depleted regions starts to grow from the implants, therefore the depleted area is smaller than the full chip size. For this reason, initially $1/C^2$ grows sub-linearly with the bias voltage until the depleted region between neighboring pixels reconnect. The other feature is a sharp capacitance change around −150 V. It is dependent on the test frequency, indicating a possible relation to surface charge. Both features are under further investigation, however the functional shape of the CV curve suggests under-depletion and isolated depleted regions under each implant in the voltage range tested.

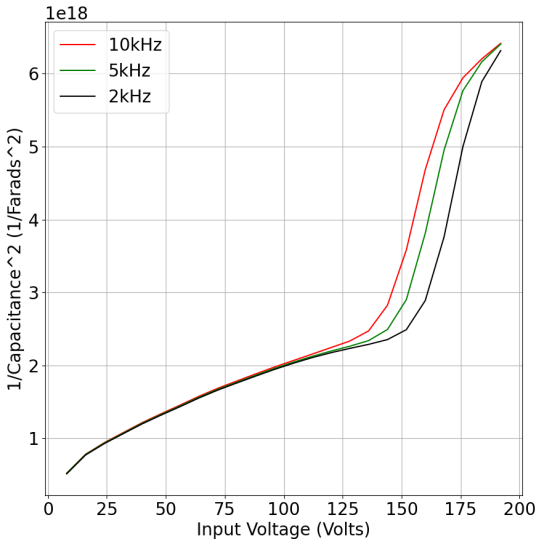

Figure 11. CV curve for Okmetic chip tested at different frequencies. [17]

Estimations of the depletion depth that the Okmetic AstroPix_v3 can achieve was tested in Ref. 16 by measuring the count rates of X-ray sources. The method exploits a rather small path length of the daughter photo-electron in silicon, of less than 20 μm, leading to proportionality of the rate and the depleted volume. An average depleted depth is extracted using the pixel area. The drawback of this method is the need to rescale the rate to account for low-energy part of the photon spectrum. This indirect measurement results in 60 ± 3 μm depletion at −150 V bias and 94 ± 6 μm depletion at −350 V bias, which agrees with the PN junction model curve with the uncertainty in the resistivity. Fitting a PN junction model to the data reproduces a resistivity of 236.8 ± 2.4 Ω∗cm.

A direct measurement of depletion depth from the same wafer using the Edge Transition Current Technique [22] was conducted at the Santa Cruz Institute for Particle Physics in November 2023. Current results from this study are detailed in Ref. 21 and Ref. 17. The results are consistent with Ref. 16 over the voltage range tested, however further analysis is ongoing.

Table 3. Ion beam properties from June 2022 radiation testing

Ion	Initial Energy [MeV]	Air gap [mm]	Sensor tilt angle [deg]	Surface energy [MeV±1 STD]	Effective LET [MeV∗cm^2/mg]	Effective range [μm]
$^{40}Ar^{+14}$	642	20	0	555 ± 1.0	8.0	206
$^{63}Cu^{+22}$	1007	20	0	805 ± 1.1	19	141
		45	23	737 ± 1.9	21	115
$^{78}Kr^{+28}$	1317	20	0	1021 ± 2.9	28	132
		45	23	921 ± 3.0	32	107
$^{124}Xe^{+43}$	1975	20	0	1341 ± 4.6	57	98
		35	23	1216 ± 4.9	64	102

6 Heavy-Ion Radiation Testing

A previous iteration of AstroPix, AstroPix_v2, was tested for radiation hardness and single-event effects (SEEs). The digital periphery design was not changed between the two versions. Like AstroPix_v3, the AstroPix_v2 chips tested were fabricated on an Okmetic (200 – 400 Ω*cm) substrate. The presence of the on-chip digital periphery motivates this testing, as that area may be the most susceptible. Two classes of SEE were monitored:

1. **Single-event latchup (SEL)**, a catastrophic event leading to runaway power draws due to parasitic switching of the CMOS component transistors [23], and
2. **Single-event functional interrupt (SEFI)**, a temporary state where radiation causes bit flips which may degrade data or configuration but a system reset can restore nominal operation.

6.1 Experimental Setup

The radiation tolerance of AstroPix_v2 was tested in June 2022 at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility 88" cyclotron [24]. The beam provides a cocktail of ions with 16 MeV/amu tune shown in Table 3. A range of ions with differing atomic masses provides a range of testable linear energy transfer (LET), and tilting the detector plane relative to the ion beam direction of propagation provides an effective LET (the surface-incident LET in silicon at normal incidence divided by the cosine of the detector tilt angle). Effective range is the ion penetration depth in silicon calculated perpendicular to the surface of the sensor (penetration range multiplied by the cosine of the detector tilt angle).

Spaceflight standards [25] require instruments to survive catastrophic latchup up to a LET of 60 – 75 MeV∗cm^2/mg and fluence of 1×10^7 cm^{-2}. Dosimetry is provided from BASE through calibration of a set of four photomultiplier tubes (PMTs) to a center PMT that is then removed during irradiation.

Figure 12 shows AstroPix_v2 on the left, 20 mm away from the beam pipe. The chip carrier board and auxiliary boards are covered with aluminum to protect active electronic components from recoil

ions. Digital data was collected from the full array (with 35% of pixels masked to reduce noise), as well as analog data from the bottom left corner pixel. Four input voltage rails and the high voltage bias were also monitored during irradiation for SEL. Non-destructive SEFI events could present as features in either power draw or returned data.

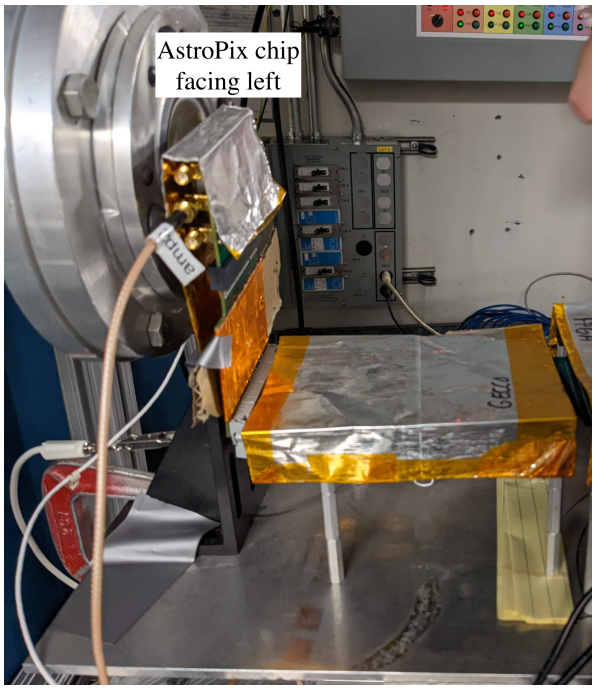

Figure 12. AstroPix_v2 at the 88" Cyclotron (beam pipe on the left). AstroPix boards are covered to protect from stray ions.

High- and low-flux data sets were collected, where the average high flux $\leq 2.05 \times 10^4/\text{cm}^2/\text{s}$ and average low flux $\leq 123.1/\text{cm}^2/\text{s}$. The total fluence of high flux runs was $1 \times 10^7/\text{cm}^2$ unless an destructive event occurred (see Sec. 6.2).

6.2 Radiation Results

No immediately destructive high-current events occurred, suggesting AstroPix_v2 has a destructive SEL threshold greater than 64 MeV$*$cm^2/mg. The device is susceptible to recoverable soft errors with a LET threshold above 19 MeV$*$cm^2/mg. It is therefore unlikely that proton-induced secondary ions will cause on-orbit SEEs, assuming a low-inclination Low-Earth Orbit.

Three potential classes of SEFI events were identified, and one ("Class B") has subsequently been identified as a software-based error in the DAQ code. The remaining two classes of events are potentially flipped bits in either the analog configuration ("Class A") or the returned digital data ("Class C") leading to loss of analog signal or digitized data corresponding to nonphysical pixel locations. Each class was corrected with a reset or power cycle of the chip.

Cross sections for each data collection run are calculated by fitting the data to a Weibull curve [26] of the form

$$F(x) = A\left(1 - e^{-[(x-x_0)/w]s}\right), \tag{6.1}$$

where x is the effective LET, A is the limiting or plateau cross section, x_0 is an onset parameter such that $F(x) = 0$ for $x < x_0$, w is a width parameter, and s is a dimensionless exponent. Figure 13 shows conservative cross sections assuming all three event classes were SEFIs. Asterisks represent Class A events and blue filled circles represent Classes B and C. The light blue circles at high LET and low cross section are from runs with an average flux of $\leq 4 \times 10^4$/cm^2/s, whereas the dark blue points were collected with an average flux of ≤ 112/cm^2/s . The distinction is not made at lower LET, as this flux effect was not found with lower LET beams for similar fluences. To account for these flux effects when calculating an upper bound on-orbit SEFI rate, the data have been fit with two Weibull curves and event rates summed. Both curves consider all data with LET< 35 MeV*cm^2/mg. Curve 1 additionally includes only dark blue (high flux) data above 35 MeV*cm^2/mg whereas curve 2 includes only light blue (low flux) high-LET data. The fits are intentionally worst-case with steep increases and saturation levels at the highest cross section data point as opposed to an average. Corresponding Weibull parameters are given in Table 4.

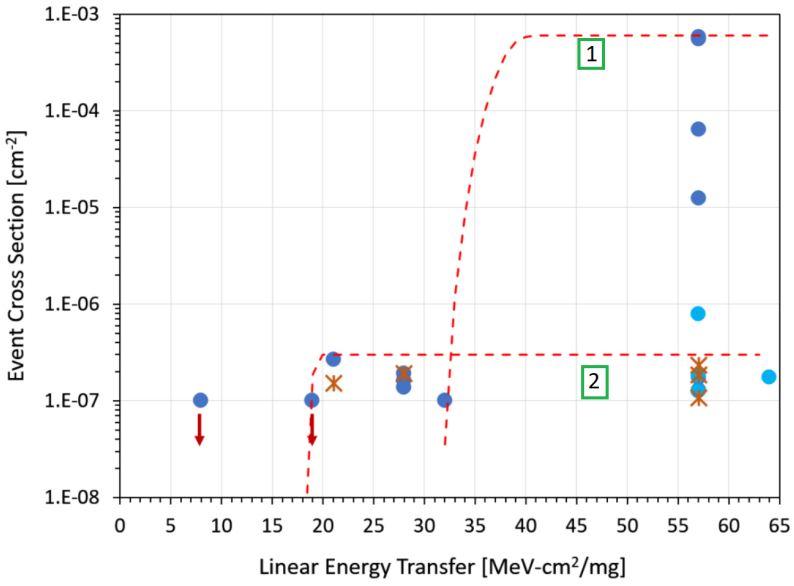

Figure 13. SEFI cross section with Weibull fits for low and high cross-section data. Blue filled circles are decoder events; asterisks are analog events. Red downward pointing arrows indicate data points with no events. Both curves include all data with LET< 35 MeV*cm^2/mg, and curve 1 (2) additionally includes only dark (light) blue (high [low] flux) high-LET data.

Using CREME96 [27], a worst-case galactic cosmic ray environment of interplanetary space at solar minimum was used to determine a SEFI rate. The sensitive volumes defined in CREME96 had x- and y-dimensions equal to the square root of the saturated cross section; each volume was assigned a depth of 2 μm. Although the pixel depletion volume is approximately 70 μm thick at the

Table 4. Weibull parameters for the curves of Fig. 13.

Curve	Saturation Cross Section [cm^{-2}]	Onset LET [$MeV*cm^2/mg$]	Power (s)	Width (w)
1	3.00×10^{-7}	18	5	1
2	6.00×10^{-4}	31	5	7

Table 5. Worst-case SEFI rate for interplanetary space at solar minimum.

SEFI rate per day	SEFI rate per year
2.386×10^{-4}	8.717×10^{-2}

voltage utilized for testing, the CMOS circuitry that is potentially responsible for the SEFIs will have a shallower sensitive volume. Within CREME96, this shallower volume yields higher event rates than would a deeper sensitive volume designation, conservatively bounding the rate. Total event rates for the worst-case assumptions described above are given in Table 5.

This result is unique to AstroPix_v2, though the digital block of AstroPix_v2 is identical to that of AstroPix_v3. The satisfactory results raise confidence in future designs. Future AstroPix versions will be tested in an identical manner to ensure continued compliance with spaceflight standards.

7 Conclusion and Outlook

The AstroPix design program is strong and robust as advances in the design are consistently made toward realizing a final version. AstroPix versions one through three show consistent improvements in key metrics such as power consumption and energy resolution, as shown in Table 1 however the design process is ongoing.

This paper has presented an overview of AstroPix_v3 HVCMOS design and benchtop operation. Current-voltage measurements illustrated chip properties, including high-voltage breakdown between $-380 - 400$ V. An overview of energy resolution studies and results from Ref. 16 were presented, where $10.4 \pm 3.2\%$ FWHM energy resolution at 59.5 keV was achieved using a medium-resistivity $200 - 400\ \Omega*cm$ substrate. The measured $94 \pm 6\ \mu m$ depletion of this substrate is discussed, and plans for increasing this depletion depth to the designed 500 μm were presented. Radiation testing with a cocktail of ions was performed with AstroPix_v2 which shares an identical digital bloc to AstroPix_v3, and no catastrophic events were detected. Single event functional interrupt rates were estimated to be at the order of 10^4 per day in the planned AMEGO-X orbit, which is a tolerable rate.

The first space-based test of AstroPix will be the Astropix Sounding rocket Technology dEmonstration Payload (A-STEP), featuring three AstroPix_v3 quad chips to be flown on a sounding rocket in 2025 [28]. The first large-format test of AstroPix is the AMEGO-X prototype tower ComPair2 [29], which is intended to fly on a high-altitude balloon. The other AMEGO-X subsystems and operations

team take heritage from the 2023 ComPair flight [30]. ComPair2 features 10 tracker layers with nearly 100 AstroPix_v3 chips per layer, which will interact with a unified trigger system to return science data. The results from this publication serve as a baseline for AstroPix_v3 operation, and will provide the basis for A-STEP design, optimization, calibration, and analysis.

At the time of writing, AstroPix_v4 has been fabricated and is undergoing preliminary testing [18]. This testing has informed the submission of AstroPix_v5 during the 2025 calendar year. Continued improvements in power consumption and dynamic range are expected with the elimination of an external fast 200 MHz clock and addition of dynamic feedback capacitance.

The AstroPix project benefits from the expertise of international collaborators in multiple fields of physics and engineering. Though not currently a final design, each AstroPix version improves upon the previous. The ultimate design will revolutionize γ-ray astronomy, especially in the elusive MeV range.

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