The ePIC Electronics and Data Acquisition Design Status, Fall 2024

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Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					183	5863	183	183	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M	128k	4k					60	82	14	301	16
PID (TOF)		6.1M				500	1364	500	500	14	50	12
PID Cherenkov			318k		143k			1283	1283	32	1275	32
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**843**	**9,787**	**2,788**	**2,810**	**95**	**1,774**	**109**

Fig. 1 ePIC DAQ component count summary.

1 Requirements

The electronics and data acquisition systems are required to digitize and readout the data provided by the sensors of all ePIC detectors. The Electronics must tag hits with a time resolution sufficient to identify the bunch crossing (10.16 ns) and provide high resolution time references as stringent as 5 ps according the specific detector needs. The ePIC readout system must provide high data volume links to front end electronics up to 10 Gb/s for selected components. The readout system must provide very high live times, with the goal of zero-system wide deadtime in normal operation, despite the possibility of by-channel deadtime according the specific readout technology of each detector.

The Data Acquisition will group streaming data into time frames of O(0.6 ms). The readout systems are expected to digitize up to O(2 Tb/s) and must be capable of reducing this data volume to an output rate of O(100 Gb/s) using techniques to compress signal and remove noise with minimal impact to signal integrity. The data from all running detectors for each time frame will gathered together in a single buffer for transfer to the echelon 1 computing facilities located at BNL and JLAB for archive and analysis.

1.1 Requirements from Physics

The scientific mission of ePIC is reflected in the requirements of the Electronics and DAQ through the scale and technology of the ePIC detectors shown in figures 1 and 2. Large channel counts combined with low occupancy lead to the need for multiple levels of aggregation at the Front End Boards (FEB), the Readout Boards (RDO) and the Data aggregation and Manipulation Boards (DAM).

The performance of the EIC Collider also impacts the requirements of the readout system. The collision rates and background rates have been calculated in the ePIC background group [1]. Two aspects are particularly important for the Electronics and DAQ.

The first is the maximum event rates, which we expect to be as high as 500 kHz for DIS, 3.2 MHz for Electron Beam Gas and 32 kHz for hadron Beam Gas. These rates are of primary interest within DAQ to estimate the data volumes which are described below.

The second consideration is that individual bunch crossing can have different polarization states. This implies that the luminosity and polarization of the beams must be tracked by bunch and produces the requirement that events must be associated to the bunch crossing from which they originated.

1.2 Requirements from Radiation Hardness

The electronics installed in the ePIC detector will be subjected to significant radiation doses. Expected radiation doses have been calculated by the ePIC Background group [1]. While the radiation distribution within the ePIC detector varies with the location, the worst case radiation dose is expected to be O(100 Krad) and O(1×10^{12} 1MeVn/cm^2) over ten years at maximum EIC luminosity. Although these doses are four orders of magnitude lower than radiation doses seen at the LHC, electronics must be chosen and placed to minimize failure rates. Transient failures such as single bit upsets (SEUs) must have a recovery process which

Detector System		Channels	ASIC	FEB	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
SI Tracking:	Inner Barrel (IB)	1.8B Pixels	160	592*	24	2.36	2.36	1	ITS-3 sensors &	ASIC corresponds to VTRX+ counts
	Outer Barrel (OB)	5.0B Pixels	495	1870*	55	3.52	3.52	2	ITS-2 staves / w	FEB corresponds to detector fiber
	Backward Disks (EE)	4.7B Pixels	462	1744*	52	4.68	4.68	2	improvements	RDO is off detector Fiber aggregator
	Forward Disks (HE)	4.7B Pixels	462	1744*	52	4.68	4.68	2		
MPGD tracking:	Electron Endcap	16,384	256	64	16	2.86	0.58	1	uRWELL / SALSA	VTRX+ based FEB
	Hadron Endcap	16,384	256	64	16	4.01	0.80	1	uRWELL / SALSA	
	Inner Barrel	32,768	512	128	32	4.10	0.82	1	MicroMegas / SALSA	
	Outer Barrel	98,304	1536	384	96	15.81	3.16	2	uRWELL / SALSA	
Forward Calorimeters:	LFHCAL	63,280	1130	1130	74	18.54	2.47	2	SiPM / CALOROC	CALOROC:
	HCAL Insert	8k	142	142	9	17.72	2.36	1	SiPM / CALOROC	56 Ch/CALOROC
	ECAL W/SciFi	18,320		574	72	14.75	7.36	2	SiPM / Discrete	16 CALOROC / RDO
Barrel Calorimeters:	HCAL	1,536	28	28	2	0.87	0.12	1	SiPM / CALOROC	
	ECAL SciFi/PB	5,760	102	102	4	11.45	1.52	1	SiPM / CALOROC	Discrete:
	ECAL ASTROPIX	500M pixels			340	1.25	1.25	8	Astropix	32 Ch/FEB,
Backward Calorimeters:	NHCAL	3,256	58	58	4	3.46	0.47	1	SiPM / CALOROC	8 FEB/RDO conservative (16 estimate).
	ECAL (PWO)	2,852		102	13	2.00	0.99	1	SiPM / Discrete	
Far Forward:	B0: Crystal Calorimeter	135		5	1	2.3	2.3	1	SiPM/APD / Discrete	
	4 AC-LGAD layer	688,128	672	168	42	12.75	2.1	1	AC-LGAD / EICROC	4 layer x 42 module x 4 EICROC x 1024 ch
	2 Roman Pots	524,288	512	128	32	14.53	2.1	1	AC-LGAD / EICROC	2 stations x 2 layer x 32 module x 4 EICROC x 1024 ch
	2 Off Momentum	294,912	288	72	18	3.53	0.7	1	AC-LGAD / EICROC	2 stations x 2 layer x 18 module x 4 EICROC x 1024 ch
	ZDC: Crystal Calorimeter	900		30	4	2.30	4.5	1	SiPM/APD / Discrete	
	HCAL	9,216	165	165	11	0.22	.22	1	CALOROC	
Far Backward:	2 x Low Q Tagger	66M pixels	3456	288	24	37	.3	10	Timepix4	Firmware Trigger to reduce output rate
	2 x Low Q Tagger Cal	420			1	-	-	1	SiPM / CALOROC	Low Q Calorimeter doesn't run at high luminosity
	2 x Lumi PS Calorimeter	3,360			1	19	7	1	SiPM / Discrete	
	2 x Lumi PS tracker	128k	1000	250	64	45	2	2	AC-LGAD: FCFD or EICROCx	
	Direct Photon Lumi Cal	100		24	24*	200	7	1	SiPM / fADC250	Direct Photon: commercial digitizer, no RDO
PID-TOF:	Barrel	2,359,296	18,432	288	288	15.95	4.79	8	AC-LGAD: FCFD or EICROCx	bTOF 128 ch/ASIC, 64 ASIC/RDO
	Endcap	3,719,168	3,632	212	212	33.92	7.34	6	AC-LGAD: EICROC	eTOF 1024 pixel/ASIC, up to 28 ASIC/RDO
PID-Cherenkov:	dRICH	317,952	4968	4968	1242	1240	13.5	30	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction Firmware trigger
	pfRICH	69,632	544	68	17	24	12.5	1	HRPPD / FCFD or EICROCx	
	DIRC	73,728	576	144	24	11	6	1	MCP-PMT / FCFD or EICROCx	

Fig. 2 ePIC DAQ component counts

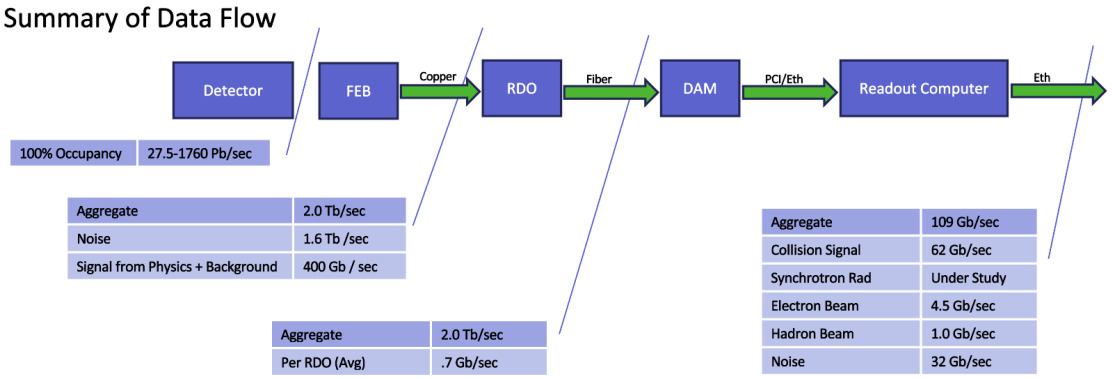

Fig. 3 Expected worse case data rates contributions for the ePIC detector

Detector	Noise (Hz/channel)
ITS3, Astropix, Timepix	0.01
AC-LGAD	30
HRPPD	230
dRICH(Initial)	1,500
dRICH(Maximum)	300,000
All Others	$4.5\sigma = 340$

Table 1 Noise Estimates By Detector

automatically senses, initiates, and accomplishes recovery while running in order to avoid downtime. There are commercial IP cores available for FPGAs that can support recovery from simple SEUs. More complex (multi-bit) failures will require an automated reset and reload feature for FEBs and RDOs. The electronics placed in the central detector (SVT, eTOF, bTOF, and MPGDs) will accumulate significant radiation and will utilize radiation hard components to minimize it's effect.

1.3 Requirements from Data Rates

The triggerless readout of the ePIC detector uses zero-suppression to help manage the volume of data read out. The streaming model's sensitivity to noise, beam background, and collision data make the understanding of these effects critical. Collision, synchrotron radiation and beam gas backgrounds from both the electron and hadron beams have been studied extensively by the ePIC collaboration [1].

The hit rate for the collision signal is taken from simulated hits for DIS events generated by the ePIC physics and detector simulations. The simulated data set was taken for 18x275 GeV collisions with $Q^2 > 0$ with luminosity 1.54×10^{33} cm^{2}s^{-1}. The collision rate was 83kHz, but the hit rates were scaled to the maximum rate of the EIC collider of 500kHz. Hadron and electron beam gas events were generated using the simulated vacuum profile after 10,000 Ah of pumping. Noise calculations are currently based on the ePIC detector group expert estimates and shown in table 1.

One additional factor that must be considered is dark currents in the SiPM detectors which increase with radiation damage. In particular, this issue affects the dRICH, in which the SiPM threshold must remain low enough to be sensitive to single photons. At these thresholds the dark current rates are expected to be 1.5 kHz/ch @ -40 C. These rates will increase to 300 kHz/ch after several years of radiation damage.

There are several features planned to reduce these dark currents including annealing, and implementation of timing windows to synchronise readout with collision times. The DAQ system must be designed with the capability to read the highest rates expected by the dRICH to the DAM board. The DAQ must also be able to apply filters to reduce the dRICH noise at the DAM board, either by applying a firmware trigger or by using specialized AI algorithms to determine which hits correspond to a dRICH physics signal.

Finally, noise is expected to be a potential issue in all other detectors as well. Generally, the noise level can be controlled with thresholds. The acceptable noise level by detector is planned to be set according to the full data bandwidth requirements.

Detector	Channel Max Hit Rate (Hz)	Noise To RDO (gbps)	Noise Per RDO (gbps)	Noise To Tape (gbps)	RDO (max) (gbps)	RDO_max / with Noise (gbps)
SiBarrelTracker	4.13E-04	3.25	0.06	3.25	0.00	0.06
SiBarrelVertex	5.22E-03	1.15	0.05	1.15	0.17	0.21
SiEndcapTracker	2.78E-03	6.02	0.06	6.02	0.23	0.29
BackwardMPGDEndcap	2.19E+02	1.74	0.11	0.35	0.42	0.52
ForwardMPGDEndcap	4.44E+02	1.74	0.11	0.35	0.86	0.97
MPGDBarrel	8.67E+01	3.26	0.10	0.65	0.04	0.14
OuterMPGDBarrel	1.29E+01	15.23	0.16	3.05	0.01	0.17
LFHCAL	2.10E+04	10.33	0.14	1.38	1.30	1.44
HcalEndcapPInsert	6.18E+04	1.31	0.15	0.17	2.78	2.93
EcalEndcapP	1.51E+05	0.78	0.01	0.35	2.69	2.70
HCcalEndcapN	7.81E+04	0.53	0.13	0.07	2.64	2.77
EcalEndcapN	8.07E+04	0.14	0.01	0.06	1.06	1.07
HcalBarrel	1.30E+03	0.25	0.13	0.03	0.08	0.21
EcalBarrelImaging	2.92E-02	0.32	0.00	0.32	0.01	0.01
EcalBarrelSciFi	1.52E+03	0.94	0.07	0.13	2.69	2.76
TOFBarrel	1.74E+00	13.59	0.05	4.53	0.01	0.06
TOFEndcap	8.34E-01	32.13	0.15	7.14	0.07	0.22
hpDIRC	2.35E+02	3.22	0.13	1.07	0.00	0.13
pfRICH	4.99E+02	3.05	0.18	1.02	0.00	0.18
dRICH	1.09E+02	1220.94	0.98	6.10	0.00	0.98
B0 Crystal Calorimeter	2.66E+05	0.00	0.00	0.00	0.00	0.00
B0 AC-LGAD	1.72E+01	5.95	0.20	1.32	0.00	0.20
RP	3.31E+01	4.53	0.21	1.01	0.00	0.21
OM	5.93E+00	2.53	0.21	0.56	0.00	0.21
ZDC Crystal Calorimeter	7.81E+04	0.02	0.00	0.02	0.00	0.00
ZDC HCAL	3.39E+01	0.20	0.02	0.20	0.00	0.02
DirectPhoton	2.00E+08	0.00	0.00	0.00	0.00	0.00
LowQ2Tracker	8.76E+00	0.04	0.00	0.04	0.00	0.00
LowQ2Calorimeter	0.00E+00	0.01	0.01	0.01	0.00	0.01
PairSpectrometerTracker	2.44E+02	0.74	0.07	0.25	0.00	0.07
PairSpectrometerCalorimeter	3.26E+04	0.07	0.07	0.07	0.00	0.07
Total		1334.01		40.67		

Fig. 4 Maximum data volume per RDO with noise estimates.

We have summed the expected hits from each of these sources and converted to data volumes using our current understanding of zero suppression and data formats of each detector readout. Furthermore, the distribution of hits to each component has been estimated by arbitrarily assigning readout components to the sensitive planes of the detectors in order to estimate the impact of potential bottlenecks.

The data volumes expected, including collisions, background and noise for the worse case RDO by detector, is shown in table 4.

2 Device Concept and Technological choice: Streaming Readout

The ePIC readout system will implement a flexible, scalable, and efficient streaming DAQ as outlined by the EIC Yellow Report [2]. This design will provide the advantages of streaming include the replacement of custom L1 trigger electronics with commercial off-the-shelf (COTS) computing, virtually deadtime-free operation, great flexibility in event selection using full event data along with offline analysis, and the opportunity to study event backgrounds in detail. These advantages come at the cost of greater sensitivity to noise and background. A schematic of the readout system is show in figure 5.

The components in the ePIC readout system are shown in figure 6. Readout will be accomplished using detector specific front end sensors and adaptors. Even though the organization of the front end electronics varies by detector needs the custom electronics of each system generically referred to as Front End Boards (FEBs). There is no global trigger system in ePIC, instead each FEB is required to self-trigger, providing a stream of hit data. Digitization and zero-suppression are typically handled with ASIC support in the FEB. Each FEB has similar needs for clocks, configuration, and serial data links. These needs are provided by

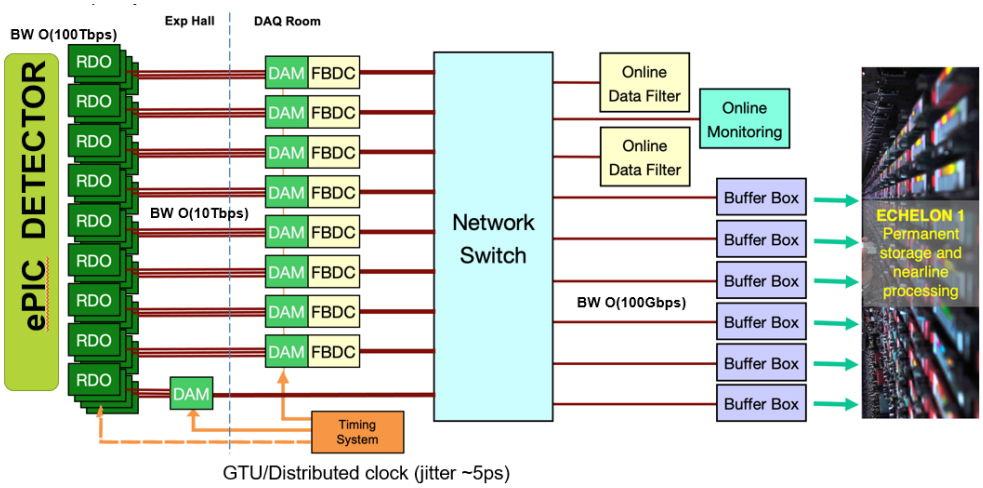

Fig. 5 Schematic of the ePIC Streaming DAQ

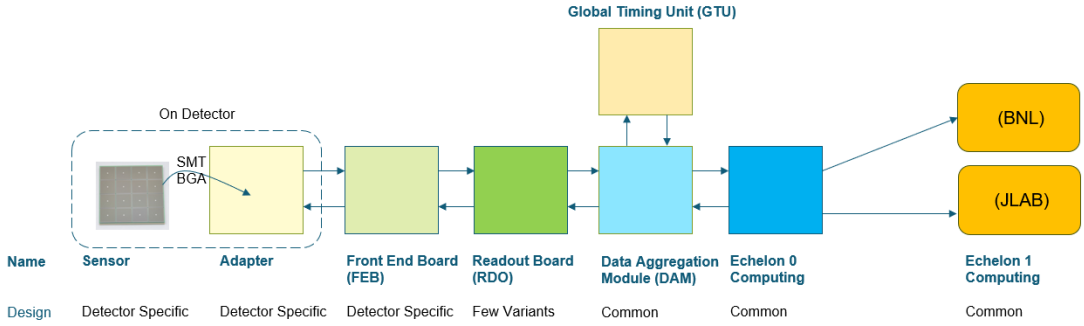

Fig. 6 Components of the ePIC Streaming DAQ System

Readout Boards (RDOs). The RDOs also aggregate data from the FEBs. The RDOs are driven by either FPGAs or lpGBT. The RDO serves as an interface between custom, technology driven, readout schemes of specific detectors and the ePIC DAQ. While there are a number of variations of the RDOs depending upon the FEB technology, all of the RDOs support a unified ePIC DAQ fiber protocol. They distribute high-resolution time reference, configuration, and control to the FEBs and transmit hit data and monitoring information to the Data Aggregation and Manipulation Boards (DAM).

The DAM boards have significant FPGA processing available for implementing firmware triggers and other data reduction algorithms. They also provide further aggregation and function as the interface between the electronics and the first level of COTS computers called the Frame Builder Data Collectors (FBDC). The farm of COTS DAQ computers dedicated to readout, data reduction, logging, monitoring, QA and data buffering and transfer to data centers is integrated in the ePIC computing model and referred to as echelon 0.

Synchronizing the front end electronics and provide high resolution time reference to beam crossings is an important requirement of the streaming DAQ. The Global Timing Unit (GTU) is the interface to EIC collider controls. It receives the 98.5Mhz bunch crossing clock, orbit information, and beam polarization information and distributes it via the DAM boards to the RDOs and FEBs. The GTU is the only global source of real time information provided to the FEB/RDOs, so it must provide information a trigger system would normally provide. These functions include the ability to synchronize data from different detectors, to send flow control signals, to pass bunch information such as spin orientations and bunch structure, the ability to provide user defined signals for signaling special data formatting or calibration needs, and the ability to implement a hardware trigger for debugging or as a fallback option to solve unforeseen readout issues.

The communication between the RDOs, DAM, and GTU will use an unified data protocol serving five functions:

- The distribution of configuration information from the DAQ System to configure the RDOs.

Implementation	Detector/Sensor	Key Attributes
Discrete	Calorimeter/SiPM	COTS devices, 14-bit digitization
CALOROC	Calorimeter/SiPM	ASIC, 10-bit digitization
EICROC	AC-LGAD, pixel	ASIC, High-precision timing for Cd < 5 pF
FCFD	AC-LGAD, strip	ASIC, High-precision timing for Cd < 10 pF
ALCOR	dRICH/SiPM	ASIC, uses shutter for 1 p.e. sensitivity
SALSA	MPGD	ASIC, peaking time to 50 ns, includes DSP

Fig. 7 ePIC Electronics and ASICs summary

- The distribution of configuration information to the FEBs via the RDOs.
- The distribution of real-time control information to the RDO and FEBs,
- The distribution of a high-resolution beam crossing timing signal to the RDO and FEBs,
- The high performance (∼10 Gb) transfer of hit data and monitoring information from the FEBs and RDO to the DAM boards.

3 Subsystem Description (components)

3.1 Readout Electronics and ASICS

3.1.1 Overview

Readout electronics are being developed based on the sensor technologies. Common requirements among various sub-detectors have been identified to maximizing synergy. The readout electronics conforms to the ePIC streaming readout model with triggerless operation and serial interfaces. To facilitate calibration and debugging, capability for triggered operation is also implemented. The development of the readout electronics and ASICs are summarized in figure 7.

3.1.2 Discrete

The Discrete readout implementation addresses the readout from calorimeters with SiPMs where high resolution digitization is required and commercial devices (COTS) are employed. The design and technologies will be validated for specific locations within the ePIC detector, where radiation hardness of COTS devices will need to be verified. The block diagram is shown in figure 8.

The circled area in fig. 8 delineates the Adapter section with SiPMs and bias circuitry; the remaining parts make up the FEB PCB, which includes signal conditioning, ADCs and readout logic. The Adapter and FEB PCBs are located at the detector, as a stack, and CAT6 cables are employed for serial interfaces. Key specifications are shown in figure 10. Prototypes of the Adapter and FEB PCBs are shown in figure 9.

3.1.3 CALOROC

The CALOROC ASIC is currently under development to address readout from calorimeters with SiPMs and for which a 10-bit resolution digitization with wide dynamic range capabilities is applicable. The CALOROC design is based on the existing H2GCROC ASIC for SiPMs with similar frontend and a backend, or digital section with interfaces, conforming to the needs of the streaming readout approach at the EIC. In parallel, tests with the H2GCROCv3 chip continue to provide input and validation into the design of the CALOROC ASIC. There are, however, two frontend variants being considered: CALOROC1A uses an ADC, a TOA and a TOT for wide dynamic range, similar to the H2GCROC; CALOROC1B uses a different frontend architecture making use of dual gain switching techniques to extend its dynamic range. The CALOROC block diagram is shown in figure 11 and its specifications summarized in figure 12.

3.1.4 EICROC

The EICROC ASIC is currently under development to address readout from AC-LGAD pixel detectors with low detector capacitance (Cdin) and very stringent timing precision requirements. The EICROC design is

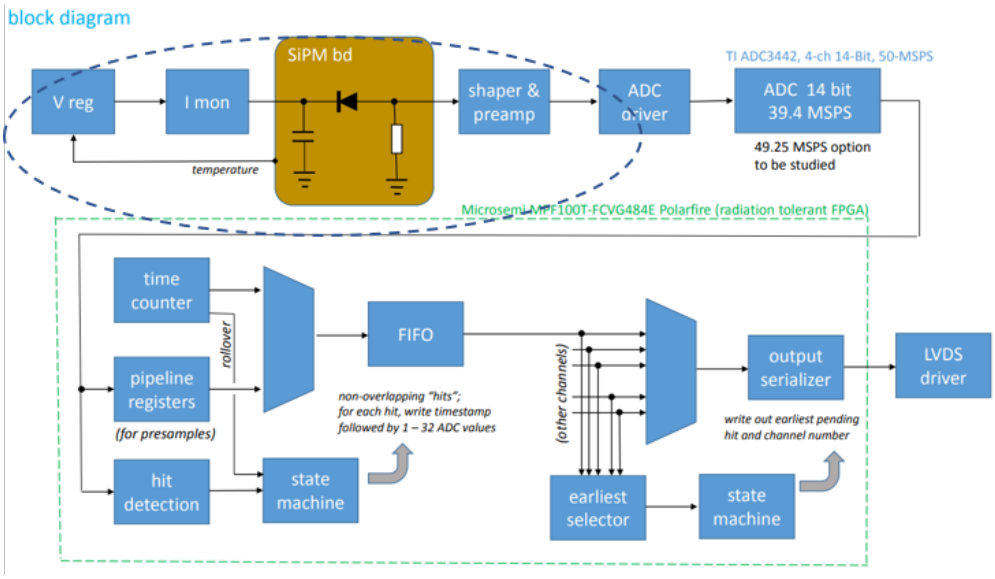

Fig. 8 Discrete block diagram

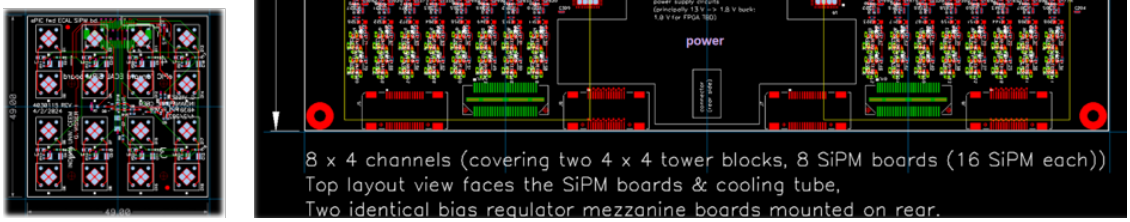

Fig. 9 Discrete Adapter (left) and digitizer FEB PCBs

Function	Waveform digitizer with COTS devices
Channels	32
Digitizer	TI ADC 3422
Resolution	14-bit (12-bit also available)
Shaping	80 ns peaking time
FPGA	Microsemi MPF100T-FCVG484E Polarfire (Rad Hard)
Power	DC-DC converter (bPOL12V, bPOL48V, LTC36xx)
Cooling	Liquid
Cabling	CAT6

Fig. 10 Discrete key specifications

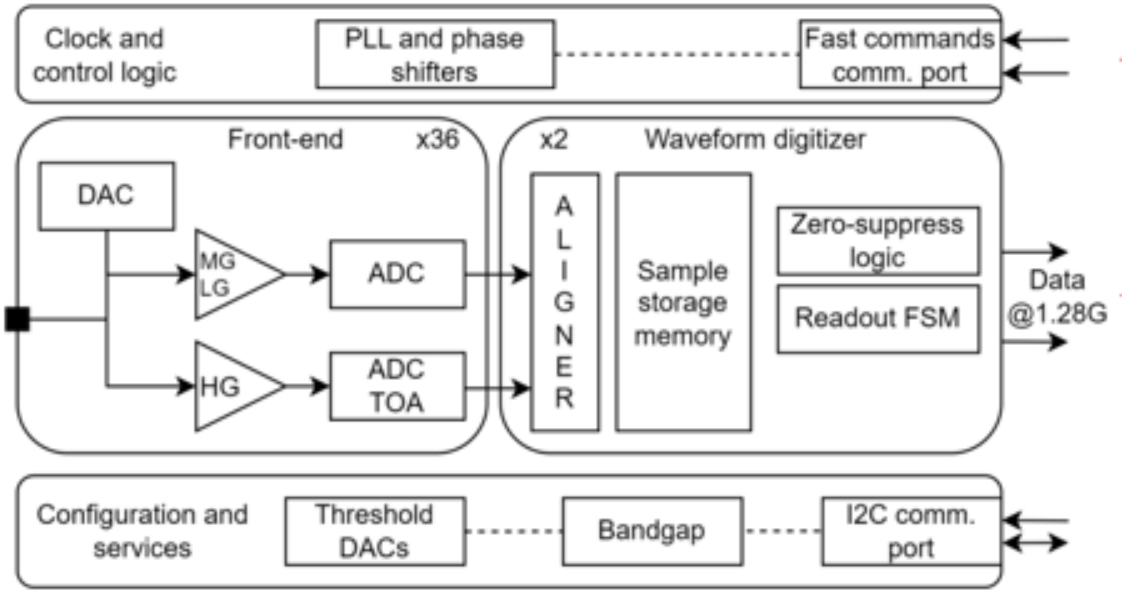

Fig. 11 CALOROC block diagram

Function	Charge and timing digitization from SiPMs
Tech Node	130 nm CMOS
Channels	64
Cdin	500 pF – 10 nF
Digitization	Charge: 10-bit ADC, 15-bit TOT; Timing: <500 ps TOT (1 MIP)
Dynamic Range	Up to 12 nC
Clock	39.4 MHz operation from BX 98.5 MHz
Links	1260.8 Mbps @ 39.4 MHz, multiple
Power	10 mW/ch
Package	BGA
Rad Tolerance	Radiation hard

Fig. 12 CALOROC Key Specifications

based on the existing HGCROC ASIC for Si and PMTs with similar frontend and a backend, or digital section with interfaces, conforming to the needs of the streaming readout approach at the EIC, which is already being designed for the CALOROC. Main IP blocks consist of preamp, discriminator, TOA, ADC and TDC. The EICROC block diagram is shown in figure 13 and its specifications are summarized in figure 15. Figure 14 shows the EICROC timing performance with varying charge from input signals.

3.1.5 FCFD

The FCFD ASIC is currently under development to address readout from AC-LGAD strip detectors with medium detector capacitance (Cdin) and very stringent timing precision requirements. The FCFD design implements the constant fraction discriminator technique for high precision timing without time-walk corrections. The backend, which is currently being considered, may be based on the existing ETROC ASIC or the EICROC development. The FCFD block diagram is shown in figure 16 and its specifications are summarized in figure 18. Figure 17 shows the FCFD timing performance with varying charge from input signals.

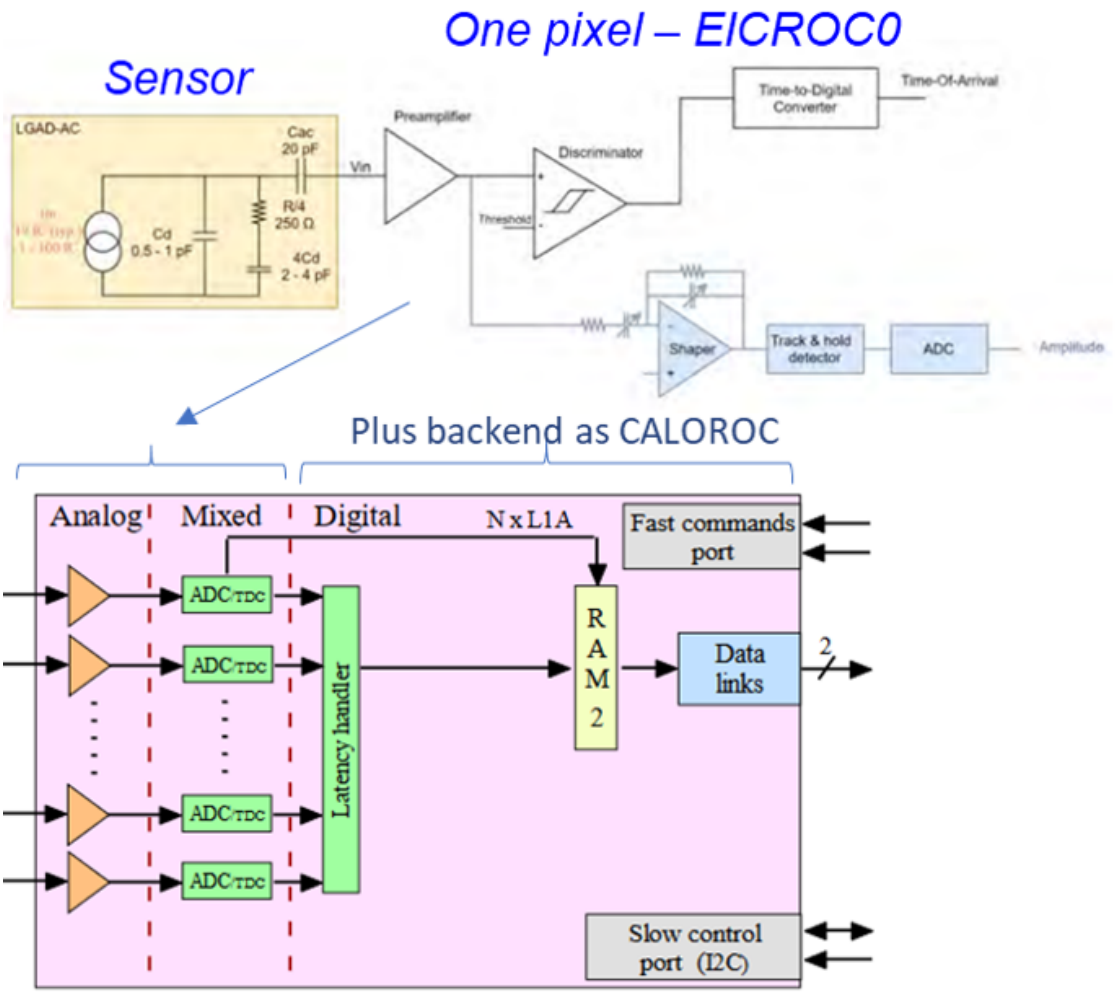

Fig. 13 EICROC block diagram

3.1.6 ALCOR

The ALCOR ASIC is currently under development specifically for the readout of the dRICH detector with SiPMs due to its single photo-electron sensitivity requirement. The ALCOR design includes trans-impedance amplification (TIA) with regulated common gate (RCG) bias for low noise, inhibit or shutter operation to limit contribution from dark-rate SiPM noise and TDCs to allow for single-photon tagging or time and charge digitization. The shutter function is a critical aspect of this ASIC and it is programmable for width and latency. The ALCOR Die and block diagram are shown in figure 19 and its specifications are summarized in figure 20.

3.1.7 SALSA

The SALSA chip is an ASIC currently under development, foreseen to do the readout of the different MPGD trackers, namely the barrel cylindrical Micromegas, the barrel μRWELL and the end-cap μRWELL detectors. The purpose of SALSA is to amplify, shape and digitize signals coming from the MPGD detectors, and then perform basic data processing on the digitized samples before to transmit them to the next element of the data acquisition chain. It gathers in a single die a CSA pre-amplifier, a shaper and an ADC for each of the 64 channels, followed by a DSP which performs baseline corrections, digital shaping and a zero-suppression in order to reduce the output data bandwidth. Furthermore, to reduce data output even more, a peak finding algorithm is implemented to extract from samples information like amplitude and time of detected hits.

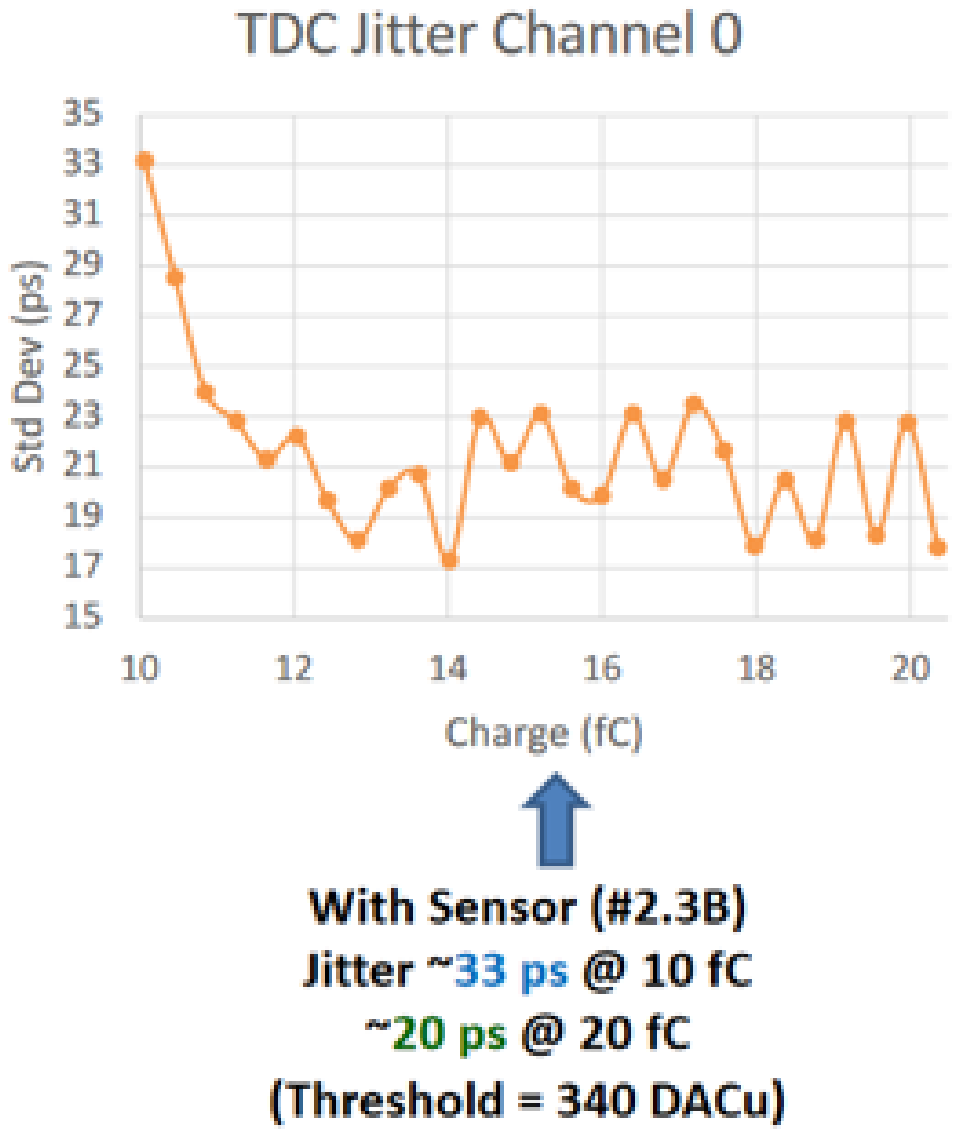

Fig. 14 EICROC timing performance

Function	Timing digitization from AC-LGAD pixels
Tech Node	130 nm CMOS
Channels	1024 (32x32)
Cdin	1 – 5 pF
Digitization	ADC: 8-bit, TDC: 10b; Timing: 30 ps
Dynamic Range	1 – 50 fC
Clock	39.4 MHz operation from BX 98.5 MHz
Links	1260.8 Mbps @ 39.4 MHz, multiple
Power	<2 mW/ch
Package	Bump + wire bonds
Rad Tolerance	Radiation hard

Fig. 15 EICROC Key Specifications

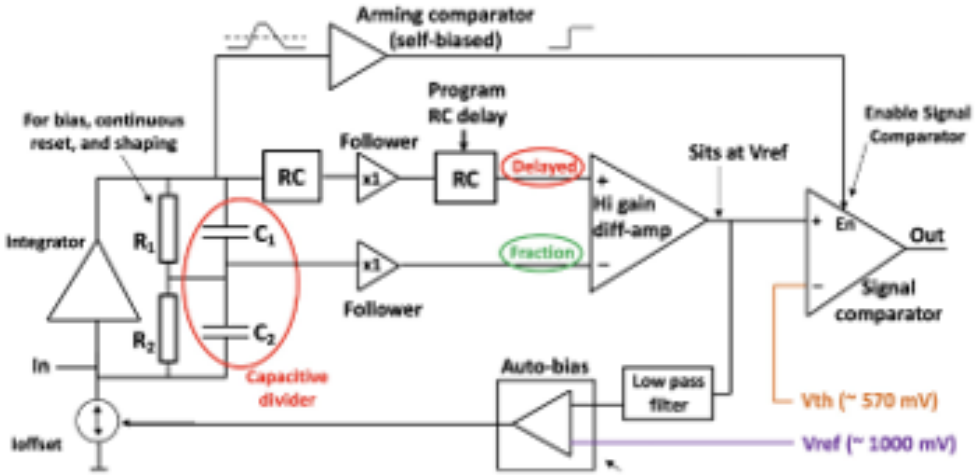

Fig. 16 FCFD block diagram of the frontend

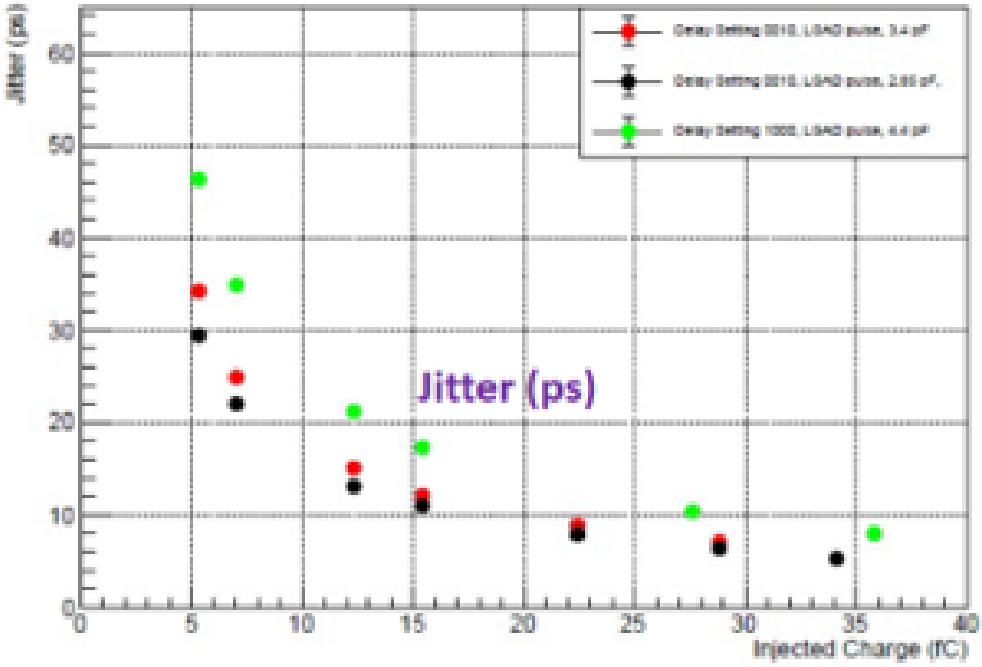

Fig. 17 FCFD timing performance

Function	Timing digitization from AC-LGAD strips
Tech Node	65 nm CMOS
Channels	128
Cdin	<15 pF
Digitization	TBD; Timing: 10 - 30 ps
Dynamic Range	5 – 40 fC
Clock	39.4 MHz operation from BX 98.5 MHz
Links	1260.8 Mbps @ 39.4 MHz, multiple
Power	<2 mW/ch
Package	Bump + wire bonds
Rad Tolerance	Radiation hard

Fig. 18 FCFD Key Specifications

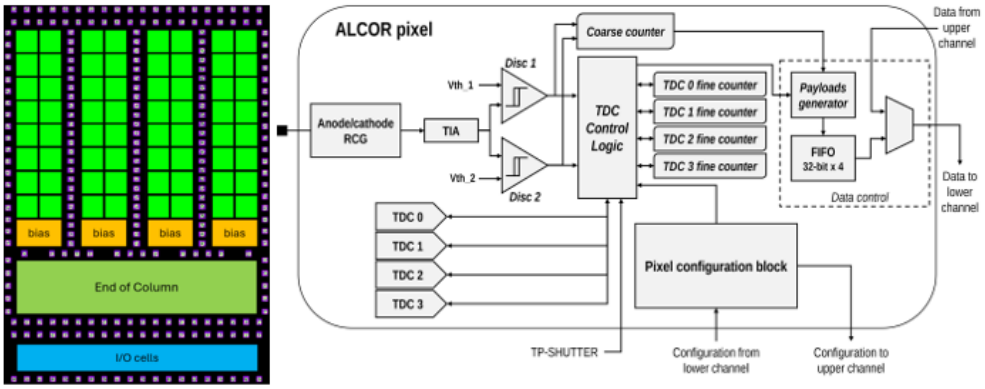

Fig. 19 ALCOR Si Die (left) and block diagram

Function	Digitization from SiPMs with 1 p.e. sensitivity
Mode	Single-photon tagging or time and charge
Tech Node	110 nm CMOS
Channels	64 (8x8), dual polarity
Cdin	<1 nF
Digitization	20-40 ps TDCs, TOA + TOT; Timing <150 ps
Shutter	Width: 2–3 ns, programmable latency
Input Rate	<2.4 MHz (up to 5 MHz on single channel)
Clock	394.08 MHz operation from BX 98.5 MHz
Links	788 Mbps LVDS, SPI configuration
Power	12 mW/ch
Package	BGA
Rad Tolerance	Radiation hard

Fig. 20 ALCOR Key Specifications

It will be able to work both in the streaming readout environment foreseen at EPIC, and in a triggered environment.

The characteristics, performances and configurability of SALSA are designed to make the ASIC very versatile, being able to be adapted to several kinds of MPGD detectors and to several applications. It will be able to work with a large range of signal amplitudes, a large range of electrode capacitance and large range of signal rise times. Its target specifications are summarized in the Table 2.

Scope of the Effort

The scope of the electronics and ASICs developments is summarized in figure 21, based on the number of readout channels, technologies employed and institutions developing these readout solutions.

It is noted that the pfRICH and the hpDIRC detectors benefit from the FCFD and the EICROC developments due to their timing precision requirements. The FCFD is, however, the nominal choice due to its lower channel density packaging for these applications with higher detector capacitances, which enable tailoring their timing performance via detector bias adjustment.

3.2 FEB components

3.2.1 DC/DC converters

DC/DC converters are employed throughout ePIC for the efficient distribution and regulation of the various sub-systems. The bPOL12V and bPOL48V DC/DC modules are selected for their radiation hardness and high magnetic field tolerances. Designs based on the LTC36xx family of devices will also be employed after proper validation.

Specification	Values	Remarks
Number of channels	64	
Input capacitance	50-200 pF	Reasonable gain up to 1 nF
Peaking time range	50 - 500 ns	
Max gain range	50 fC to 5 pC	
Max input rate	100 kHz/channel	Fast CSA reset
Signal polarity	Negative and positive	
ADC max sampling rate	50 MS/s	
ADC dynamics	12 bits	More than 10 effective bits
DSP processing	Baseline correction, filter, zero-suppression, peak finding	
Readout modes	Streaming readout, triggered	
Output data links	4 Gigabit links	1 only used at EPIC
Die technology	TSMC 65nm	
Die size	$\sim$1 cm^2	
Power consumption	$\sim$ 15 mW/channel	
Radiation hardness	Up to 300 Mrad and 10^{13} n_{eq}/cm^2	

Table 2 Main specifications of the SALSA chip.

	# Ch	# Ch/ Unit	#ASICs/ Wafer	#Wafers	Node (nm)	Package	Institution
Discrete/COTS	24 k	32	NA	740 Digitizers	COTS	NA	IU
CALOROC	97 k	64	480	5	130	BGA	OMEGA/IN2P3/IJCL/ORNL
EICROC	5.2 M	1024	160	42	130	Wafer Bump	OMEGA/IN2P3/IJCL/CEA-IRFU/AGH
FCFD	2.6 M	128	180	149	65	Wire Bond	FNAL
ALCOR	318 k	64	800	8	110	BGA	INFN
SALSA	202 k	64	500	9	65	BGA	CEA-Saclay/U of Sao Paulo

Fig. 21 Scope of the electronics and ASICs developments

3.2.2 lpGBT

The low power Giga-Bit Transceiver (lpGBT) chip [3] will be extensively used in ePIC sub-systems to provide aggregation and fiber interfaces to the FEB ASICs. It is capable of downlink serial communications of up to 2.5 Gbps and uplink serial communications of up to 10.24 Gbps. The lpGBT is radiation hard with Serializer/Deserializer (SERDES) functionality.

3.2.3 VTRX+

The VTRX+ module [4] is an electro-optical receiver/driver which will be extensively used in ePIC to interface to multi-mode optical fibers with MT optical connectors. One (1) receiver Rx (2.5 Gbps) and four (4) transmitters Tx (10 Gbps) are implemented. The VTRX+ is radiation hard and it is tolerant to high magnetic fields; it has a small footprint, has low power consumption and interfaces directly to the lpGBT transceiver devices.

3.3 RDOs

The RDO aggregates ASIC information from the multiple front end boards. The RDO also has the function of delivering a high resolution clock (<=5 ps jitter) to the front end boards. This clock is reconstructed from the data downlink fiber. The final function of the RDO is act as the interface between the detector specific function of the ASICS to the global ePIC DAQ fiber protocol. This protocol labels bunch crossings, organizes

Target Detector	Input	Output	technology
TOF Pre-Prototype, Calorimeters	copper	SFP+ fiber	FPGA
dRICH	copper	VTRX+ fiber	FPGA
SVT, MPGD, AC-LGAD second level	fiber	fiber	FPGA
AC-LGAD	copper	VTRX+ fiber	lpGBT
Imaging Calorimeter (Astropix)	copper	fiber	FPGA
Low Q^2 Tagger (Spyder3 Board)	copper	up to 12 fiber	FPGA
Direct Photon Detector	copper	fiber	flash

Table 3 Types of RDO

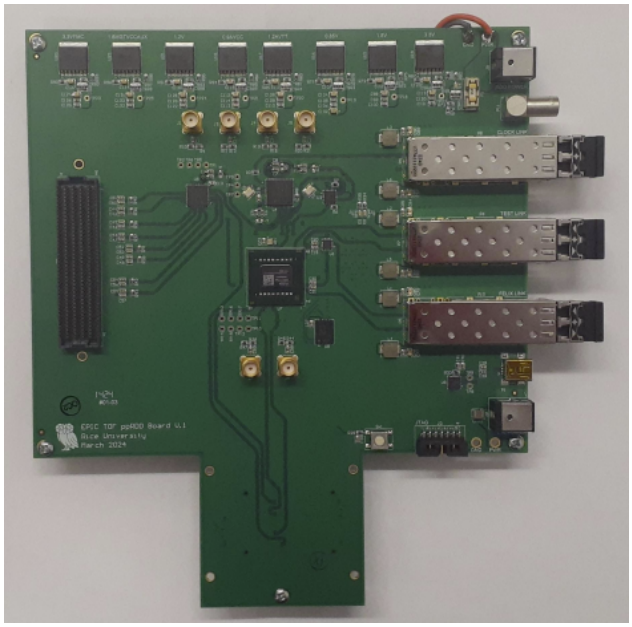

Fig. 22 TOF pre-protype RDO

time frames, uses user defined fast commands to communicate with the ASICs and provides the capabilities for firmware triggering and flow control.

However, several detectors: the SVT, the MPGD based detectors, and all AC-LGAD based readouts will make use of lpGBT or lpGBT-like aggregation using VTRX+ transceivers. The lpGBT aggregates ASIC information, and deliverers a high resolution reconstructed clock. However, it attempts to give a transparent interface to the ASICs. It does not have the capability of implementing the full ePIC protocol. For these RDOs the protocol will be implemented at the next level, either inside the DAM board or in a second level fiber to fiber RDO.

There will be several versions of the RDO depending on the needs of the specific detectors. The different RDO types are summarized in table 3

3.3.1 TOF pre-prototype RDO (FPGA based copper to SFP+)

The TOF pre-prototype RDO was designed to use elements common to most ePIC detector RDOs. These elements include Xilinx Ultrascale+ Artix FPGA, SFP+ fiber optics interface, clock cleaner PLLs, and clock recovery. The pre-prototype has been produced and is undergoing measurements of power usage and clock jitter. The board is shown in figure 22.

3.3.2 dRICH RDO

The dRICH RDO is part of the dRICH Photo Detector Unit PDU. 1248 PDUs will serve the dRICH. It provides read-out of four 64-channel ALCOR ASICs, each installed on a separate FEB. The space constraints are particularly demanding: the total RDO area is 40x9 mm^2 - quite similar to a credit card - requiring a devoted design, given the high integration of data buses and services within the PDU. The FPGA providing

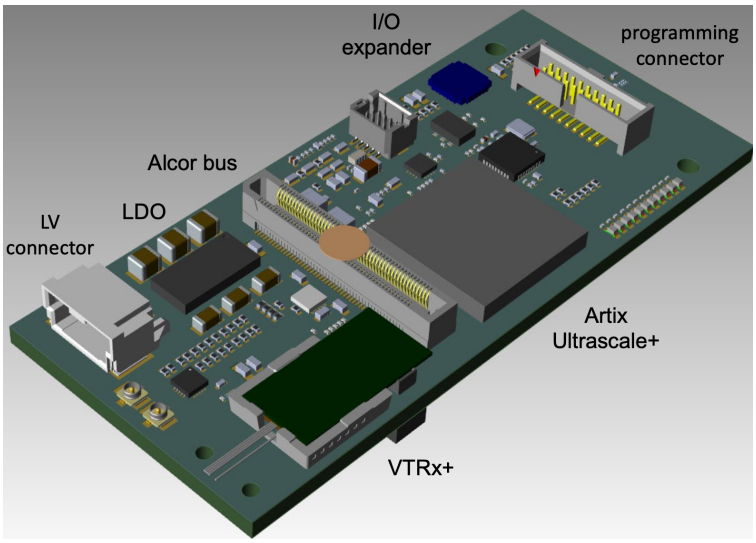

Fig. 23 3D model of dRICH RDO

readout of the ALCOR is an AMD Artix Ultrascale+ AU15P-SBVB484, complemented by a PolarFire FLASH-based FPGA MPF050T-FCSG325. The latter will support remote programming and continuous scrubbing of configuration bits of the SRAM-based AMD FPGA, to protect against SEU. Given the space constraints and the need to curb power consumption (total RDO power is expected $\approx$ 4 W) the CERN-developed VTRX+ optical transceiver has been selected, directly connected to the AMD FPGA SERDES. The maximum throughput per link (reached at maximum radiation damage before annealing) is foreseen not exceeding 2 Gbps, safely within VTRX+ specifications The ALCOR will be read out at 394 MHz, with a clock multiplier and jitter-attenuator (Skyworks Si5326) deriving this clock from the reconstructed EIC clock. A Microchip microcontroller provides power management and acts as watchdog against SEL. The first prototype of this card is under production and will be intensively tested during 2025, including irradiation tests. A 3D-rendering of the card is shown in Fig. 23.

3.3.3 Fiber to Fiber RDO

The fiber to fiber RDO is to be used with lpGBT-like FEBs to convert the transparent ASIC interface to the ePIC DAQ protocol. They are also necessary to further aggregate the fibers, particularly in the case of SVT and bTOF, where large numbers of low-data utilization fibers are required.

3.3.4 lpGBT based copper to fiber RDO

This RDO is yet to be designed, but is required for the lpGBT based readout of the inner detectors.

3.3.5 Astropix End of Stave Card (RDO)

This RDO is to be developed by NASA for use with the Astropix sensors.

3.3.6 Low Q^2 RDO

This is a RDO specifically for the low Q^2 taggers. It is expected to be an updated version of the Spyder3 board. These use the timepix sensor and have high potential data volumes, requiring several uplink fibers per RDO.

3.3.7 Flash based RDO

The Flash RDO is a specialized interface for the Direct Photon Detector. This detector has only about 100 channels, but is expected to have very high occupancy, and as such the appropriate technology is to digitize all data at 200 MHz and stream it directly to the DAM boards which will summarize the information, writing

out only the summed energy deposited each bunch crossing, or histograms of the bunch crossing energies according to bunch number.

3.4 DAM - Data Aggregation and Manipulation Hardware

For the ePIC DAQ system the DAM boards will be used as the primary aggregation point for the "raw" detector data streams. Because these boards are also the final aggregation points for the front-end (hardware managed) DAQ, there will need to be some well-defined but configurable algorithms for merging streams and managing potential congestion and data loss both for the incoming detector streams and the outgoing aggregated streams being queued up for online processing.

In Addition, the DAM boards will interface with the Global Timing Unit (GTU) hardware via a proprietary communication protocol that supports a synchronized EIC clock distribution to all subsystems and general DAQ/Run control and configuration. Finally, the DAM will act as the slow control interface for configuration and monitoring of all detector subsystem front-end boards (e.g. ASICs and other digitizing electronics).

We have identified an ideal candidate for the DAM hardware. An updated version of the FELIX board [5] (Model FLX155) is currently being produced at BNL for ATLAS at the HL-LHC. Its features are substantial and the updated components ensure a longevity of production, performance and support that match very well with the EIC timeline. The board is built around the Xilinx Versal ACAP. This will facilitate using the board both as a PCIe device (supporting both PCIe Gen4 and Gen5 standards) in a server or as a standalone "smart" "aggregation" switch running a Linux OS. It can support up to 48 serial links to RDOs at the front-end running at speeds up to 25 Gbps as well as an LTI interface (8 fibers) supporting a high-resolution direct clock along with our GTU-DAM communication protocol. There is also a separate 100 Gb ethernet link off the board. A DDR4 RAM slot is available to support buffering and more complex algorithms for data reduction or interaction tagging. The board supports JTAG and I2C communications.

We expect to procure several FLX155 boards for testing and software/firmware development in 2025.

3.5 GTU - Global Timing Unit

The design of the global timing distribution system (GTU) will be central to the operation of the streaming readout model. The timing system must provide signals to ensure that the data from different detectors can be synchronously aggregated. It must provide a copy of the accelerator bunch crossing clock (running at 98.5Mhz) to all front-end systems. A subset of these systems (e.g. TOF) will require a phase aligned system clock with a jitter of <5 ps in order realize required timing resolutions for these detectors (20-30 ps).

The GTU is also the only source of real time information provided to the FEB/RDOs, so it must provide information a trigger system would normally provide. This information must be sufficient to synchronize data from different detectors, to send flow control signals, to pass bunch information such as spin orientations and bunch structure, to provide synchronous user defined signals for signaling special data formatting or calibration needs, and to implement a firmware and hardware triggers for debugging, calibration or fallback to solve unforeseen readout issues.

Figure 24 shows a schematic layout based on required functionality of the GTU. The physical concept is shown in figure 25. The GTU will be custom rack-mounted hardware in the DAQ room with a base board and multiple plug-in optical interface modules. It will be based on a multi-FPGA architecture including a single Zync SoC FPGA supporting gigabit ethernet and a full Linux OS to facilitate both ePIC Run Control and other user-based applications. It will include an interface for the EIC Common platform (Clock, beam orbit and other collider information) and an interface for feedback from the local IP-6 beamline to support bunch crossing clock phase corrections

The jitter-cleaned and phase corrected clock then is fanned out for distribution to all DAM boards via a multi-fiber communications link (We intend to support up to 150 of these links for current needs as well as potential future requirements). In addition we plan to support up to 250 direct clock links to the RDO/FEB electronics. This is to mitigate potential limitations with the distribution of the low jitter (<5 ps) clock via the DAM path communication protocol.

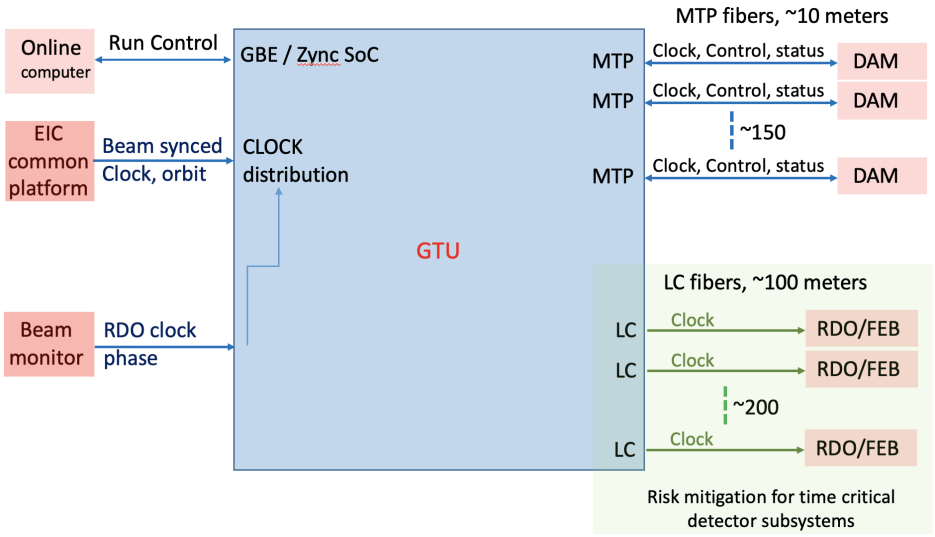

Fig. 24 Schematic layout based for the GTU

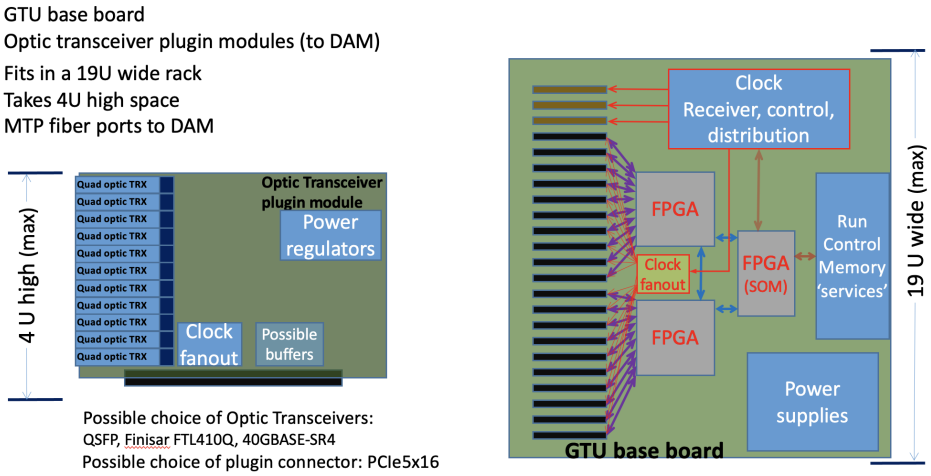

Fig. 25 Physical concept for the fiber distribution for the GTU

Decoded Synchronous Command Structure							
[0:7]	[8:15]	[16:23]	[24:31]	[32:39]	[40:47]	[48:55]	[56:64]
Flexible Command Data Encoding					FAST CMD		Comma
type	type specific				FAST CMD		Comma

Table 4 DAM/RDO Decoded Synchronous Command Structure. This structure is defined to allow continuous availability of the critical beam related bits and more rare commands. The data in the 40 bits worth of flexible command data encoding remains flexible but must contain enough control bits to select what structure it has. The "type", "type specific" division is an potential holding this flexibility

3.6 Protocols

The ePIC fiber protocol is used to communicate information between the GTU, DAM and RDO boards. The DAM to RDO communications are limited by the type of interface, and can be described in three categories as shown in table 5.

The ePIC fiber protocol depends upon a synchronous command structure (table 4 which simultaneously encodes fast commands, to be delivered to the RDO or ASICs with fixed latency relative to the bunch crossing and control information such as the current bunch crossing. The RDO acts upon delivered synchronous

type	clock (MHz)	downlink rate (Gb/s)	downlink word length (ns)	downlink word width (bits)
FPGA Standard	98.5	10	10.15	64
FPGA VTRX+	98.5	2.56	10.15	16
lpGBT VTRX+	39.4	2.56	25.375	64

Table 5 RDO downlink words

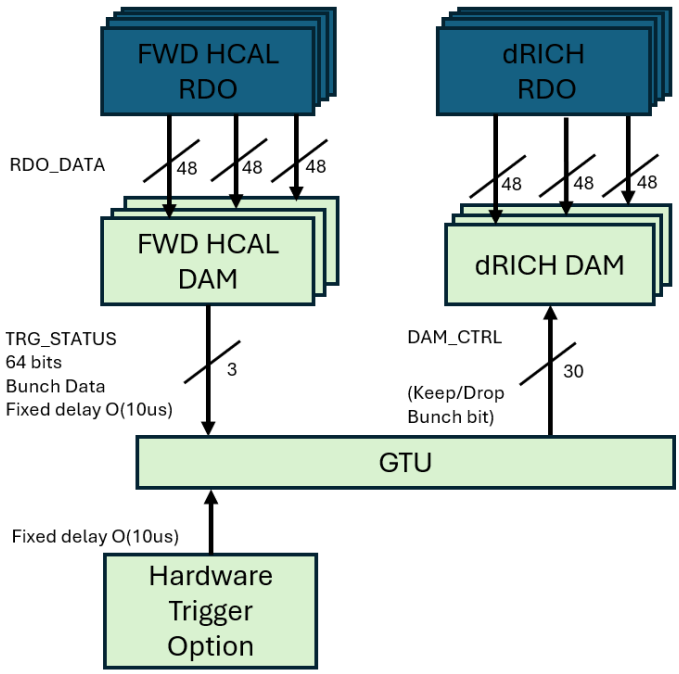

Fig. 26 Operation of firmware trigger under assumption that the trigger decision for the dRICH depends upon data from fHCAL

commands to provide headers defining the time frames, and to implement required features. The lpGBT provides a transparent fiber interface to the ASICs and does not have features capable of implementing the full ePIC DAQ protocol, so this functionality must be provided later in the chain, either in a second layer fiber to fiber RDO, or in the DAM board itself.

The maximum timeframe length, in bunch crossings will be defined to fit within 2^{16}, which implies a time frame length of ≈0.6 ms. This is also a convenient time as it corresponds to a manageable maximum time frame size of ≈10 MB. The need to support both the 10.15 ns EIC clock and the synchronized 25.375 ns clock support by cern lpGBT and CERN developed ASICs demands that time frame lengths be limited to multiples of 5 EIC clocks, if the time frame's are to be synchronized in time.

The features encoded in the Synchronous command protocol are

- Synchronize bunch counters among all detector readouts
- Define the time frame boundaries
- Provide RDO and DAM Data processing flags
- Configure ASICs and RDOs
- Firmware based triggering
- Flow control
- Transfer Data
- Transfer Slow Controls Data

3.6.1 Firmware Trigger

One example of the operation of the protocol is in the firmware trigger to be implemented to reduce dRICH noise. It's important to note that the the firmware trigger under discussion is not (or not necessarily) a global trigger that would remove full events from the readout of the ePIC detector. Instead, this trigger is expected to affect only the data from particular detectors with unusually high data volumes. In this example, the dRICH.

The path of the commands sent is show in figure 26. Data arrives at DAM boards with 10us from digitization. It is stored in the DAM boards. After 10us FPGA based algorithms provide a description of the data (for example number of hits above a specified threshold) from each fHCAL DAM board. This information is encoded into 64 bits and sent to the GTU which aggregates data from fHCAL DAM boards and sends the keep/drop bunch bit to the dRICH DAM boards. The dRICH DAM boards drop or transmit data based upon this message. The decision comes after a fixed latency of about 11us which is very small compared to the buffering available on the DAM board.

Note that a similar approach can be implemented with a hardware signal into the GTU. In this case a fixed delay is applied to the hardware signal, but the decision mechanism uses the same data path.

3.6.2 dRICH data algorithms

There are also additional schemes for implementing dRICH data reduction using only dRICH data or aggregated data from different sub-detectors. This is currently under investigation by the dRICH groups at INFN. One possibility would be to perform such reduction on the network of interconnected dRICH DAMS using the APEIRON framework [6] which implements a multi FPGA ML algorithm with deterministic time. The results of this calculation are transmitted to the GTU in the same manner as in the previous firmware trigger. The DAM buffering capacity is exploited in this scheme. Another possibility is to use instead, Online Data Filter algorithms in the servers receiving the aggregated data (see Fig. 5), exploiting xPU resources. The fact that the noise rate in the dRICH will increase with the radiation damage will provide an opportunity to develop and carefully test such systems

3.7 DAQ/Online Computing - Echelon 0

Resource	Totals
DAM/FELIX boards	136
EBDC Servers	92
DAQ Compute Nodes	108
File Servers (Buffer Box)	6

Table 6 DAQ Computing Resources

Table 6 outlines the planned resources for the ePIC detector DAQ and Online computing needs. This is based on the elements shown in the DAQ schematic in Figure 5. Several thousand fibers from the RDOs will be aggregated in the DAM boards and presented to the Online Farm. To be clear each online farm node represents one multi-core server. The expectation is that they will minimally support 32-64 cores, and selected nodes will support PCIe-based GPUs and/or FPGAs in addition to the DAM boards in the FBDC (Frame Building Data Concentrator) nodes. The high performance DAQ network is expected to support 100/400 Gbps bandwidth connections. As the majority of the Online computing is expected to be COTS hardware, much of it will be acquired as late as is reasonable in the construction phase.

All Echelon 0 resources are fully dedicated to operation of the ePIC Detector and are included as part of the EIC Project. One open question under consideration, however, is to split these resources between the DAQ Room at IP-6 and the SDCC (BNL main data center) and to integrate them as a single enclave under ePIC control. There are several advantages to this configuration. First it will reduce the overall cost of infrastructure upgrades to the DAQ Room cooling systems. Also, having a subset of ePIC computing resources available in the SDCC will allow better network access to DAQ and electronics labs during construction (when the DAQ Room will not be available. Finally, during operations having DAQ tiered storage of production data in the SDCC will facilitate distribution of that data to both Echelon 1 processing sites (BNL and JLAB).

At the DAM stage the aggregated data streams will have substantial buffering and available network bandwidth for online processing that will be primarily focused on event identification and background/noise reduction. While we do not currently have solid estimates on the necessary computing resources to complete the required tasks, we have tried to provide conservative estimates of computing resources that would allow a full reconstruction of a 500 kHz trigger rate of events from similar scale detectors that exist now (e.g. GlueX and CLAS12 at Jefferson Lab and sPHENIX at RHIC). More likely the necessary computing resources for online filtering to get the expected data rates of O(100 Gbps) to files will be somewhat smaller.

3.7.1 Time Frame Building

In the streaming model, the primary consideration is ensuring that enough bandwidth and buffering will be available to handle the digitized data at each stage of the DAQ. At the front-end stage time frames for the individual streams are created, managed and aggregated. Given current background and noise estimates the planned bandwidth off the detector to the DAM boards O(10 Tbps) should be more than sufficient.

Streams at the DAM boards will support time frames using a 16 bit bunch crossing counter which would represent a configurable time window of up to 65536*10.15 ns = 665 s. Although the front-end DAQ will be synchronized using a single common clock from the EIC, not all ASICS/digitizers at the FEBs will be running at the same frequency. Hence the timestamps coming from hits in different detectors will need to be wrapped in smaller "time slices" within the full time frame to establish an absolute time for each hit.

Time frames buffered at the DAM boards will be able to utilize the online farm to complete a full build of complete time frames with data from all detectors. Effectively N streams from the DAM boards will generate M<N streams of time frames containing the time frame fragments from the N original streams. This will greatly facilitate additional event identification and processing at both the Echelon 0 and Echelon 1 stages.

3.7.2 Data Processing

The ePIC readout system must support data reduction techniques. The implementation of firmware based triggering has already been described, but there are many additional techniques that might be implemented in echelon 0. These include zero loss techniques like aggregation of headers from ASICs or DAM board data. It could include standard or ML based compression techniques. It could involve analysis techniques such as cluster finding or track reconstruction. There could also be ML based noise reduction techniques. And there could be analysis done for specific purposes such as the creation of scalers for monitoring or collider feedback.

The framework for the code generating these features must allow the code to be shared with the offline software, for operational transparency, and for algorithm evaluation.

The results of the code must be incorporated into the time frame data using data formats that allow for independent data banks to co-exist. The policy of ePIC is expected to be to avoid dropping any data unless data volumes make it necessary. There should also be a sample of unprocessed data even if the readout of raw data banks are suppressed due to data volume limits. This implies that the write out of specific data banks be controlled by configurable prescales.

3.7.3 Configuration Databases

Configuration information must be stored and made accessible to the ePIC Collaboration.

3.7.4 Slow controls interface to RDOs/FEBs

The primary configuration and slow control communications interface to all the ASICs and other digitizing electronics (FEBs) will be through our proprietary data link between the DAM board and the RDOs. Our current plan is to take advantage of the Versal SoC FPGA dual-core ARM CorteX processor. ALL DAM boards will support a full LinuxOS and gigabit ethernet access. This will facilitate running an EPICS soft IOC as well as user-based server applications for local and remote communication with the front-end electronics.

Slow control communication on the DAM-RDO link must be bidirectional which means that slow control communications must share the link with streaming data coming from the detectors. The protocol must ensure that adequate bandwidth is available for digitized hits from the detector and slow controls readouts. The flow control provisions must enforce this requirement.

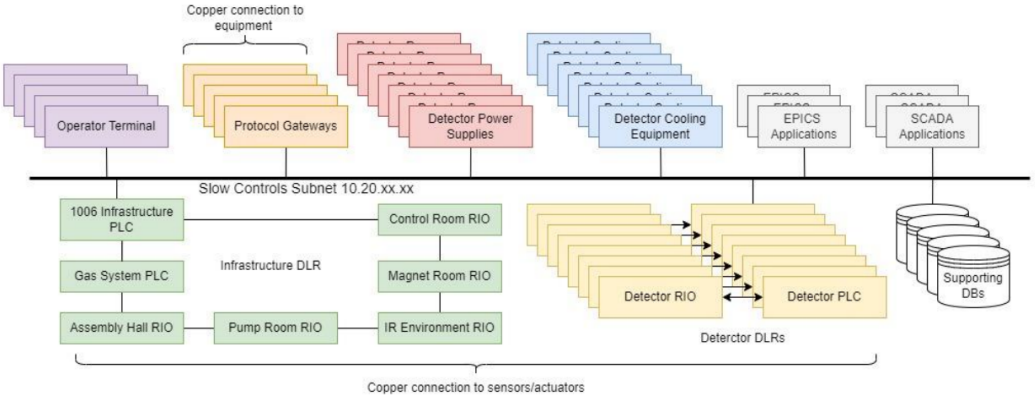

Fig. 27 Proposed ePIC slow controls network topology

Software and firmware development of drivers and libraries necessary to access all the FEB "flavors" is supported as part of the Project. The majority of the FEBs will support standard I2C control communications.

3.7.5 Monitoring / Logging

A unified system for centralized logging of informational and error messages is required. These messages should be ideally be available and archived in web-accessible form.

A unified system for monitoring of the real time behaviour and utilization of online components is also needed.

3.7.6 Interface to Echelon 1

As discussed in Section X (computing), the ePIC DAQ (Echelon 0) is an integral part of the computing system, and the output of the DAQ data triggers the calibration and reconstruction pipeline in Echelon 1, located at the computing centers of the host labs. From the DAQ buffering disks, two identical copies will be sent to the buffer file system at the BNL SDCC via a dedicated fiber link and at the JLab Data Center via the 400 Gbps ESnet link, respectively. Each data center's data buffer has the capability of about three weeks' ePIC data taking to allow for multiple iterations of calibration jobs and reconstruction passes. Data will also be copied to permanent archival storage (presumably HPSS-like tape system), one copy at each site, which allows for reprocessing of the data in the future in case a problem identified in the prompt reconstruction pass or an improved reconstruction becomes available in the future. Nevertheless, in a steady state, the prompt calibration and production are expected to make the final analysis-ready data for physics working groups within days of the data taking, significantly expedited compared to many ongoing Nuclear Physics experiments.

3.8 Slow Controls

There will be a myriad of slow controls information associated with both the EIC collider and the ePIC detector. These include various systems associated with the beamline, magnets, detector biases, gas flows, temperatures, pressures, etc... While the design and implementation of these slow control systems will be driven by the relevant subsystems they are associated with, it is the defined responsibility of the DAQ to provide software tools to facilitate the integration of all this information with the streaming physics data. This will include synchronizing the times associated with readout of slow control systems and the bunch-crossing clock that will be driving the DAQ system. Online slow control databases to support calibration and reconstruction processing will also be developed. Finally, a general network infrastructure in the experimental hall and control room, independent of the high performance DAQ network, will be provided to support integration of all slow control systems

Scenario	Yearly Database Storage (TB)	Network Traffic (Mbps)
estimated	53.9	22.8
worst case	173.5	73.4

Table 7 Slow Controls data volume and network traffic

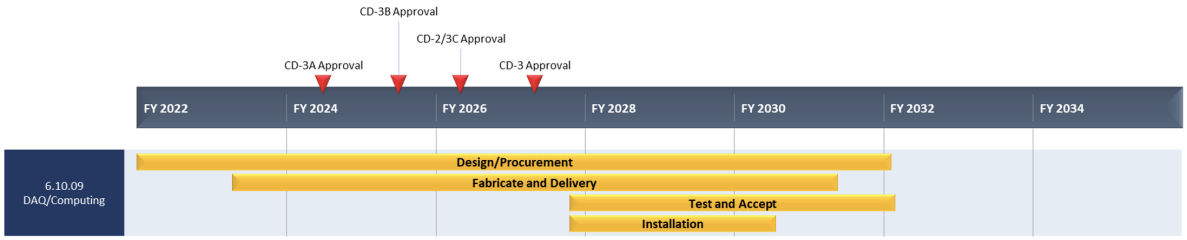

Fig. 28 DAQ/Computing schedule

A schematic of the proposed slow controls network topology is shown in figure 27. The implementation uses EPICS 7 on an ethernet network to control detector operation and read and archive conditions information. Allen-Bradley PLCs are to be used for controlling power to racks in the IR and for detector interlocks.

Resource requirements for the slow controls system were obtained by surveying detector managers. These resulted in approximately 500,000 channels to be read and stored. The yearly storage estimates and network traffic estimates are show in table 7.

4 Calibration, alignment and monitoring:

During run time, predetermined calibration and alignment will be used in configuring the readout electronics and data reduction computing tasks. These calibration and alignment are managed by detector groups, extracted from dedicated prior-to-beam calibration runs, such as pedestal runs and zero field runs. When necessary, such as changes in detector condition, new calibration will be extracted and updated to be used in data taking. The calibration constant used will be archived in the run database and made available for reference in the offline analysis.

Constant monitoring for detector status and data pipeline healthiness is key to high-efficiency data taking and a successful run. We expect a multi-level of monitoring that includes monitoring the metrics on (1) detector statues (2) each stage of the data pipeline (3) sampled data content for decoding and analysis. In addition, in the Echelon-1 computing facility, full reconstruction will be performed for a small fraction of time frames expediently to provide holistic feedback of the experiment capability down to analysis level observable such as pi0 and K0s.

5 Status and remaining design effort:

- R&D effort: ASIC R&D to continue through 2025
- E&D status and outlook: The bulk of the engineering design efforts still required for the readout electronics are centered around the development of RDO and FEB designs needed to support all the detector subsystems. This information is needed to establish baseline costs and better define construction and testing schedules. Project Engineering design for a GTU engineering article can be completed prior to CD2/3. Finally, we expect to procure several FLX155 engineering articles in 2025 to support further timing and communication protocol testing and initial firmware development.
- Status of maturity of the subsystem: Electronics and DAQ held a second PDR in June 2024. We expect to hold a third PDR in 2025 on track to an FDR in 2026. There are CD-3B items in the Electronics for VTRX+ and lpGBT. The FDR was held in June 2024, and will be presented during the CD-3B review in January 2025.

Detector System		Channels	SensorTechnology	Redout Technology	Institution
Si Tracking					
	3 vertex layers	7 m^2	MAPS	lpGBT, VTRX+	STFC, UK, ORNL
	2 sagitta layers	368 pixels	MAPS	lpGBT, VTRX+	STFC, UK, ORNL
	5 backward disks	5,200 MAPS sensors	MAPS	lpGBT, VTRX+	STFC, UK, ORNL
	5 forward disks		MAPS	lpGBT, VTRX+	STFC, UK, ORNL
MPGD Tracking					
	Barrel, e & H Endcaps	202 k	uRWELL, MicroMegas	SALSA	CEA, OMEGA, JLab
Forward Calorimeters					
	LFHCAL	63,280	SiPM	CALOROC	ORNL, Debrecen
	HCAL Insert	8 k	SiPM	CALOROC	ORNL, Debrecen
	pECAL W/SciFi	16,000	SiPM	Discrete	IU
Barrel Calorimeters					
	HCAL	7,680	SiPM	CALOROC	ORNL, Debrecen
	ECAL SciFi/Pb	5,760	SiPM	CALOROC	U Regina, ORNL
	ECAL Imaging Si ASTROPIX	500 M pixels	Astropix	Astropix	KIT,NASA (GSFC), ANL
Backward Calorimeters					
	nHCAL	3,256	SiPM	CALOROC	ORNL
	ECAL (PWO)	2,852	SiPM	Discrete	IU, EEEMCAL Consortium
Far Forward					
	B0: 3 Crystal Calorimeter	135	SiPM/APD	Discrete	IU, JLab
	B0: 4 AC-LGAD layers	688,128	AC-LGAD Pixel	EICROC	IJCLab, OMEGA, BNL, ORNL, Rice
	2 Roman Pots (RP)	524,288	AC-LGAD Pixel	EICROC	IJCLab, OMEGA, BNL, ORNL, Rice
	2 Off Momentum (OMD)	294,912	AC-LGAD Pixel	EICROC	IJCLab, OMEGA, BNL, ORNL, Rice
	ZDC: Crystal Calorimeter	900	SiPM/APD	Discrete	IU, JLab
	ZDC: HCAL	9,216	SiPM	CALOROC	ORNL, Debrecen, JLab
Far Backward					
	Low Q Tagger 1	33,030,144	Timepix4	Timepix4	U. Glasgow
	Low Q Tagger 2	33,030,144	Timepix4	Timepix4	U. Glasgow
	Low Q Tagger 1+2 Cal	420 (2x210)	SiPM	CALOROC	U. York
	2 Lumi PS Calorimeter	3,360 (2x1680)	SiPM	Discrete	U. York
	2 Lumi PS Tracker	128,000 (2x64,000)	AC-LGAD Strip	FCFD/EICROCx	FNAL, OMEGA, Hiroshima, NTU, ORNL, UIC, UH, Rice, KSU, Tokyo
	Lumi Direct Photon Calorimeter	100	SiPM	Flash250	AGH Krakow, JLab
PID-TOF					
	Barrel bTOF	2,359,296	AC-LGAD Strip	FCFD/EICROCx	FNAL, OMEGA, Hiroshima, NTU, ORNL, UIC, Rice, BNL, KSU, Tokyo
	Hadron Endcap fTOF	3,719,168	AC-LGAD Pixel	EICROC	IJCLab, OMEGA, BNL, ORNL, Rice
PID-Cherenkov					
	dRICH	317,952	SiPM	ALCOR, VTRX+	INFN (BO, FE, TO)
	pfRICH	69,632	HRPPD	FCFD/EICROCx	BNL, FNAL, JLab
	hpDIRC	73,728	MCP-PMT or HRPPD	FCFD/EICROCx	BNL, FNAL, JLab

Fig. 29 Electronics and DAQ Resources

6 Construction and assembly planning:

Figure 28 shows the current project schedule for DAQ/Computing. It is broken down into four general categories: Design/Procurement, Fabricate and Delivery, Test and Accept and Installation. Early in the construction phase there is a heavy focus on building and testing custom hardware (GTU, DAMs, RDOs) in order to facilitate detector subsystem testing and DAQ firmware/software development.

Once IP-6 infrastucture upgrades have been completed (DAQ and Control rooms, Wide Angle Hall), we can begin the main trunk fiber pulls into the hall and tunnels and install required patch panels and terminate fibers. At this time we can also start installation of the general IP-6 network infrastructure in the Hall, DAQ and Control Rooms.

Computing hardware procurement and installation are scheduled in three phases during the course of construction. Phase I at the beginning of construction will be for a small subset of machines for development and evaluation. They will be placed in both the DAQ/Electroncs development labs as well as in the SDCC. Phase II will be primarily in the DAQ Room as part of the DAQ subsystem installations and will provide the opportunity for full chain large scale testing of the DAQ as well as for detector subsystems as they begin to be installed at IP-6. Finally Phase III will be implemented at the end of the full ePIC detector installation as we have a better understanding of the required resources needed for inital Physics operation. This hardware will be installed at both the DAQ Room and in the SDCC which will define the full Echelon 0 enclave.

7 Collaborators and their role, resources and workforce:

The institutions specifically developing the readout electronics and ASICs are listed under the electronics section. Figure 29 lists the institutions which have expressed interest in participating in the design of various other parts of the readout chain. Formal agreements committing engineering and technical personnel have not been officiated.

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