Report of the

Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics

Performed at Jefferson Lab (Remotely)
Newport News, Virginia

June 10-11, 2024

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1. Executive Summary

The committee would like to thank the ePIC community for preparing the material for the review. Each contribution addressed concisely the charge questions and allowed the committee to make a well-informed assessment.

The committee finds that the development of electronics and data acquisition for ePIC is well advanced for this stage of the project. There has been significant progress in the architectural design and prototype development. Performance requirements, documentation, scheduling, and ES&H/QA plans are well defined in many sub-systems, and the strategies for achieving a global system maturity were clearly stated.

Although much work remains to be done, we are encouraged by the status and urge the ePIC community to move ahead in the same coherent manner, to strive for synergy and common solutions, and to benefit from the experience of the wider instrumentation community.

2. Reponses to Charge Questions

Responses to Questions

Charge Question 1:

Are the technical performance requirements appropriately defined and complete for this stage of the project?

Yes. The teams are working towards well-defined specifications of the front-end ASICs for processing the detector signals. The requirements for ReadOut/DAQ/controls are less mature but acceptable for this stage of the project. The remaining steps to bring these to maturity appear to be well defined.

Comments

- We applaud the adaptation of the readout architectures to match detector environment specs, in particular for the dRICH where steps to mitigate the high DCR will be implemented in the ASIC together with other handles such as triggering within the DAM.
- We appreciate these steps towards robustness. However, it would be reassuring to see simulations or measurements to demonstrate the effectiveness of the shuttering mechanism for dRICH.
- The RO/DAQ architecture is evolving in the right direction, but some specifications are yet to be fully defined and this should now move ahead at speed to allow implementation (RDOs in particular) to start.
- We feel that a dedicated overview and discussion on the slow-controls would have been helpful for the review, in particular from the point-of-view of hardware/firmware.

Recommendations

1) Rationalize the dRICH readout with the benefit of simulation/measurement to reassure

the community of the benefit of the shutter implementation.

2) We recommend to include a dedicated overview and discussion on the slow-controls in a subsequent review.
3) To achieve the next level of maturity of the RO/DAQ architecture and based on the experience of recent experiment upgrades, we recommend the following steps:
    - Fix the definition of protocol between DAM and RDO.
    - The general architecture of the command (and trigger) distribution from GTU to DAMs/RODs must be developed and specified further.
    - The trigger (foreseen as a mitigation of excessive data volume) is not yet mature and may introduce as yet unforeseen complications. This should be developed.
    - Define the performance requirements of DAQ systems at different stages of the development.
    - Define the DAQ/control requirements from sub-detectors from the perspective of testing and validation. This was an important step during the evolution of the recent upgrades at the LHC.
    - If many variants of RDO and or DAMs are indeed required, the division of responsibilities should be discussed and clarified. Central support must be properly resourced. This was massively underestimated in recent LHC upgrades.
    - Plans to evaluate techniques to reduce data volume should be developed in data challenges, as they might have large impact on the data rate and performance of the DAQ system.
    - A table showing how many DAM boards and readout server are assigned to each detector should be provided for completeness.
    - Dataflow from the FEE to the STORAGE must be better described.

Charge Question 2:

Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project)?

Yes. The ASIC documentation is mostly mature and complete. The RO/DAQ documentation/plans are less mature but appropriate for this stage of the project. The completion of these is on the right track and the remaining steps are being formulated.

Comments

- We encourage the pursuit of synergy and encourage further steps in this direction in the RDO developments. This can only help with the documentation and definition of interfaces.

Recommendations

1) In particular for the ASICs, the reviewing procedures must be carefully planned and inserted appropriately into the planning. Key dates must be chosen to allow realistic reviewing and time for revision if recommended as an outcome of the reviews.
2) The full specification for the FCFD architecture was not presented. It was stated this will largely follow the previous ETROC ASIC for CMS, but this must be clearly documented for the ePIC framework.

3) Documentation of interfacing between RDOs and DAMs should be finalized, from the perspective of both DAQ and controls.

Charge Question 3:

Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?

Yes. However, for the ASICs, the remaining development steps must be concluded and reviewed carefully. That being said, all results from prototyping are encouraging and show progress everywhere. For RO/DAQ, risk has been minimized by the choice of FELIX as the DAM implementation. Similarly, the RDO architecture and synergy across sub-systems will help to minimize risk.

Comments

- There was little information on the MAPS system/implementation, and hence no comments are possible. Given that there is a strong physical overlap between sensor and electronics, we suggest the inclusion of more information on the tracker in the next review.
- We appreciate the move towards digital-on-top design for the EICROC and CALOROC designs.
- For the EICROC/CALOROC designs, there is a worry that human resources for digital design may be limited in the key institutes. This must be monitored closely. Can collaborative help be identified and injected in a strategic manner to enhance the likelihood of success?

Recommendations

1) For the ASICs, all remaining steps towards the conclusion of development must be clearly defined and progress monitored. This was a clear lesson from recent experience in the LHC projects.
2) One point of worry is the packaging strategy for the ALCOR ASIC and the corresponding in power (and signal?)-routing. Has this been extracted and simulated carefully to enhance confidence in the V3 design? And is there a clear route to successful flip-chip packaging, either through a vendor or a collaborating institute? Maximal effort must be dedicated to resolve this as it is a deviation away from the power/signal/packaging concepts used through the successful prototyping steps.
3) For the CALOROC and SALSA, it was unclear how the 40/50 MHz sampling would translate into the 100MHz BX regime and the time-tagging of the hits. This should be clarified and documented.

Charge Question 4:

Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?

Yes. However, there is little room for margin in the ASIC scheduling. The RO/DAQ

components (HW, FW, SW) are more comfortable, but should not be allowed to slip. So, we strongly encourage finalizing all interface definitions (protocols) as soon as possible.

Comments

- We suggest that the plan for a triggered RO be rationalized coherently across the experiment. If it is to be pursued in some sub-systems, it should be worked out while considering the full readout chain (ASIC through to RDO and DAM for each sub-system implicated in the trigger) in case design modifications are required.

Recommendations

1) For the ASICs, we recommend a strong monitoring of the progress towards finalization of the designs and the decision making between options (e.g., CALOROC v1A or v1B)
2) For RO/DAQ, we recommend the outstanding protocol definitions to be fixed to allow progress, as well as the clear definition of responsibilities, synergies and sharing.
3) We strongly recommend a clearer definition from the sub-detectors of their DAQ/control needs and quantities, and how these develop in time (short-term for prototyping and long-term for scaling up of the sub-systems).

Charge Question 5:

Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

Yes. ES&H issues are correctly under consideration and included in planning. Similarly, QA steps are being folded into the planning.

Comments

- The QA steps towards ASIC production have been assessed and seem to be well under control at this stage of the process and for the ASICs discussed during this review. Similarly, QA considerations for the RDO designs have started. We assume that QA for the DAM is guaranteed by the ATLAS program.
- We advise studying the possibility to group ASIC submissions for Engineering and Production Runs (e.g., the 65nm chips). This will complicate scheduling but may help to reduce costs.

Recommendations

1) The team designing the discrete component readout (calorimeter) must rationalize their approach to radiation qualification and assurance of the COTS components.

3. Conclusion

We appreciate the great effort to prepare for this review.

We congratulate the ePIC community on the enormous progress in the electronics and data-acquisition.

We are satisfied with the answers to the charge questions provided by the contributors.

We have provided comments and made recommendations which we believe will be beneficial to the ePIC community.

4. Appendices

4.1 Appendix A: Charge to the Review Committee

Jefferson Lab
Thomas Jefferson National Accelerator Facility

MEMO

Date: 20 May 2024

To: Ken Wyllie (CERN), Mitch Newcomer (UPenn), Prashansa Mukim (BNL), Filippo Costa (CERN)

From: Rolf Ent (JLab) and Elke Aschenauer (BNL)

Subject: Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics

The scope of this review includes all aspects of the readout electronics and data acquisition design for the ePIC detector: the luminosity monitor, the backward small-angle electron tagging detectors, the Zero-Degree Calorimeter, the Roman Pots and off-momentum detectors, and the detector systems in the B0 magnet. The review may include design and fabrication choices and their cost-effectiveness, the construction schedule, considerations for safety and quality assurance, levels of redundancy, front-end electronics and interface to the data acquisition system, commissioning and calibration procedures, considerations for materials and labor, operational reliability and longevity, and any other considerations that may influence the construction, maintenance and operation of the electronics components.

Please address the following questions:

1) Are the technical performance requirements appropriately defined and complete for this stage of the project?
2) Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project?
3) Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?
4) Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?
5) Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

Please address these questions point-by-point.

You will be supplied with the project milestones extracted from the most current EIC resource loaded P6 schedule, copies of presentations relevant to this subject material, and other relevant material as part of the pre-brief material. Several aspects of the EIC detector have been reviewed previously. As part of your briefing materials, you will also be supplied with the reports from earlier reviews (e.g., on the tracking and PID systems).

cc: S. Nagaitsev
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L. Lari
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4.2 Appendix B: Review Committee

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4.3 Appendix E: Agenda

Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics

Monday June 10, 2024 - Tuesday, June 11, 2024

Click here for Zoom link (Open Session)

Day 1, Monday June 10th

Time	Talk Topic	Speaker
7:30 AM – 8:00 AM	Executive Session	Closed Sessions
8:00 AM – 8:15 AM	Introduction - An Overview of the ePIC Detector	Rolf Ent (JLab) / Elke Aschenauer (BNL)
8:20 AM – 8:40 AM	Readout System Overview	Jeff Landgraf (BNL)
8:45 AM – 9:10 AM	Electronics Implementation	Fernando Barbosa (JLab)
9:20 AM – 9:40 AM	DAQ/Computing Overview	David Abbott (JLab)
9:45 AM – 10:00 AM	Coffee Break	All
10:00 AM – 10:20 AM	Timing Implementation for the Readout Chain	William Gu (JLab)
10:25 AM – 10:40 AM	RDO - Readout Board - Pre-Production (ppRDO)	Tonko Ljubicic (Rice Univ)
10:45 AM – 11:05 AM	The EICROC ASIC for Detectors with AC-LGAD Pixels	Christophe de la Taille (OMEGA CNRS/IN2P3-Ecole Polytechnique (FR))
11:10 AM – 11:30 AM	The CALOROC ASIC for Detectors with SiPMs	Frederic Dulucq (OMEGA - Ecole Polytechnique - CNRS/IN2P3)
11:35 AM – 11:55 AM	The ALCOR ASIC for the dRICH Detector	Fabio Cossio (INFN Torino)
12:00 PM – 12:15 AM	RDO - Readout Board for the dRICH Detector	Pietro Antonioli (INFN - sezione di Bologna)
12:20 PM – 12:35 PM	Q&A	All
12:35 PM – 1:00 PM	Lunch	All
1:00 PM – 3:00 PM	Executive Session	Closed Session

Day 2, June 11th

Time	Talk Topic	Speaker
8:00 AM – 8:15 AM	Discrete Readout - Calorimeter Waveform Digitizer System	Gerard Visser (Indiana University)
8:20 AM – 8:40 AM	The FCFD ASIC for Detectors with AC-LGAD Strips	Artur Apresyan (Fermilab)
8:45 AM – 9:05 AM	The SALSA ASIC for Detectors with MPGDs	Damien Neyret (CEA Saclay IRFU/DPhN)
9:10 AM – 9:30 AM	Q&A	All
9:30 AM – 9:45 AM	Coffee Break	All
9:45 AM – 10:10 AM	Final Design Review for lpGBT/VTRX+ - Requirements	Fernando Barbosa (JLab)
10:10 AM – 10:40 AM	Final Design Review for lpGBT/VTRX+ - lpGBT/VTRX+ for MAPS	Joachim Schambach (ORNL)
10:40 AM – 11:05 AM	Final Design Review for lpGBT/VTRX+ - VTRX+ for dRICH	Pietro Antonioli (INFN - sezione di Bologna)
11:05 AM – 11: 20 AM	Final Design Review for lpGBT/VTRX+ - Q&A	All
11:20 AM – 2:00 PM	Executive Session	Closed Session
2:00 PM – 2:30 PM	Closeout	All