EIC-AncBrain

A Slow Control and Communication Management System of AncASIC

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Contents

1. Introduction

This document provides a comprehensive overview of the AncASIC (Ancillary ASIC). The AncASIC performs the following key functions:

- **Internal Sub-Module Control:** Manages the operation of internal sub-modules, including the Negative Bias Voltage Generator (NBVG) and Shunt LDOs, through dedicated control interfaces and registers.
- **Communication Bridging:** Facilitates communication between the lpGBT (Low Power GigaBitTransceiver) and the LAS (Large Area Sensors) by interpreting commands, handling data flow, and managing protocols.
- **System Stability:** Ensures system reliability through robust error handling mechanisms and a watchdog timer to monitor system health and respond to potential failures.

2. System Overview

The AncASIC is part of a larger system consisting of the following components:

- **lpGBT (Low Power GigaBit Transceiver) Interface:** Upon receiving a command from the control room, it initiates communication and sends control commands to the AncASIC modules via a serial interface. There are 16 e-links @80 Mbps and 24 e-links @160 Mbps/320 Mbps. **One** e-link provides slow control to a group of up to **four** EIC-LAS where each slow control e-link has **3 signals**: Clock *SCL*, *SC_in*, *SC_out*
    - ***SC_In*:** Serial differential data line for transmitting commands and data to the AncASICs.
    - ***SC_Out***: Serial differential data line for receiving responses and status information from the AncASICs.
    - ***SCL*:** Clock signal line (differential) operating at **Global Clock (not defined yet)**, providing the timing reference for serial communication.
- **AncASIC Modules:** Several AncASIC modules (assuming 4; **not defined yet**; based on number of LAS to be connected) are connected in a daisy chain configuration. Each module contains a Negative Bias Voltage Generator and Shunt LDOs. It independently processes received commands and controls internal sub-modules.
- **LAS Interface:** Operates on specific communication protocols and functionalities. Receives commands and data from the AncASIC. There are dedicated lines for
    - Clock Signal (*GCLK*),
    - Global Reset (*GRESET*),
    - Synchronization Signal (*SYNC*), and
    - Slow Control Interfaces (*SC_SRV* and *SC_CORE*).

  All lines are differential and derived from AncASIC based on the command from lpGBT.

3. AncASIC Module Functionality

3.1 Sub-Module Control

(will be completed further upon receiving information from the collaborators)

The AncASIC houses and controls two primary sub-modules:

- **Negative Bias Voltage Generator (NBVG):**
  - Generates a negative voltage from a positive supply.
  - Offers different levels of configurable bias voltages.
  - Enables zero-volt output in single-supply systems.
  - **Components:** Charge Pump, DAC, Control Register, Oscillator, Bandgap Reference.
- **Shunt LDOs:**
  - Provides stable and regulated output voltage independent of input voltage fluctuations.
  - Offers configurable output current limits.
  - Includes enable/disable control for individual LDOs.
  - **Components:** Voltage Reference, Pass Transistor, Control Register, Monitoring Circuits.

3.2 Communication Interface:

The AncASIC manages communication with both the lpGBT and LAS through distinct interfaces:

3.2.1 lpGBT Interface:

- **Physical Layer:**
  - Employs the *SC_In* and *SC_Out* lines for half-duplex, bidirectional communication at **Global Clock (not defined yet)**.
  - Operates with a serial protocol synchronized by the *SCL* clock signal.
  - Each AncASIC module analyzes the received address information to determine if the transaction is intended for itself. Only the addressed module responds; others discard the transaction.
  - Responses and status information are sent back to lpGBT via the *SC_Out* line using the same protocol and clocking scheme.
- **Protocol:**
  - Adheres to a specific message format consisting of:
    - **Start of Frame (2 bits):** Predefined pattern ("*01*") signaling the beginning of a transaction.
    - **Module Address (3 bits):** Identifies the target AncASIC module within the daisy chain (0-3). **001 - 100:** AncASIC module addresses 1 to 4.
    - **Data Type (2 bits):** Defines the purpose and format of the 40-bit data payload (see
    - **Table 2**).
    - **40-bit Data Frame:** Structure varies based on the Data Type.

        - **Frame Checksum (CRC) (16 bits):** 16-bit CRC for error detection.
        - **End of Frame (2 bits):** Predefined pattern ("*01*") signaling the end of a transaction.
- **Data Type Interpretation:**
    - The "*Data Type*" field determines how the AncASIC interprets the 40-bit data payload:
        - **00 (Internal):** Data is intended for configuring or controlling internal AncASIC sub-modules (NBVG or Shunt LDOs).
        - **01 (LAS Service Management):** Data is meant for the LAS Service Management interface.
        - **10 (LAS Core Management):** Data is intended for the LAS Core Management interface.
        - **11 :** Reserved Bits.

3.2.2 LAS Interface:

- **Physical Layer:**
    - Employs a dedicated serial interface operating at 5 Mbps.
    - Utilizes Manchester encoding and decoding for reliable data transmission.
- **Protocol:**
    - Adheres to the LAS protocol specifications ***(REQ01-1-1 to REQ01-4-1)*** for data frame format and functionality.
    - Handles WRITE_posted, WRITE_non-posted, and READ transactions, interpreting the "*R/W*" field within the 40-bit LAS data frame to determine the operation type and manage responses accordingly.
- **Response Handling:**
    - AncASIC buffers responses from the LAS before forwarding them to the lpGBT via the *SC_Out* transceiver.
    - Manchester decoding is performed on the received LAS responses before adding the address and other overhead for transmission to the lpGBT.

3.2.3 GCLK Interface:

- The AncASIC directly routes the Global Clock (**not defined yet**) SCL clock signal to the LAS as GCLK for synchronization purposes.

3.3 Broadcast Signal Generation:

To optimize efficiency and synchronization, the AncASIC uses a dedicated bit within the expanded "Module Address" field to indicate broadcast signals and implements a digital delay line mechanism.

3.3.1 Broadcast Indentification:

The following patterns are used:

- **001 - 100:** AncASIC module addresses 1 to 4.
- **000:** Global Reset broadcast command.
- **111:** Global Sync broadcast command.

3.3.2 Broadcast Detection:

- The Address Comparator detects the reserved patterns (000 and 111) and generates a ***broadcast_command*** signal. This signal indicates that a

broadcast command has been received, regardless of the specific AncASIC module address.

3.3.3 Delay Line Configuration:

- Each AncASIC has a configurable digital delay line, implemented using synchronous counters/shift registers, clocked by a high-frequency clock derived from *SCL* (**Global Clock**).
- The lpGBT sends configuration transactions to set the delay value for each AncASIC based on its position in the daisy chain. This compensates for the propagation delay between modules.
- The delay value for each AncASIC is stored in a dedicated register.

3.3.4 Register Storage:

- The register storing the delay value for each AncASIC is part of the internal register map and can be accessed using "Internal" data type transactions. The specific register address and bit width for the delay value will be defined in the register map section of this document.

3.4 Error Handling, Watchdog and Temperature Protection:

The AncASIC implements a robust error-handling mechanism using a centralized error-handling block and a dedicated temperature monitoring system:

3.4.1 Centralized Error Handling Block:

- This block receives error flags from various parts of the design, including communication interfaces, sub-modules, and the watchdog timer.
- Based on the received error flags, the block determines the appropriate error code and error source information.
- It then generates a standardized error response data frame and initiates its transmission to the lpGBT via the *SC_Out* interface.

3.4.2 Error Detection Mechanisms:

- **Transmission Errors:** Parity/CRC checks are implemented on received data to detect transmission errors in communication with the lpGBT and LAS.
- **Protocol Violations:** To ensure protocol compliance, the AncASIC checks for invalid transaction types, incorrect addressing, and timing violations.
- **Response Timeouts:** A timeout mechanism monitors for timely responses from the LAS and triggers an error if a response is not received within the specified period.
- **Sub-module Errors:** The NBVG and Shunt LDOs have internal monitoring circuits to detect overcurrent and over-temperature conditions (NBVG) or out-of-regulation conditions (Shunt LDOs).
- **Watchdog Timer Timeout:** The watchdog timer monitors system health and triggers an error if not periodically reset by the AncASIC logic.
- **Temperature Monitoring:** A dedicated temperature sensor continuously monitors the AncASIC's die temperature. If the temperature exceeds a predefined critical threshold (***T_critical***), an over-temperature condition is detected.

3.4.3 Error Response Format:

- A standardized 40-bit data frame format is used for error responses to the lpGBT, conveying information about the type and source of the error.
- The format is as follows:

Field Name	Width (bits)	Description
HDR	4	Fixed value (4'hE) indicating an error response
Error Code	8	Specific error code (as defined in *Table 6* in the Appendix)
Error Source	8	Identifies the source of the error (e.g., AncASIC module address, LAS module address)
Reserved	19	Reserved for future use or additional error information
Parity	1	Parity bit for error detection within the error response frame

3.4.4 Error Reporting:

- Error responses are transmitted to the lpGBT via the *SC_Out* interface, providing information about the type and source of the error.

3.4.5 Temperature Monitoring and Protection:

To ensure the safe and reliable operation of the AncASIC module a dedicated temperature monitoring and protection system is integrated into the design. This system continuously monitors the AncASIC's die temprerature and triggers protective measures if the temperature exceeds a predefined critical threshold.

- **Temperature Sensor:**
  - A dedicated temperature sensor is integrated into the AncASIC die to provide accurate temperature readings.
  - The specific type of temperature sensor will be chosen based on its accuracy, range, power consumption, and compatibility with the AncASIC fabricaton process.
- **Temperature Threshold:**
  - A critical temperature threshold (***T_critical***) is defined, above which the AncASIC is considered to be operating in an over-temperature condition.
  - The value of ***T_critical*** will be determined based on factors such as the maximum operating temperature of the AncASIC components, thermal characteristics of the package, and system-level safety requirements.
- **Over-Temperature Response:** If the temperature exceeds ***T_critical***:
  - **Sub-module Disable:** The NBVG and all four Shunt LDOs are disabled.
  - **Error Reporting:** An error response (*Error Code 0x09*) is generated and transmitted to the lpGBT.
  - **Safe State Transition:** The FSM transitions to a designated safe state, potentially powering down non-essential circuitry.
- **Recovery Mechanism:**

- **Automatic Recovery:** The AncASIC automatically re-enables the sub-modules after a delay when the temperature falls below ***T_critical***.
- **lpGBT Controlled Recovery:** The AncASIC remains in the safe state until a command is received from the lpGBT to resume normal operation.

3.4.6 Watchdog Timer

- The AncASIC incorporates a watchdog timer to monitor system health and prevent lock-ups. The watchdog timer is a 16-bit counter, clocked by the system clock. It has a timeout period of 10ms (Programmable). The FSM resets the watchdog timer in the IDLE state, ensuring that the timer is periodically reset as long as the AncASIC is functioning correctly. If the watchdog timer expires, it asserts the *watchdog_timeout* signal, which triggers a system reset and also alerts the Error Handler to generate a specific error response to the lpGBT.

4. Communication Protocols

4.1 lpGBT to AncASIC:

- Utilizes *SC_In* and *SC_Out* lines with a serial protocol at **Global Clock (not defined yet)**, synchronized by the *SCL* clock.
- Employs a specific message format:

Table 1: Overall Transaction Structure

Field Name	Width (bits)	Description
Start of Frame	2	Predefined bit pattern to signal the beginning of a transaction("01")
Module Address	3	Identifies the target ANC module within the daisy chain (0-3); 000: Global Reset; 111: Global Sync
Data Type	2	00: Internal, 01: LAS Service Management, 10: LAS Core Management, 11: Reserved
40-bit Data Frame	40	Table ***2*** for details based on Data Type
Frame Checksum (CRC)	16	CRC-16 for error detection
End of Frame	2	Predefined bit pattern to signal the end of a transaction ("01")

Table 2: 40-bit Data Frame Formats

Field ID	Field Name	Width	Description
Internal	Submodule Identifier	4	Identifies the target sub-module within AncASIC(0-15 possible)
	R/W	2	Transaction type: Write or Read
	Register Address	8	Register address within the target sub-module
	Control/Data	4	Sub-module control data or internal signaling
	Parity	1	Transaction parity bit
	Stop	1	Internal signaling (or reserved)
	Unused	20	Reserved for future use
LAS(Service/Core Mgmt)	HDR	4	Fixed value (4'hA) indicating start of transaction
	R/W	2	0: WRITE_posted, 1: WRITE_non-posted, 2: READ
	EP_ADDR	8	Endpoint address
	REG_ADDR	8	Register address within the LAS module
	REG_DATA	16	Register write or read data
	Parity	1	Transaction parity bit (XOR of RW, EP_ADDR, REG_ADDR, and REG_DATA fields)

	Stop	1	Fixed value (1'b0) indicating the end of the transaction

4.2 lpGBT to LAS via AncASIC:

- AncASIC forwards the 40-bit LAS data frame from the lpGBT transaction to the LAS using Manchester encoding at **5 Mbps**.
- The LAS protocol specifications **(*REQ01-1-1 to REQ01-4-1*)** define the detailed format and functionality.

5. Clocking Scheme

- **Global Clock (*SCL*):** Used for lpGBT communication and LAS synchronization via *GCLK*.
- **5 Mbps Clock:** Generated from the **Global Clock (not defined yet)** clock using a binary counter divider (division factor depends on Global Clock). Used for AncASIC-LAS communication and internal operations.
- **Clock Domain Crossing:** Two-flop synchronizers ensure safe transitions between clock domains.
- **Watchdog Timer Clock:** Employs an independent clock source.

6. Register Map

- Each AncASIC sub-module has a dedicated register map for configuration and status monitoring (See Appendix for detail mapping).
- Specific register addresses are configured via e-fuses.

7. Alternative Power Supply

- The AncASIC incorporates an alternative power supply to ensure continued operation in case of a failure in the primary Shunt LDOs. A charge pump circuit, powered by the Global clock signal, generates a 1.2V backup supply. The Power Supply Monitor continuously monitors the output voltage of the primary Shunt LDOs. If a failure is detected, the switchover logic activates the backup supply, providing power to the NBVG and Shunt LDOs. The backup supply is designed for temporary operation until the primary supply can be restored. While operating on the backup supply, the AncASIC might experience reduced performance or limited functionality.

8. Triplication

- To enhance the AncASIC's resistance to radiation-induced errors, Triple Modular Redundancy (TMR) is applied to the FSM and other critical control logic blocks. The TMRG tool from CERN is used to automatically generate triplicated versions of these blocks. A majority voting mechanism ensures that the system continues to operate correctly even if a single-event upset (SEU) affects one of the triplicated modules. During layout,

the triplicated modules are spatially separated to minimize the probability of multiple modules being affected by a single radiation event. The effectiveness of the TMR implementation is verified through fault injection simulations.

9. Performance Considerations

- **Power Consumption:** will be analyzed and documented after implementation.
- **Response Time (LAS-AncASIC):** Programmable counter for LAS reponse timeout

10. Appendix

- Will include timing diagrams, detailed register maps, and error code definitions.

Appendix:

A.1 AncASIC Register Maps

This section details the register maps for the AncASIC sub-modules (NBVG and Shunt LDOs), defining the functionality of each register and its bit fields. Specific register addresses are configured using e-fuses during manufacturing, allowing flexibility for customization. ***The register mappings are done based on assumptions and will be refined once the individual sub modules are well defined by the collaborators.***

A.1.1 Negative Bias Voltage Generator (NBVG):

- **NBVG_CTRL (8-bit):**
  - **Address:** Determined by e-fuse configuration.
  - **Bits 7-0:** Output Voltage Setting (unsigned 8-bit value). This value sets the desired output voltage level of the NBVG. The specific voltage range and resolution will depend on the DAC implementation and design requirements.
- **NBVG_MODE (8-bit):**
  - **Address:** Determined by e-fuse configuration.
  - **Bits 1-0:** Operating Mode
    - **00:** Continuous Mode - The NBVG continuously generates the programmed output voltage.
    - **01:** Pulsed Mode - The NBVG generates the output voltage in pulses. Additional configuration may be required to define pulse parameters (e.g., duty cycle, frequency).
    - **10:** Standby Mode - The NBVG is placed in a low-power standby state.
    - **11:** Reserved
  - **Bits 7-2:** Reserved for future expansion.
- **NBVG_STATUS (8-bit):**
  - **Address:** Determined by e-fuse configuration.
  - **Bit 0:** Overcurrent Flag (1 indicates an overcurrent condition detected)
  - **Bit 1:** Over-Temperature Flag (1 indicates an over-temperature condition detected)
  - **Bits 7-2:** Reserved for future expansion.

Table 3: Negative Bias Voltage Generator (NBVG)

Register Name	Address	Bit Field	Description
NBVG_CTRL	0x00	7-0	Output Voltage Setting (unsigned 8-bit value)
NBVG_MODE	0x01	1-0	Operating Mode: (00: Continuous, 01: Pulsed, 10: Standby, 11: Reserved)

		7-2	Reserved
NBVG_STATUS	0x02	0	Overcurrent Flag (1: Overcurrent)
		1	Over-Temperature Flag (1: Over-temperature)
		7-2	Reserved

- **SLDOx_CTRL (8-bit):**
  - **Address:** Determined by e-fuse configuration (x denotes the LDO number, 1-4).
  - **Bits 5-0:** Output Current Setting (unsigned 6-bit value). This value sets the current limit for the corresponding LDO. The specific current range and resolution will depend on the design.
  - **Bit 6:** Enable (1 = Enabled, 0 = Disabled). This bit controls whether the LDO is active or in a low-power disabled state.
  - **Bit 7:** Reserved for future expansion.

- **SLDOx_STATUS (8-bit):**
  - **Address:** Determined by e-fuse configuration (x denotes the LDO number, 1-4).
  - **Bit 0:** Overcurrent Flag (1 indicates an overcurrent condition detected)
  - **Bit 1:** Out-of-Regulation Flag (1 indicates the output voltage is outside the acceptable range)
  - **Bits 7-2:** Reserved for future expansion.

Table 4: Shunt LDOs (assuming 4)

Register Name	Address	Bit Field	Description
SLDOx_CTRL	0x10 + (x-1)*4	5-0	Output Current Setting (unsigned 6-bitvalue)
		6	Enable (1: Enabled, 0: Disabled)
		7	Reserved
SLDOx_STATUS	0x11 + (x-1)*4	0	Overcurrent Flag (1: Overcurrent)
		1	Out-of-Regulation Flag (1: Out-of-regulation)
		7-2	Reserved

Note: 'x' in the SLDOx register names represents the LDO number.

A.1.3 Delay Line Configuration (8bit):

Delay Value (unsigned 8-bit value). This value sets the delay for the digital delay line in the corresponding AncASIC, used for synchronizing broadcast signals. The unit of delay (e.g., clock cycles of the high-frequency clock) and the range of configurable values will be defined based on the digital delay line implementation and the expected daisy-chain propagation delays

Table 5: Delay Line Config Bits

Register Name	Address (e-fuse)	Bit Field	Description
Delay_Config	0x20	7-0	Delay Value for Digital Delay Line (Broadcast Synchronization)

A.2 Error Code Definitions

This section defines the error codes used by the AncASIC to report various error conditions to the lpGBT. The specific encoding and transmission of error codes will be determined during implementation.

Table 6: Error Code Definitions

Error Code	Description
0x00	No Error
0x01	Parity Error (lpGBT or LAS communication)
0x02	CRC Error (lpGBT or LAS communication)
0x03	Invalid Transaction Type
0x04	Incorrect AncASIC Address
0x05	Incorrect Sub-module Identifier (Internal transactions)
0x06	Invalid Register Address
0x07	Response Timeout (LAS communication)
0x08	NBVG or Shunt LDO Overcurrent
0x09	NBVG Over-temperature
0x0A	Shunt LDO Overcurrent (For each LDO)
0x0B	Shunt LDO Out-of-Regulation (For each LDO)
0x0C	Manchester Encoding Error
0x0D	Manchester Decoding Error
0x0E	Watchdog Timer Timeout

Note: This list provides a basic set of error codes. Additional codes may be defined based on specific system requirements and error conditions encountered during development and testing.

A.3 AncASIC Finite State Machine (FSM) Diagram

States:

- **IDLE:** The initial state, where the AncASIC waits for a transaction from the lpGBT.
- **RECEIVE_HEADER:** Receiving and decoding the header (Start of Frame, 3-bit Module Address, Data Type).
- **ADDRESS_CHECK:** Checking if the received "Module Address" matches the AncASIC's address or if it's a broadcast command (000 or 111).
- **DECODE_DATA:** The state where the AncASIC decodes the 40 bit data payload based on the identified *"DataType"* in the header.
- **PROCESS_INTERNAL:** The state for handling transactions intended for internal sub-modules (NBVG or SLDOs). This state has three sub-states:
    - **SUB_MODULE_DECODE:** Decoding the "*Submodule Identifier*" and "*Register Address*" within the internal transaction.
    - **READ_INTERNAL:** Performing a read operation on the specified internal register.
    - **WRITE_INTERNAL:** Performing a write operation on the specified internal register.
- **PROCESS_LAS:** The state for processing transactions intended for the LAS. This state has several sub-states:
    - **LAS_DECODE:** Decoding the "*R/W*" field and other relevant information within the LAS transaction.
    - **MANCHESTER_ENCODE:** Performing Manchester encoding on the 40-bit LAS data frame.
    - **SEND_LAS_CMD:** Transmitting the encoded data to the LAS at 5 Mbps.
    - **WAIT_LAS_RESP:** Waiting for a response from the LAS (for WRITE_no-posted and READ transaction).
    - **RECEIVE_LAS_RESP:** Receiving and buffering the response from the LAS.
    - **MANCHESTER_DECODE:** Decoding the Manchester encoded response from the LAS.
- **SEND_RESPONSE:** The state where the AncASIC sends a response or acknowledgement back to the lpGBT through the *SC_Out* interface.
- **BROADCAST:** Handling broadcast commands. Sub-states:
    - **LOAD_DELAY:** Loading the configured delay value into the digital delay line.
    - **WAIT_DELAY:** Waiting for the delay to elapse.
    - **GENERATE_PULSE:** Generating the *las_reset* or *las_sync* pulse.
- **ERROR:**
    - **INTERNAL_ERROR:** Handles errors related to internal AncASIC operations, such as submodules errors, invalid register accesses, etc.
    - **LAS_TIMEOUT_ERROR:** Handles errors specifically related to response timeouts from the LAS.
    - **MANCHESTER_ERROR:** Handles errors detected during Manchester encoding or decoding.
    - **PROTOCOL_ERROR:** Handles errors related to protocol violations in communication with lpGBT or LAS.

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Transitions:

- **IDLE to RECEIVE_HEADER:** Triggered by the detection of valid Start of Frame pattern on *SC_in* line.
- **RECEIVE_HEADER to ADDRESS_CHECK:** Transition occurs after successfully receiving and decoding the header information.
- **ADDRESS_CHECK to DECODE_DATA:** If "*Module Address*" matches or it's a broadcast command.
- **ADDRESS_CHECK to IDLE:** Transition occurs if the "*Module Address"* doesn't match, discarding the transcation.
- **DECODE_DATA to PROCESS_INTERNAL / PROCESS_LAS:** Transition depends on the identified "*Data Type*" in the header.
- **DECODE_DATA to ERROR:** Transition if the received "Data Type" is invalid or undefined.
- **PROCESS_INTERNAL Transitions:**
  - **DECODE_DATA to SUB_MODULE_DECODE:** Transition occurs when the Data Type is Internal.
  - **SUB_MODULE_DECODE to READ_INTERNAL / WRITE_INTERNAL:** Based on the "*R/W"* field within the internal transaction.
  - **READ_INTERNAL/WRITE_INTERNAL to SEND_RESPONSE:** After completing the read/write operation on the internal register.
  - **SUB_MODULE_DECODE to ERROR / READ_INTERNAL/WRITE_INTERNAL to Internal_ERROR:** Transition if an error occurs during internal operations.
- **PROCESS_LAS Transitions:**
  - **DECODE_DATA to LAS_DECODE:** After decoding the initial information within the LAS data frame.
  - **LAS_DECODE to SEND_LAS_CMD:** If the transaction is intended for the LAS.
  - **SEND_LAS_CMD to WAIT_LAS_RESP:** If the "*R/W"* field indicates a WRITE_non-posted or READ transaction.
  - **SEND_LAS_CMD to SEND_RESPONSE:** If the "*R/W"* field indicates a WRITE_posted transaction to a broadcast command.
  - **WAIT_LAS_RESP to RECEIVE_LAS_RESP:** Upon receiving a response from the LAS.
  - **RECEIVE_LAS_RESP to MANCHESTER_DECODE:** After buffering the complete response from the LAS.
  - **MANCHESTER_DECODE to SEND_RESPONSE:** After successful Manchester decoding of the LAS response.
  - **MANCHESTER_ENCODE to MANCHESTER_ERROR:** Transition occurs if a Manchester encoding error is detected.
  - **MANCHESTER_DECODE to MANCHESTER_ERROR:** Transition occurs if a Manchester decoding error is detected.
  - **WAIT_LAS_RESP to LAS_TIMEOUT_ERROR:** Transaction occurs if the response timeout expires.
- **BROADCAST Transitions:**

    - **DECODE_DATA to LOAD_DELAY:** Upon receiving a valid broadcast command.
    - **LOAD_DELAY to WAIT_DELAY:** After loading the delay value.
    - **WAIT_DELAY to GENERATE_PULSE:** When the delay has elapsed.
    - **GENERATE_PULSE to SEND_RESPONSE:** Upon successful pulse generation.
    - **GENERATE_PULSE to ERROR** (appropriate sub-state): If an error occurs during pulse generation.
- **General Transitions to ERROR State/PROTOCOL_ERROR:** From any state, if an error condition is detected (parity error, CRC error, invalid transaction type, etc.)
- **SEND_RESPONSE to IDLE/ERROR:** After attempting to send the response to the lpGBT:
    - Transition to IDLE if the transmission was successful.
    - Transition to the appropriate ERROR sub-state (e.g., PROTOCOL_ERROR) if an error occurred during transmission.
- **ERROR to IDLE:** After handling the error condition and potentially sending a NACK to the lpGBT, the state returns to IDLE.

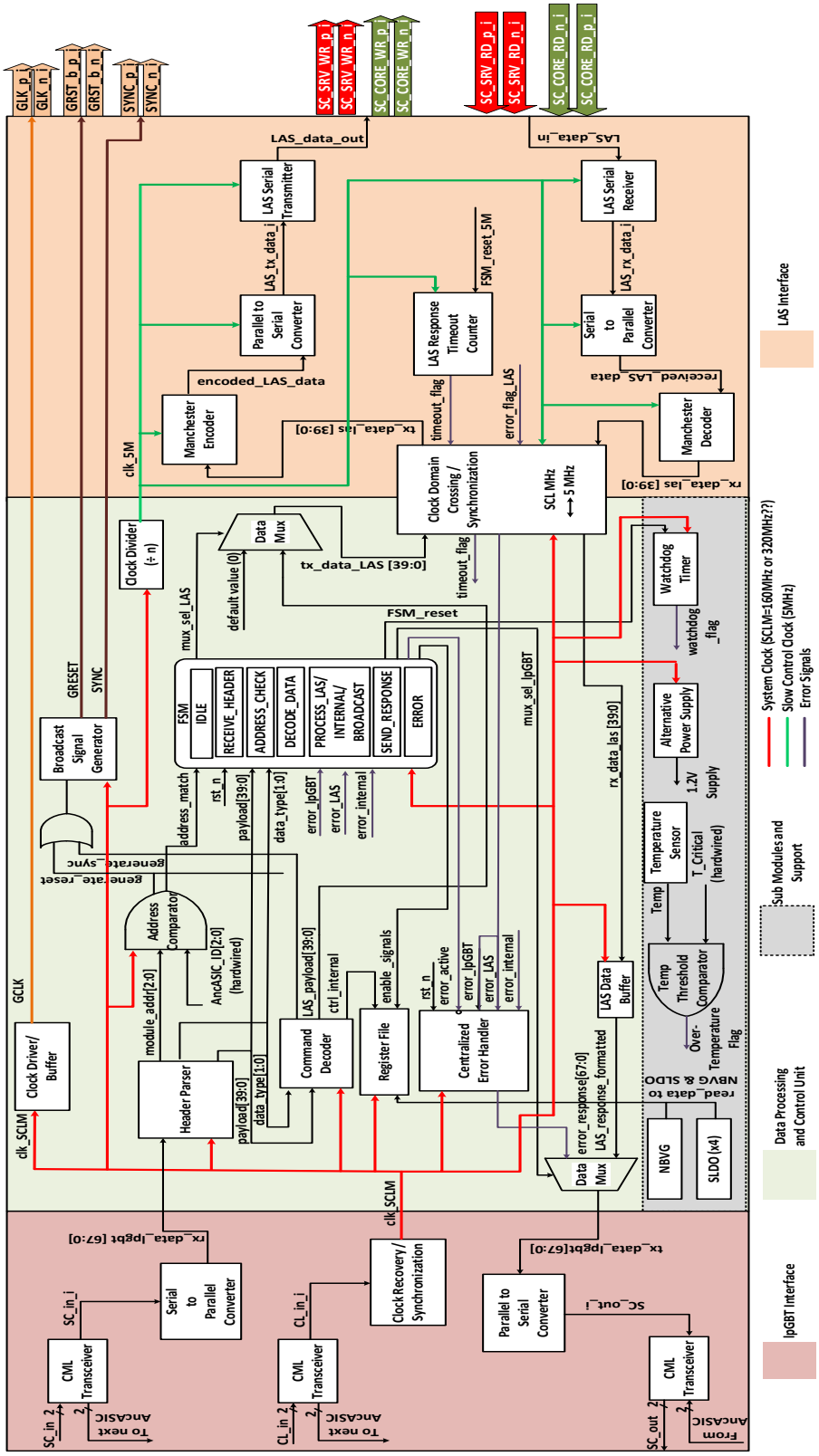
Actions:

- **Each state performs specific actions based on the received data, current state, and transiton conditions. These actions may involve:**
    - Decoding data fields from the received transaction.
    - Checking the AncASIC address or sub-module identifier.
    - Reading from or writing to internal registers.
    - Performing Manchester encoding/decoding.
    - Transmitting data to the LAS or lpGBT.
    - Generating reset/sync pulses.
    - **Error Handling:**
        - Detecting error conditions: Parity errors, CRC errors, invalid transactions, timeouts, sub-module errors(overcurrent, over-temperature, out-of-regulation), and Manchester encoding/decoding errors.
        - Identifying the error source.
        - Assigning the appropriate error code.
        - Generating the error response data frame.
    - Sending acknowledgments (ACK) or negative acknowledgments (NACK).
    - Resetting the watchdog timer.
- **Actions within ERROR Sub-states:**
    - Indentify the specific error condition based on the active sub-state (INTERNAL_ERROR, LAS_TIMEOUT_ERROR, MANCHESTER_ERROR, or PROTOCOL_ERROR).
    - Generate the standardized 40-bit error response data frame, including the appropriate error code and error source information.
    - Transition to SEND_RESPONSE state to transmit the error response to the lpGBT.
- **Recovery from Over-Temperature:**

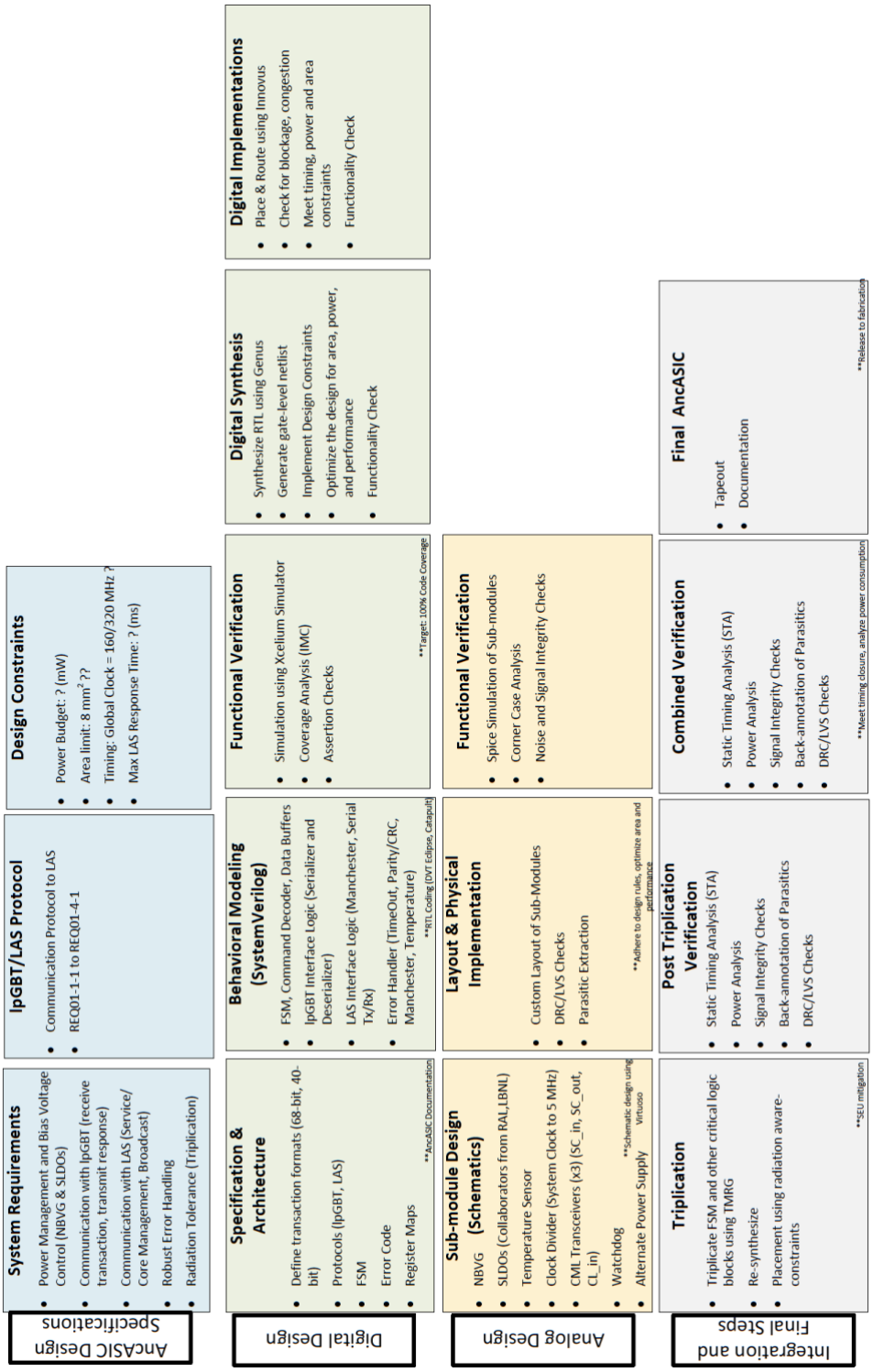
- **Automatic Recovery:** Implement a timer within the INTERNAL_ERROR state. After that timeout, check the temperature sensor; if the temperature is below the threshold, automatically reenable the NBVG and SLDOs and transition back IDLE.
- **lpGBT Controlled Recovery:** Remain in the INTERNAL_ERROR state until specific command from the lpGBT is received. Upon receiving the command, check the temperature sensor; if the temperature is below the threshold, re-enable the submodules and transiton to IDLE.

- **BROADCAST State Actions:**
  - **LOAD_DELAY:** Read the configured delay value from the register and load it into the digital delay line.
  - **WAIT_DELAY:** Monitor the delay line and wait for the delay to elapse.
  - **GENERATE_PULSE:** Assert the appropriate broadcast signal (*las_reset* or *las_sync*) based on the decoded command.

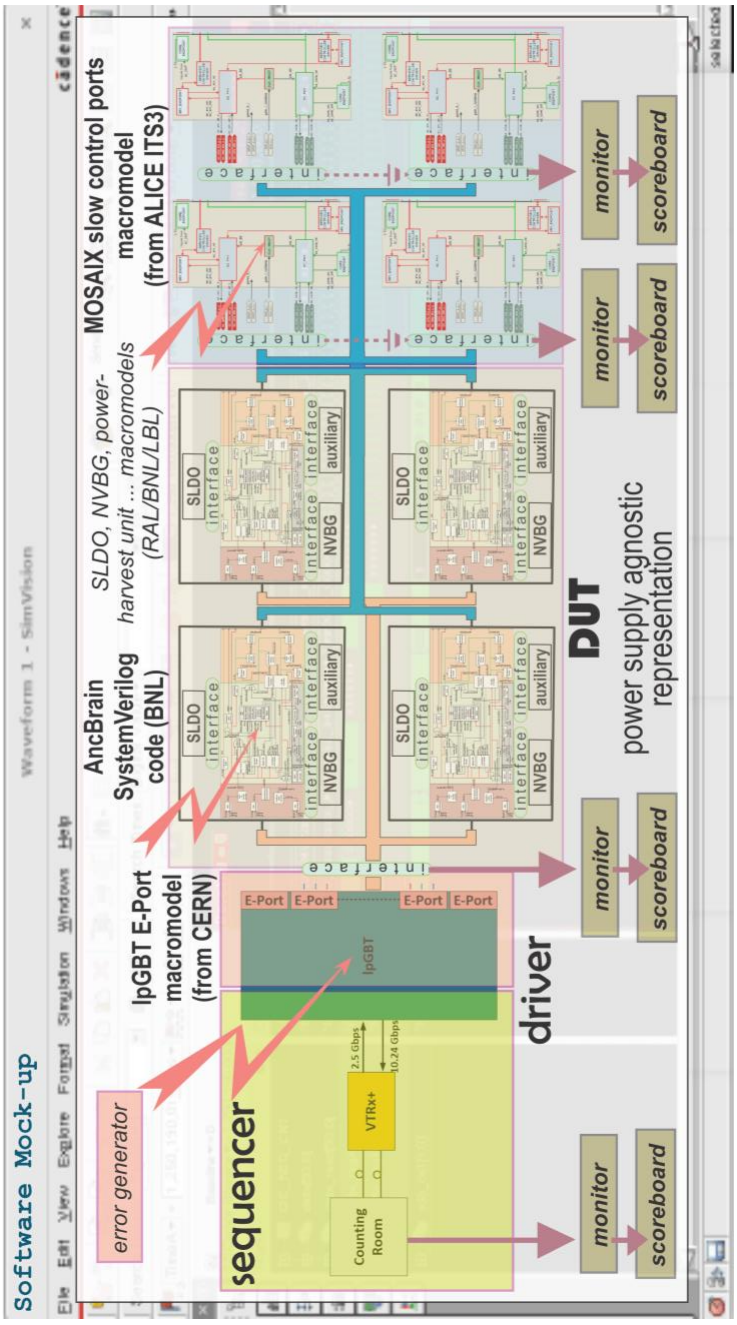
A.4 AncBrain Block Diagram



A.5 AncBrain Implementation Flow



A.6 Software Mockup



A.7 Hardware Mock-up