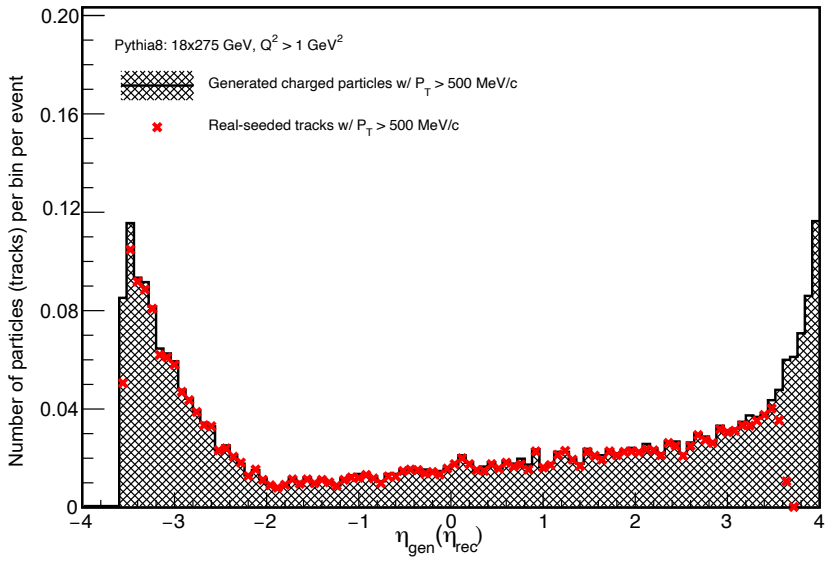


**Figure 8.19:** The number of generated charged particles vs. the generated pseudorapidity of those particles (filled black). The number of reconstructed tracks vs. the reconstructed pseudorapidity of those tracks (red crosses). The y axis shows the number of particles (tracks) per pseudorapidity bin per event. The events were generated with a $Q^2$ minimum of 1 $GeV^2$; the scattered electron peak can be seen at negative pseudorapidity. The particles (tracks) shown all have a generated (reconstructed) transverse momentum greater than 500 MeV/c.

#### 8.3.3.1 The silicon trackers

### Requirements

**Requirements from physics:** The Silicon Vertex Tracker (SVT) needs to meet stringent performance requirements, set by the EIC science program, on acceptance and resolutions for charged-particle trajectories. At a high level, the SVT needs to precisely measure the trajectories of the scattered electron and charged hadrons produced in electron-ion beam collisions over a wide kinematic range. The scattered ion, if it remains intact, is outside of the SVT acceptance. The SVT also needs to measure charged decay-particles from hadrons containing heavy quarks and from vector mesons. It is to aid in particle-identification a) through determination of the displacement of the geometrical origin of the decay particles (secondary vertex) from the collision point (event vertex) via precision reconstruction of both vertices and b) by providing direction and position information on charged-particle trajectories through the outer gaseous tracking subsystems and into the outer particle-identification subsystems.

The SVT is the innermost subsystem of the ePIC central detector. Constraints from the overall detector size and the outer subsystems limit the active volume of the SVT to $-105 < z < 135$ cm and a radius of approximately 42 cm. In combination with the 1.7 T solenoidal field, this leads to a requirement on the point resolution of better than 10 $\mu$m as well as the need to minimize traversed material by limiting the number of detection surfaces and minimizing their radiation lengths.

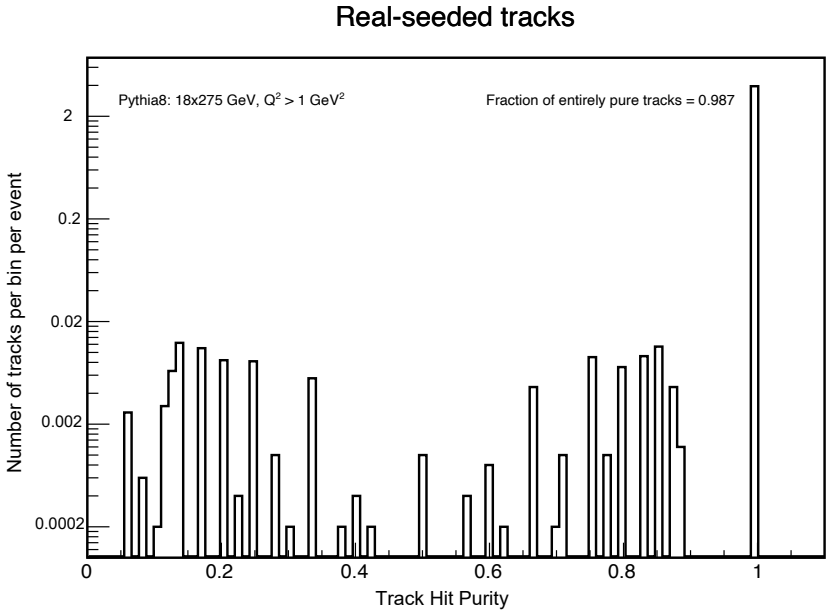


**Figure 8.20:** The distribution of the track hit purity for NC DIS events with a $Q^2$ minimum of 1 $GeV^2$. The track hit purity is defined as the fraction of measurements in a track which are associated with a given generated charged particle. The peak at 1 indicates that most of the tracks ( 99%) are associated only with a single particle.

**Requirements from Radiation Hardness:** We have evaluated the radiation levels in the SVT using the current knowledge of the beam configuration and beam backgrounds from beam gas interactions and synchrotron radiation. Figure 8.21 shows the current estimates for neutron equivalent fluence, and dose. The black lines indicate the approximate locations of the SVT detection surfaces. These radiation maps have been estimated for the beam configuration with the highest luminosity (10 GeV electron beam and 275 GeV proton beam at $10^{34}$ cm$^{-2}$ s$^{-1}$), and include contributions from hadron and electron beam gas interactions. The results assume that the machine and detector run at 100% efficiency for 6 months per year over a period of 10 years. Even under these conservative assumptions, the radiation doses in the SVT will be low to moderate, and are expected to be acceptable. The majority of the SVT will see fluence levels well below $10^{11}$ $n_{eq}$ cm$^{-2}$. The innermost central layers and layers in the hadron going direction will experience slightly higher fluence between $10^{11}$ and $10^{12}$ $n_{eq}$ cm$^{-2}$, with some small regions reaching above $10^{12}$ $n_{eq}$ cm$^{-2}$. The dose rate map indicates that areas close to the beam pipe will experience a total ionising dose between ten and a few hundred krad, while the rest of the SVT remains below 10 krad.

**Requirements from Data Rates:** EIC physics rates are expected to be below 0.5 MHz. That is, only a small fraction of the EIC beam crossings produces a physics event and physics event pileup from within a single beam crossing is negligible. The dominant fraction of these events originate from a region, $|z| < 80 - 100$ mm, surrounding the nominal interaction point. We thus estimate that event pileup within the SVT is determined by its readout frame or integration window of 2 $\mu$s or a small multiple thereof. Within this window, SVT will also accumulate hits from noise and beam backgrounds. We estimate that the associated hit load and data volume will exceed that from physics events. Hit occupancies will be low in view of the high SVT granularity. We estimate a hit probability per pixel per readout frame of $\mathcal{O}(10^{-7})$ and a typical total data rate at the level of 15

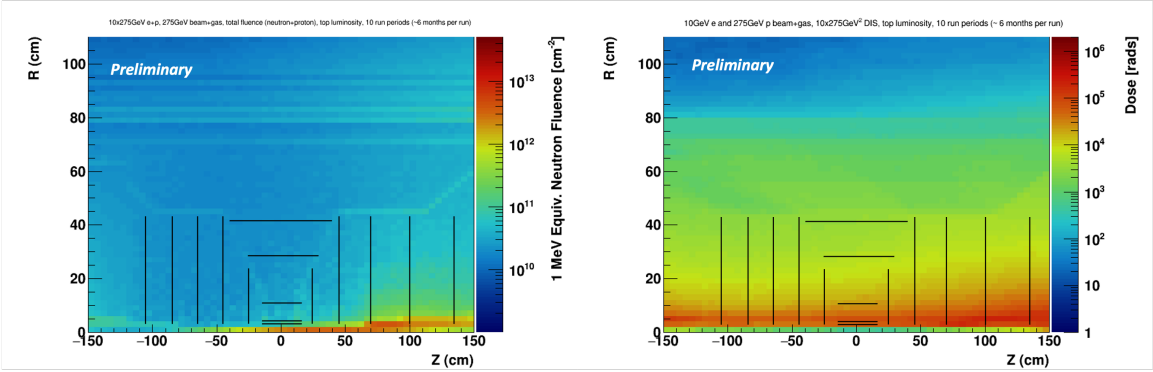


**Figure 8.21:** Maps of simulated 1 MeV neutron equivalent fluence (left) and total ionising dose (right) over the ePIC tracking envelope. This is a conservative estimate assuming 10 years of running at top luminosity with 100% efficient accelerator and detector. The black lines indicate the approximate location of the ePIC SVT detector layers.

Gbps. The sensor and readout chain need to be efficient under these conditions.

## Justification

**Device concept and technological choice:** To meet the stringent requirements on charged-particle tracking and vertexing, we have designed the SVT to provide a well-integrated, large acceptance, high granularity, and low-mass tracking and vertexing subsystem. The SVT has four regions covering a total active area of approximately 8.5 m$^2$. An Inner Barrel (IB) and Outer Barrel (OB), made of three and two active layers, respectively, cover the mid-central pseudorapidity range and have an active volume that extends radially to approximately 42 cm. Endcaps, each with five active annuli surrounding the beampipe, are placed on either side of the nominal interaction point with their active area constrained to $-105 < z < 135$ cm and an outer radius equal to that of the OB. The Electron Endcap (EE) is positioned in the direction of the electron beam and has acceptance for a large fraction of the scattered electrons, while the Hadron Endcap (HE) provides acceptance for many of the hadrons produced in physics collisions. Figure 8.22 shows the SVT regions and geometrical layout.

We designed the SVT to cover the required pseudorapidity range and to reach spatial resolutions as low as $\leq 6$ $\mu$m through a combination of high granularity ($\sim 20$ $\mu$m pixel pitch), lightweight support structures, cooling, and electrical services enabled by a low power sensor design ($\leq 40$ mW cm$^{-2}$). Our development aims at achieving 0.05% $X/X_0$ in the IB, 0.25% $X/X_0$ in the innermost OB layer and in the disks, and 0.55% $X/X_0$ in the outermost OB layer. We selected a sensor technology based on the ALICE-ITS3 development [40] to meet our requirements. This is a new generation, large area Monolithic Active Pixel Sensor (MAPS) in a commercial 65 nm CMOS imaging process.

## Subsystem description:

General device description: Tables 8.2 and 8.3 show the positioning and size of the SVT active layers, together with their material budget target. We designed the IB to provide precise vertex reconstruction, while also contributing to momentum measurement. This is achieved with a combination of very thin layers at optimised radii. The IB will use the ALICE ITS3

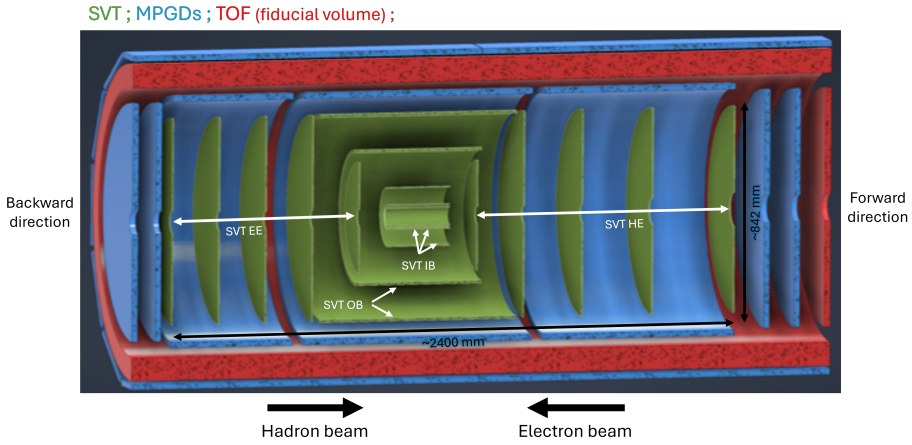


**Figure 8.22:** Schematic layout of the ePIC SVT showing the central region consisting of the inner and outer barrel made of three and two cylindrical layers, respectively, together with the endcap regions made of five annuli each. The figure also shows the surrounding Micro Pattern Gas Detector (MPGD) layers and the envelope of the Time of Flight PID detector.

wafer scale sensor [40] with a suitable adaptation of the ITS3 ultra-thin detector concept to the large EIC beam pipe diameter. The IB design has three layers of silicon sensors thinned below 50 $\mu$m and bent around the beam pipe, with minimal mechanical support, air cooling, and no electrical services in the active area, to reach the very low material budget target of $X/X_0 = 0.05\%$. The innermost layer is positioned as close as possible to the beam pipe, taking into account the constraints coming from the large beam pipe radius and the requirements from beam pipe bake-out, which will be performed with the IB installed. The position of the second layer is chosen to maximize vertex resolution. The outermost layer of the IB aims at maintaining the very low material budget at a radius of 120 mm and serves both vertexing and sagitta measurements. The OB, EE and HE will be equipped with the EIC Large Area Sensor (LAS), a modified version of the ITS3 sensor, optimized for high yield, low cost, and large area coverage. These sensors will be thinned to 50 $\mu$m and mounted on lightweight support structures, in the form of staves for the OB and disks for the endcaps, with integrated cooling and electrical interfaces for power, data and slow control. The OB layers and the endcap disks are positioned to provide high precision measurements over a large lever arm to improve momentum resolution and optimize acceptance at large pseudorapidity. The inner openings of the disks will accommodate beam pipe bake-out constraints as well as beam pipe divergence. These translate into six different inner opening geometries over ten disks.

Sensors: The SVT will be constructed with MAPS sensors, that integrate sensing and front-end electronics functionalities in one device. The ePIC SVT will use MAPS sensors developed in a 65 nm CMOS imaging process based-off the ALICE ITS3 development [40]. This technology enables a high granularity and low power consumption design, and offers stitching on 300 mm wafers for the development of large area sensors. These characteristics are key to delivering a high precision detector through high spatial resolution and minimized material budget.

The SVT IB will use the ALICE ITS3 sensor, called MOSAIX. A sketch of MOSAIX on a wafer is shown in figure 8.23. MOSAIX is composed of an active matrix of Repeated Sensor Units (RSUs). Twelve RSUs are stitched along the length of the sensor, giving a total length of $\approx 27$

| Region | Layer | radius [mm] | length [mm] | $X/X_0$ |
|---|---|---|---|---|
| IB | L0 | 36 | 270 | 0.05% |
| | L1 | 48 | 270 | 0.05% |
| | L2 | 120 | 270 | 0.05% |
| OB | L3 | 270 | 540 | 0.25% |
| | L4 | 420 | 840 | 0.55% |

**Table 8.2:** Radius, length and material budget of the SVT IB and OB layers.

| Region | Disk | z [mm] | $r_{out}$ [mm] | $X/X_0$ | Region | Disk | z [mm] | $r_{out}$ [mm] | $X/X_0$ |
|---|---|---|---|---|---|---|---|---|---|
| EE | ED0 | -250 | 240 | 0.25% | HE | HD0 | 250 | 240 | 0.25% |
| | ED1 | -450 | 415 | 0.25% | | HD1 | 450 | 415 | 0.25% |
| | ED2 | -650 | 421 | 0.25% | | HD1 | 700 | 421 | 0.25% |
| | ED3 | -850 | 421 | 0.25% | | HD3 | 1000 | 421 | 0.25% |
| | ED4 | -1050 | 421 | 0.25% | | HD4 | 1350 | 421 | 0.25% |

**Table 8.3:** Position along the beam pipe, outer radius and material budget for the SVT layers in the EE and HE regions. Disks in the electron direction are labeled ED0 to ED4. Disks in the hadron direction are labeled HD0 to HD4. Disks ED0/1/2 and disks HD0/1 have the same inner opening. Each of the other five disks has a different inner opening.

cm. The sensor will be three, four, and five RSUs wide ($\approx$ 6, 8, and 10 cm) for L0, L1 and L2, respectively. Each RSU is further divided into 12 tiles that can be switch off independently in case of faults to improve yield over such large area device. A row of 12 RSUs, together with the left and right endcap (LEC, REC) is called a segment. The LEC contains circuits for power, slow control and data. The REC hosts another set of power connections to ensure a uniform power distribution over the full sensor length. Data links for each segment can be configured with three links, plus one spare, at 10.24 Gb/s or six links, plus two spares, at 5.12 Gbps. For each segment, seven electrical links provide clock, synchronisation and control signals, referred to here as slow control signals. The clock runs at 160 MHz, while the control signals will run at 5 Mbps. MOSAIX has different power domains for analogue and digital circuitry at 1.2 V, plus two more domains for specific blocks, one at 1.2 V and one at 1.8 V [40]. The sensor's bias voltage will be in a range between -1.2 and -4.8 V.

The SVT OB and endcaps cover an area of approximately 8 $m^2$. Considerations based on yield, cost, integration, and coverage require the use of a sensor with a smaller size than the wafer-scale sensor used in the IB. These regions will use the MOSAIX sensor with modifications to reduce the size. This sensor would still be large in traditional terms and is therefore referred to as the EIC Large Area Sensor (EIC-LAS). The EIC-LAS will be one RSU wide and either 5 or 6 RSUs long. Power will need to be fed into the EIC-LAS only from the LEC given the reduced length. In addition to reducing the size of the sensor, the EIC-LAS will see a reduction of the number of data links to match the lower SVT data rate, reduce material and ease integration aspects. To further ease the integration of the EIC-LAS in the OB and endcaps, EIC-LAS sensors will be powered in series by a constant current and a dedicated communication protocol will be used to reduce the number of slow control links from the

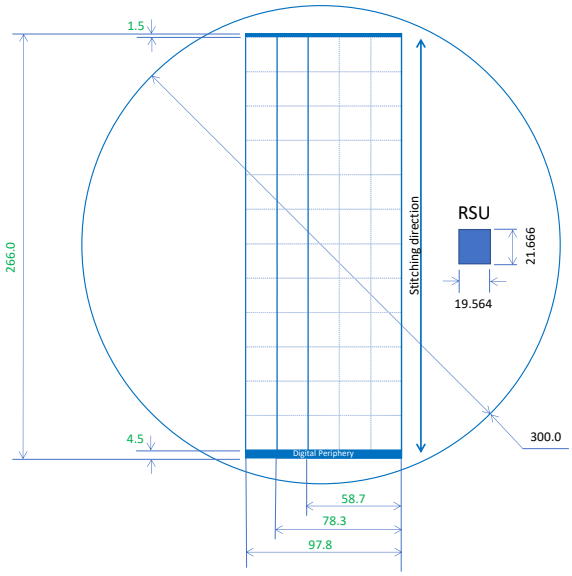


**Figure 8.23:** Sketch of the MOSAIX sensor on a 300 mm wafer showing the size of the RSU, LEC, REC and of the full sensor for the three different widths. All positions are in mm.

counting room to the sensor. These features will be provided by a supporting ASIC, referred to as the Ancillary ASIC (AncASIC).

FEE: One AncASIC will be used per EIC-LAS. This chip includes three main features. It integrates the shunt low-dropout (SLDO) regulator for serial powering. This regulator will generate the voltages needed by the EIC-LAS from the input current. This design is adapted from the original SLDO design for the upgrades of the ATLAS and CMS pixel detectors at the HL-LHC [41]. One AncASIC will integrate five SLDO regulators. The AncASIC will also contain a Negative Voltage Generator (NVG) block. The NVG is a diode-based charge-pump circuit (Dickson-type charge pump voltage multiplier). It will generate the sensor's negative bias voltage from one of the regulated power supplies at 1.2 V generated by the SLDOs. The third block is the Slow Control (SC). Slow control signals from the counting room will be transmitted over I2C for multiple EIC-LAS sensors over one link. The SC block will decode them into the MOSAIX format (i.e. into seven links). The AncASIC will be produced in a 110 nm SOI process offering multiple Multi-Project Wafer (MPW) runs per year and the required transistors' ratings for the SLDO and NVG.

Other components: All components of the SVT detector are designed with the goal of achieving the low material budget target, while providing a robust, high precision system. Traditionally the bulk of the material in silicon detectors is contributed by the powering system. While the IB will powered using a traditional voltgae based powering scheme, a current based power distribution scheme, so called serial powering, is adopted for the OB and disks to reeduce the mass associated to the SVT power distribution. Groups of up to four EIC-LAS sensors are powered in series by a constant current, with the electronics low voltage generated close to the sensors by the SLDO regulators in the AncASIC. This scheme reduces cabling material and provides the only viable powering solution to fit within the available space for services in the ePIC detector. For the smaller IB system, a traditional voltage based, direct powering scheme is foreseen. Data, slow control signals and power are routed over aluminium-based flexible printed circuits (FPC) between the SVT active elements (MOSAIX, EIC-LAS, AncASIC) and the readout (RDO) boards. Four different RDO boards are used in

the SVT: the interface board, the control board, the fiber aggregator board, and the power board. The interface board receives data from the sensors for transmission to the counting room. The control board receives slow control signals from the counting room to be transmitted to the MOSAIX and EIC-LAS (through the AncASIC), and to the VTRX+ devices. Lightweight communication between these RDO boards and the counting room is achieved by use of optical fibers. A fiber aggregator board achieves a reduction of the optical fiber lines through multiplexing via FPGA to match the number of fibers to the available channels of the data acquisition board in the counting room. The data acquisition board is common to all ePIC sub-detectors and it is the FELIX board developed for CERN experiments [42]. The electro-optical interface components used on the interface and control boards are the lpGBT [43] and VTRx+ [44] devices developed by CERN. The power board provides interface for power distribution for sensors and AncASIC as well as devices on the RDO boards. Whilst the functionality of the RDO boards and FPC remains the same, different designs will be needed for IB, OB and disks to accommodate the different powering schemes, number of data links, and sensors grouping. The preferred cooling solution for the SVT detector is air cooling, baselined for the two innermost layers of the IB and under study elsewhere. The OB, EE and HE are designed to allow air flow through the low mass staves and disks, made of carbon composite material, that support the sensors.

**Performance** As discussed in the preceding section, we have simulated track finding and reconstruction within the ePIC software framework to quantify momentum and vertexing resolutions in the nominal 1.7 T solenoidal field strength of the MARCO magnet. The sensor response in these simulations requires cross-validation with actual measurements.

We have performed beamtests at FNAL with a single-RSU sensor, called babyMOSS, from the ITS3 Engineering Run 1 (ER1) submission. In these tests, a particle telescope was constructed using six sensors, with a seventh sensor, the Device Under Test (DUT), placed in the middle. The angle of the DUT with respect to the incident beam was varied in the horizontal plane of the telescope. Figure 8.24 shows a close-up of the telescope and results for the cluster extent as a function of the incident beam angle onto the DUT from data and simulations. The results show that the cluster size increases with the particle incident angle, consistent with a geometrically driven expectation. The analysis of the point resolution as a function of the particle incident angle is in progress. Initial results are consistent with the expectation from the pixel pitch.

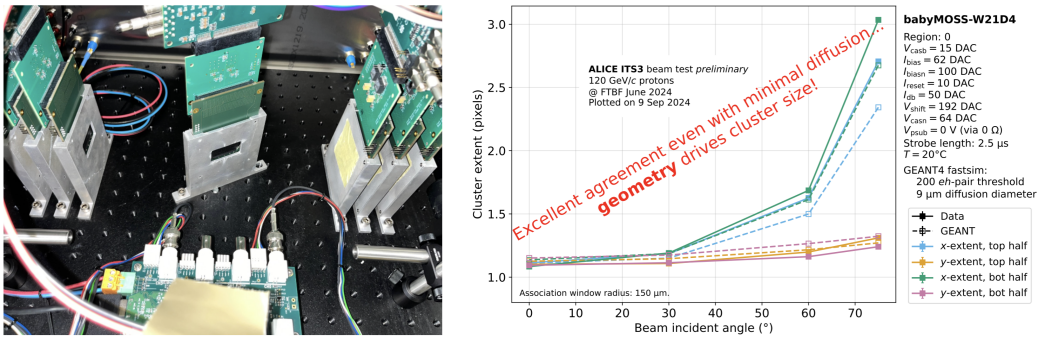


**Figure 8.24:** Left: A close-up of a beam telescope constructed using 6 single-RSU sensors from the ITS3 Engineering Run 1, with a seventh sensor, the Device Under Test (DUT), placed in the middle. Right: Comparison of results from beamtests at FNAL and from simulations for the cluster extent as a function of the beam incident angle onto the DUT.

### Implementation

**Services:** Services to the SVT are of two types: electrical/fiber-optical services and cooling. Electrical/fiber-optical services to the SVT comprise power, data and slow control. Services are routed to/from the IB from the hadron going direction. Services for OB are routed to/from the electron and hadron going directions. For the IB (MOSAIX sensor and direct powering), electrical services will be by MOSAIX segment. For the OB and endcaps (EIC-LAS and serial powering), they will be by group of up to four EIC-LAS. A summary of the data, slow control and power lines needed in the different regions of the SVT is given in Table 8.4.

| Region | Sensor | Electrical services group | # power lines/group | # slow control links/group | # data links/group |
|---|---|---|---|---|---|
| IB | MOSAIX | MOSAIX segment | 10 | 7 | 8 |
| OB | EIC-LAS | Up to 4 EIC-LAS | 2 | 3 | 4 |
| EE/HE | EIC-LAS | Up to 4 EIC-LAS | 2 | 3 | 4 |

**Table 8.4:** Summary of power and readout services for the different regions of the sPIC SVT (slow control and data links are differential pairs of wires). A services group is one MOSAIX segment in the IB, and up to four EIC-LAS sensors (i.e four segments) in the OB and endcaps.

The table illustrates the reduction in power lines using serial powering versus direct powering. In the IB, each MOSAIX segment will need ten lines (including the return line) to serve the four power domains of the electronics plus the sensor bias. For each segment, the full MOSAIX current will be transmitted. In the OB and endcaps two lines (including the return line) will be needed to deliver the same power to up to four EIC-LAS (i.e. four segments). The current flowing on these lines will be the current needed by one EIC-LAS only, reducing the current being transmitted to the detector by up to a factor four, and correspondingly reducing cables cross section and material budget.

Figure 8.25 shows the data and slow control distribution for a group of four EIC-LAS in the OB and disks. Each data line connects to one input of a VTRx+ on the interface board. Given the high speed of the data transmission, this board will be placed at the end of each stave and disk for signal integrity. The VTRx+ transmits the data of a group of up to four EIC-LAS over a bundle of optical fibers to the counting room (each VTRx+ has a pigtail bundling up to 5 optical fibers). Slow control signals are transmitted over optical fibers to the control board, placed along the SVT support structure. Once converted into electrical signals, one lpGBT elink provides the slow control signals to up to four AncASICs. Each lpGBT has 16 elinks, meaning that each control board will serve multiple groups of up to four EIC-LAS. The slow control signals are transmitted between the control board and the AncASIC either in a daisy-chain architecture (as shown in the figure) or via multi-drop. The exact configuration is still being evaluated. The AncASIC converts the incoming I2C protocol to the MOSAIX protocol expected by the EIC-LAS. As the OB and endcaps are powered in series, each EIC-LAS is on a different ground potential. A dedicated communication scheme is thus needed. Data lines will be AC-coupled. For the slow control, a standard DC transmission is also being investigated with the ground difference between EIC-LAS sensors being accommodated.

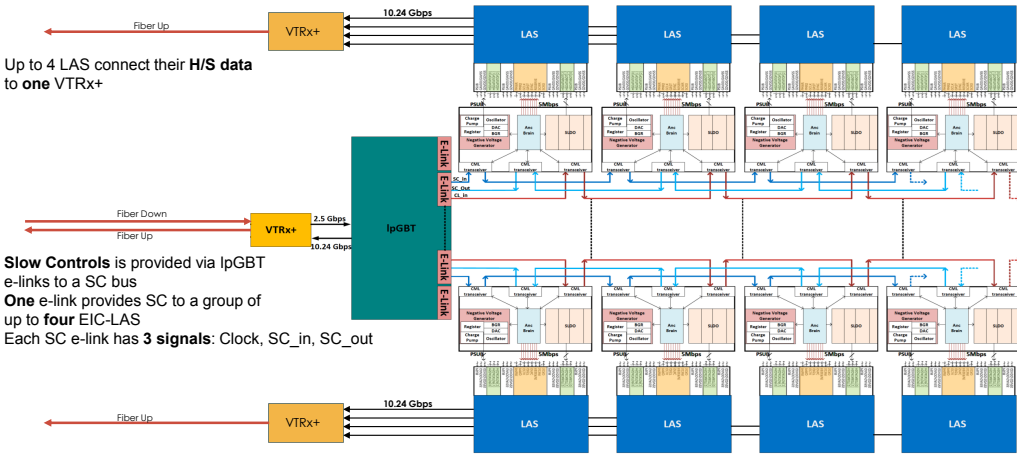


**Figure 8.25:** Schematic overview of data and slow control lines to groups of up to four EIC-LAS in the OB and disks.

Flexible printed circuits (FPCs) are required to electrically connect MOSAIX sensors, EIC-LAS sensors and AncASIC chips to the interface and control boards. In the IB the FPC will connect to the LEC of the MOSAIX sensor. In the OB and disks, a main FPC will run along staves and disks, serving groups of up to four EIC-LAS sensors. It will connect to the AncASICs through bridge FPCs (see prototype in fig. 8.32). The maximum length of the main FPC is constrained to a maximum of 40 cm based on signal integrity and power drop considerations. Two and four main FPCs will be needed on L3 and L4, respectively, to cover the full length of the stave. The FPCs must have a low mass in order to maintain the low material budget of the SVT. It is therefore advantageous to select conductive tracks made of aluminium ($X_0$ = 8.9 cm) instead of traditional copper ($X_0$ = 1.4 cm). Dielectrics like polyimide ($X_0$ = 28.57 cm) are the default solution for the manufacturing technologies of aluminium-based FPCs deployed in scientific experiments. The selection of the dielectric material is dependent on its loss-tangent properties versus the frequency of the signals to be transmitted. Typically the most stringent requirements for signal attenuation are set by the high-speed data transmission lines. In case of the ePIC SVT, it is envisaged that data links can transmit signals as fast as 10.24 Gb/s for a length of $\sim$50 cm. The baseline configuration for the FPCs assumes a stack-up made of two aluminium conductive layers (each $\sim$15 $\mu$m thick) separated by a polyimide dielectric substrate ($\sim$35 $\mu$m), and then additional polyimide cover layers ($\sim$35 $\mu$m combined thickness) to insulate the conductive tracks from external electrical shorts. This cross section ($\sim$100 $\mu$m in total) would equate to a combined material budget of $\sim$0.06% $X_0$. The combination of serial powering, slow control daisy-chained/multi-drop configuration and impedance matching at 100 $\Omega$ for clock, control lines and data, enables a reduction of the number of signals to be propagated. This is particularly important for staves and disks where the FPCs overlap the sensitive area of the MAPS. By combining these power and signal distribution techniques, it is estimated that the minimum width for the FPC can be as narrow as 6 mm. This is $\sim$1/3 of the width of the LAS ($\sim$19 mm).

The transmission of the signals to the counting room will see a further stage of processing. The data fiber-optic lines will be aggregated in the aggregator board, common to all SVT regions, which has multiple fiber inputs, an FPGA for extracting the payload from these fibers, and one fiber output towards the FELIX board, thus reducing the number of fiber inputs at the data acquisition boards. For the FPGA, we are considering both a radiation tolerant PolarFire FPGA and an SRAM based FPGA, with the choice to be made depending on the location of this board and radiation levels present.

For the optical interface, we are considering both a FireFly optical transceiver and a standard SFP (Small Form Facotr Pluggable) transceiver. It is estimated that approximately 5000 data fiber links run from the sensors to the aggregator board. Assuming an aggregation factor of 10, there will be approximately 500 fibers towards the DAQ FELIX boards, which can be accommodated by 11 FELIX boards (assuming each FELIX board will have 48 fiber inputs).

Cooling adds to the service load, including the target radiation lengths in the SVT active areas. The preferred cooling solution for the SVT detector is air cooling (using dry air), baselined for the two innermost layers of the IB and under study elsewhere, with liquid cooling in strategic places as necessary. We will operate the sensors at or near room temperature ($\sim 25\,^{\circ}$C), which requires a lower coolant temperature. Thermal performance of the cooling is measured was the temperature difference between the sensor and the coolant, i.e. $\Delta T = T_{sensor} - T_{inletairorcoolant}$. Our target for thermal tests and simulations is $\Delta T$ of $10\,^{\circ}$C. FEA analysis is underway based on current power dissipation estimates.

For the inner layers of the IB, the baseline is air cooling with thermally conductive foam near the LEC. Measurements from ALICE ITS3 show this is reasonable to cool the MOSAIX sensor [40]. Air will be forced between L0 and L1. To cool L2, the possibility for natural convection with liquid cooling near the LEC if necessary is under study. The air inlet and outlet are under design, with the bulk of the material to be placed on the hadron-going side of the detector.

In addition to cooling during operation, the IB will need to be kept cool during beam-pipe bake-out. The aim is for no additions to the operational cooling, i.e. no additional material (e.g. insulators) or changes (i.e. liquid instead of air). Ongoing ANSYS studies at Jlab and LBNL, discussed further down, have shown that there are options to keep the detector cool under these constraints. Tests of sensor prototypes by ePIC (flat sensor prototypes) and ITS3 (wafer-scale, curved mechanical prototypes) institutes, at temperatures up to $50\,^{\circ}$C in a climate chamber have shown no electrical and no mechanical failures.

The target for both the OB staves and the EE and HE disks is air cooling. We are targeting a maximum air velocity of 12 m/s within the structures of the staves and disks. Current estimates are approximately 1700 $m^3h^{-1}$ total air split between the staves and disks. This will require compressed air to mitigate the otherwise excessive size and number of air tubes coming into the detector and pressure regulation inside the detector. Studies are ongoing to reduce these numbers, including the use of thermally conductive materials (e.g. carbon foam) to help with heat dissipation. The SVT will be interlocked to turn off in the case of failure of its cooling system, including conditions so as to prevent pressurizing the system beyond its design values.

**Subsystem mechanics and integration:** The SVT IB, OB, and disks are supported by their own support structure. The outermost components of this structure are carbon composite half-cylinders, which jointly form the experiment's so-called inner support tube. The inner support tube surrounds the entire SVT and spans its entire length. Cones inside the inner support tube connect the OB to the IB and to the innermost disks. These cones are supported from the inner support tube and are projective to the nominal collision point. They are currently designed to consist of spokes. The outermost disks connect to the inner support tube. This entire SVT support structure, shown schematically in fig. 8.26, is integrated in and supported off the experiment's global support tube.

The IB layers will be made of two symmetric half-layers, which will be the basic assembly elements of the detector. The two innermost layers (L0 and L1) will be based on four MOSAIX sensors (two for each half-layer), while the outermost layer (L2) will contain eight MOSAIX sensors (four for each half-layer). The MOSAIX sensors for L0, L1, L2 will be three, four and five segments wide, respectively. All the sensors equipping a given half-layer will be placed one next to the other to

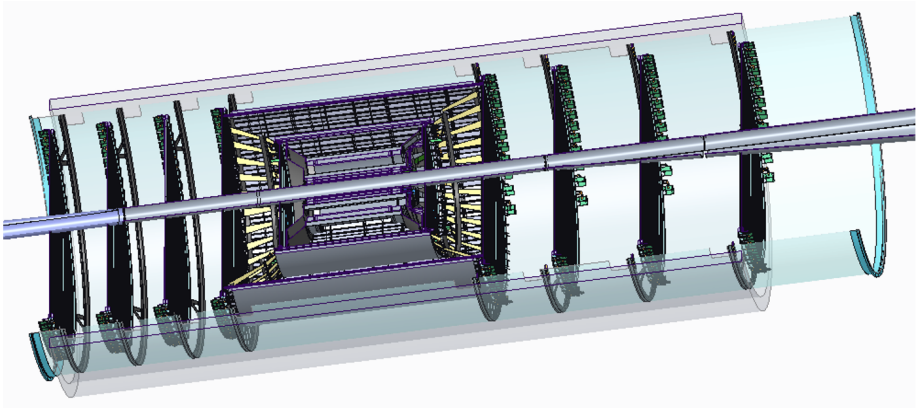

**Figure 8.26:** SVT global support structure, consisting of a surrounding carbon composite support tube and a projective arrangement of spokes that form cones connecting the IB, OB, and innermost disks. Also shown are several outer disks and the beampipe.

fully cover the half-layer surface and bent on a cylindrical shape at the corresponding radius (c.f. table 8.2).

Each IB half-layer will consist of the following components: the MOSAIX sensors, a local support structure mainly made in carbon foam shaped as a frame along the edges of the sensors, two sets of FPCs wire-bonded to the sensor peripheries for powering and data/control transmission. The sensor cooling will be air-flow based and delivered through appropriate ducts that will be part of the local support structure and matched to the global mechanics described below.

The IB global support will be the main structure supporting the MOSAIX sensors already assembled in half-barrels. The current design foresees a cylindrical frame structure for each layer, supported by two conical endcaps, one for L0-L1 and a second for L2, the last including a flange for connection to the L0-L1 half-cone and to the OB. The material is currently fixed in a carbon fiber composite, whose thickness will be approximately 0.5 mm. A half-cylindrical shell made of polyamide is placed outside and close to L2 for mechanical stability in the current design. Electrical services for the IB are brought in/out from the hadron going side and are routed along the inner surface of the conical support. In the current design the routing of the power cables to the REC needs that the longerons of the local mechanics have also the role of cable trays. The requirement of rigidity and the U-shape for cables routing suggests carbon fiber composite as a preferred material choice, while alternatives are being considered. Figure 8.27 shows CAD representations of the IB support.

For the OB, EE, and HE, we introduced a modular approach in the SVT design to simplify the assembly process of these complex detector elements, reduce risks and increase the predictability of the production rate. EIC-LAS sensors and AncASICs will be assembled into modules, that will pre-assemble and pre-test and then mount/interlink in the final staves or disks. The EIC-LAS sensors and AncASICs will be connected via flexible printed circuits boards and micro-electronics interconnection techniques to form an electrically coherent unit, and supported by a mechanical frame to be interfaced with cooling systems and to meet handling requirements.

The design of a module for the outer barrel envisions two EIC-LAS with their respective two AncASIC (see Fig. 8.28). The mechanical frame is made of a thin film of polyimide that holds together all the module components. The design of a module for the disks envisages one LAS and one AncASIC and a mechanical frame made of a carbon fibre plate. We will test modules standalone after

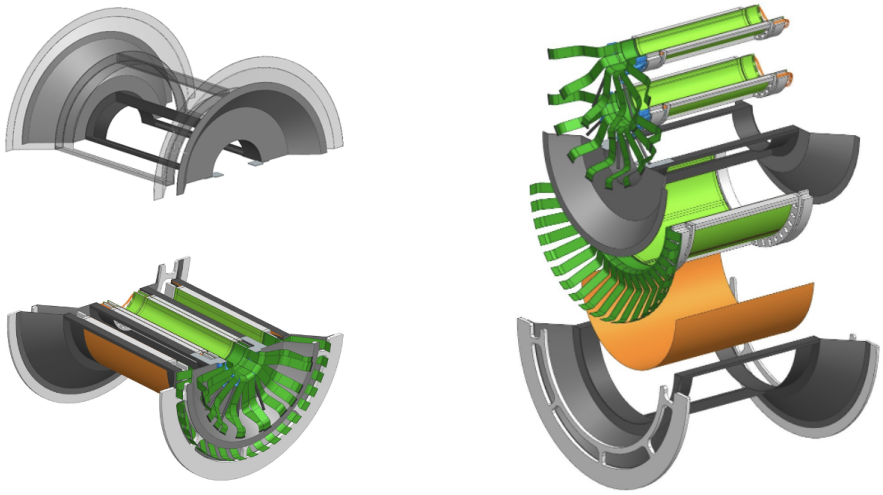

**Figure 8.27:** Left: CAD representation of the IB global support (top) and IB half-barrel CAD view with sensors and cable routing (bottom). Right: Exploded CAD view of IB. The orange element is the kapton shield. In blue the air conveyors are shown.

their assembly and before their assembly into staves or disks.

The outer barrel layers will be segmented in staves. The staves are composite structures using carbon fibre (CF) skins, a central CF I-beam spar and cross-ribs made of K9 foam. The side walls will be formed by the FPCs. The structure has openings where modules will be placed. During module mounting the modules are glued on top of these openings, forming a closed hollow structure with large second moment of area, and thus high stiffness. The closed structure provides a contained channel for the forced flow of air through the stave, that will remove the heat from the sensors and ancillary ASICs. In addition to their structural function, the cross-ribs made of highly thermally-conductive K9 foam are placed underneath high-power density components (the left endcap of the EIC-LAS and the AncASIC) to improve the transfer of the heat into the air coolant flow. Drawings of the stave design with all its components are shown in Fig. 8.28.

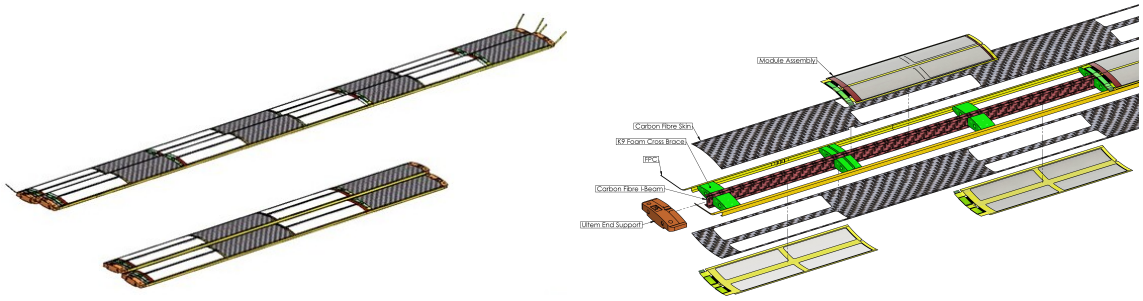


**Figure 8.28:** Left: OB staves for L3 and L4. Two staves per layer are shown. Right: Exploded view of an OB stave.

Each stave is one OB module (i.e. two EIC-LAS) wide, and has modules on both facings, staggered in $z$ so that the active areas of the modules provide overlap for tracks from the vertex. L4 staves will hold 4 modules on each facing, or 8 modules in total, while L3 staves will have half that number. The dimensions of the staves are dictated by the layout of the SVT and we achieve the required

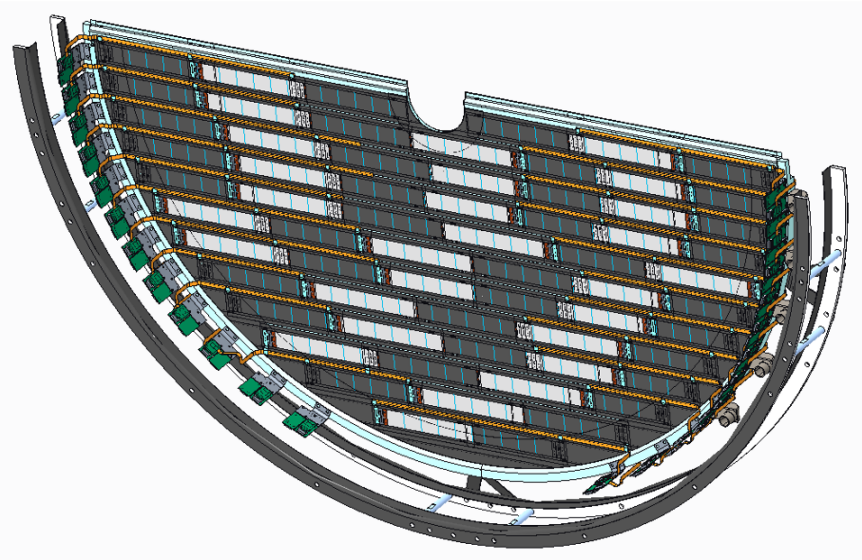

**Figure 8.29:** CAD model of the preliminary (half-) disk design. Modules are shown in alternatingly inward (dark gray) and outward (white) facing orientations. Common bus FPCs are shown in orange. RDOs (green) are arranged on the outside of the disk ring, inside of the interface to the SVT global support structure.

coverage with LAS made up of 6 RSUs in L3 and 5 RSUs in L4, respectively. L3 will consist of two halves with 44 staves in total in a castellated layout to cover the full azimuth. L4 will consist of two halves and have 70 staves. Our initial FEA analysis of the modal frequencies finds $f_1 = 91.6$ Hz.

The staves will connect mechanically at their ends to segmented half-cones that are part of the SVT support structure. This interface still needs to be detailed, but will constrain stave rotations at the support, while allowing for limited misalignment of the support cones and thermal expansion of components. The interface will also contain the couplings of the air channel inputs to the supply distribution. The cones interface at their outer radius with a support tube surrounding the entire SVT, including its services, and also connect to the the global support structure of the IB and the innermost disks.

The EE and HE disks are a two-sided design with a corrugated carbon composite core. A CAD model of the disk design is shown in Figure 8.29. The purpose of the corrugation is to add strength without adding too much mass. The corrugated channels can be used for air flow to cool the disks. It also gives options for sensor layout to maximize overlaps of inactive area. Modules with one EIC-LAS will be tiled over the valleys of the corrugation on either side of the disk, creating overlap along the long axis of the sensor. Modules will be placed in an alternating inward and outward facing orientation along the corrugation which ensures that an active area of the neighboring sensor covers the insensitive LEC.

Each disk will have a ring at the outer radius that will sandwich the corrugated core to provide mechanical support, a mounting point for the RDOs, and an inlet for air cooling. Those rings will then connect mechanically to either the SVT support cone (ED0-1, HD0-1) or support cylinder (ED2-4, HD2-4). This design is currently being optimized in conjunction with the global mechanics.

**Calibration, alignment and monitoring:** Calibration procedures are needed to optimize the settings for the pixels in the MOSAIX and EIC-LAS sensors. We anticipate these to be similar to those used for the existing ITS2 sensor (i.e ALPIDE), and ITS3 sensor prototypes, and consist in data-taking scans where one injects a charge into groups of pixels and varies their settings. We have made initial estimates of the time required to perform such scans and anticipate that they can be done in a parallel fashion in approximately half an hour with the final readout system.

Alignment procedures are needed to achieve the required resolutions. We will survey the IB (half-) layers, the OB staves, and the EE and HE disks with precision coordinate measuring machines during their construction and will pursue a global survey during installation. Final alignment will be track-based.

Monitoring will include sensor settings and other slow-control data, including temperatures, as well as analysis in near-realtime of residuals in alignment and other observables.

**Status and remaining design effort:**

R&D effort: The development of the MOSAIX sensor is well underway. Two submissions have already taken place in 2020 and 2022. The former, so called MLR1, included numerous test structures for technology exploration and to develop prototype circuit blocks for future sensors. The latter, ER1, contained exploratory designs to study stitching principles, methodology and yield. The submission of the MOSAIX sensors (ER2) aiming to satisfy ITS3 requirements is planned for beginning of 2025. ePIC designers are integrated in the MOSAIX design team and contributing to the development of logic libraries, and circuitry for data transmission over the full sensor length between RSUs. The final submission (ER3) will be the MOSAIX production version for the ITS3 detector and the ePIC SVT IB.

Work on the EIC-LAS has started in terms of defining the required modifications (reduction of size and data links). Design work will start once the design database is available upon signature of the necessary CERN-EIC agreement.

The AncASIC is in development with good progress on all functional blocks. The design of the first NVG prototype is completed both at schematics and layout level. The SLDO prototype schematic is ready and simulated, and work on the layout is ongoing. Parts of the slow control block relating to the communication with the lpGBT are begin designed, with the interface to the EIC-LAS to be defined once the MOSAIX slow control interface is completed. MPW runs are foreseen to prototype and verify each block, before submitting the full chip, ready for production in early 2027.

E&D status and outlook – IB: We have developed a preliminary design for the two innermost (L0 and L1) half-layers of the IB and its global support mechanics. Different solutions have been explored for bending and assembly of each half-layer: connecting two sensors in a single object and following a "half-layer" based procedure has been considered largely preferable mainly due to advantages from overlaps with the ITS3 building concept. Once the two half-layers have been individually built, they are assembled in a L0-L1 half-barrel. Blank silicon pieces with dimensions corresponding to the final MOSAIX sensors have been used to advance the design of the L0-L1 assembly and will serve to build the first half-barrel prototypes. In parallel, a preliminary design of the whole SVT IB mechanics, including an external shell to L2, has been also developed and a first mock-up is being built.

We will evolve the designs for the half-barrel assembly and for the global mechanics, towards properly engineered realistic ones. The next half-barrel assembly to be built will integrate prototypes of most of the components of the final detector and allow for thermo-mechanical studies to finalize the cooling design. Test campaigns in a climate chamber and in a wind

tunnel facility for ageing and cooling studies are planned. Building of a first L2 half-layer prototype, based on the guidance from the L0-L1 assembly experience, is also scheduled to happen in parallel.

For the SVT IB global mechanics, we will use carbon fiber composites as the main material for the support, given the low mass and excellent mechanical properties. In the coming months an engineered version is planned, with the goal of both verifying possible space conflicts within the global mechanics and matching with the SVT IB assembly procedures.

E&D status and outlook – OB: We are currently prototyping (fig. 8.30) the curved surface stave design for L4 to evaluate the performance of the design, as well as tooling and assembly procedures. In the first phase we are prototyping the stave design with the curved facings, as this is the more challenging to construct. Interfaces to the support cones will be designed in parallel with the design work on these structures.

These prototypes will be equipped with mechanical dummy sensors (40 $\mu$m unpatterned silicon) for mechanical studies, and thermo-mechanical dummy sensors (40 $\mu$m silicon encapsulated in 25 $\mu$m and 50 $\mu$m thick Kapton layers with a 5 $\mu$m thick Cu trace layer). In particular, we will verify/measure: Manufacturability (co-cure), mechanical integrity and good compaction of carbon fibre; Mechanical response spectrum up to 500 Hz and associated $Q$ values; Deformations with air flow up to 20 m/s; Surface temperatures with thermo-mechanical dummy sensors powered up to 40 W per stave; Thermo-mechanical deformations with thermo-mechanical dummy sensors powered up to 40 W per stave. The results from these studies will guide us in finalizing the stave design. In the first phase we are pro-

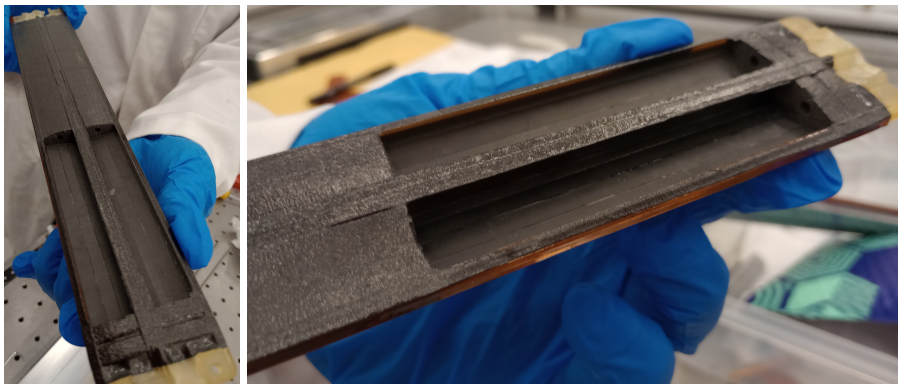

**Figure 8.30:** Co-cured support structure of first L4 quarter length stave prototype (without silicon sensors). The co-cure comprises carbon fibre skins, K9 cross ribs, central carbon fibre I beam spar and Kapton side closeouts (compare to fig. 8.28).

totyping the stave design with the curved facings, as this is the more challenging to construct. Interfaces to the support cones will be designed in parallel with the design work on these structures.

E&D status and outlook – Disks: Work continues on the design and layout of the disks. We are finalizing the carbon fiber layouts for both the corrugated core and the flat module sheets. The first prototype was made using a non-woven, randomly oriented mat of thin carbon fiber called carbon fiber veil for both the face sheets and corrugation and had a density of 500 gsm. However, the veil is not ideal for thermal performance and can be challenging to layup on the corrugated tooling. New prototypes are being made with K13CU unidirectional carbon fiber, which has a much improved thermal conductivity.

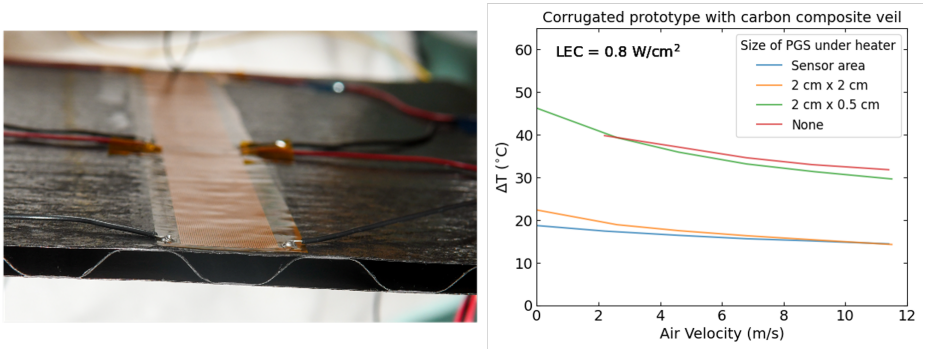


**Figure 8.31:** (Left) First test piece of the carbon composite corrugated disk core made in the LBNL composite shop. Heaters with two different heating zones that can mimic the sensor power density are placed on the carbon composite facesheet and are used for thermal measurements. (Right) Observed $\Delta T$ on the LEC section of the test heater versus coolant air velocity using corrugated carbon fiber veil prototype test piece. Measurements taken with various sizes of PGS placed underneath heater.

The initial test piece has been tested for thermal performance using copper trace heaters. The prototype is shown on the left side of Figure 8.31 and the thermal test results with the heaters are shown on the right. The measured $\Delta$T is well within 10 °C for the expected EIC-LAS RSU power density, but is high for the expected ELC power density, though trending in the right direction with increased air flow, and is dependent on the planned design dissipation. The thus far high values of $\Delta$T for the LEC region can be due to many factors, including the low thermal conductivity of the carbon fiber veil and the overall thinness of the contact surface. We are studying mitigation possibilities using pyrolytic graphite sheets (PGS), which have a large in-plane thermal conductivity (upwards of 800 W/m·K) and significantly improve the thermal performance of the prototype. The new face sheets made with K13CU have similiar thermal conductivity to the PGS and initial tests are promising. A new, full prototype is being assembled with the K13CU carbon fiber.

We are currently working on prototypes focused on the development of assembly tooling, module handling, and thermal and mechanical tests. Prototypes will undergo vibration tests to understand mechanical stability. Mechanical dummy silicon (40 $\mu$m unpatterned silicon) is in hand to construct a quarter disk mechanical prototype. We expect thermo-mechanical dummies (as described above for the OB staves) at the end of 2024 to create a thermo-mechanical prototype.

The bench tests will be paired with ANSYS structural and fluent simulations to understand the performance under air flow and the structural integrity of the disk. This will also need to be accompanied by bench tests and simulations that include the disk support ring and the outer ring.

E&D status and outlook – FPCs: The first iteration of FPC prototypes is underway targeting an initial design for OB L4. A definition stage captured the current design requirements for powering, data transmission and geometrical factors. This was followed by a design stage and then by an order submission to RPE LTU (Ukraine). The first set of prototypes (Figure 8.32) are currently being manufactured. The prototypes from RPE LTU will be distributed for testing to SVT institutes. In parallel, prototypes from Omni Circuit Board (Canada) are being evaluated and a third supplier, Q-Flex Inc. (USA), has been approached to procure low level prototypes. The aim is to evaluate the capabilities of three different suppliers to manufacture FPCs with aluminium conductors. Signal and power integrity of the FPCs will

be tested and the performance over samples of different suppliers compared. A key requirement is signal attenuation for the high speed differential transmission lines (10 Gb/s). Wire bonding and single point Tape Automated Bonding (spTAB) are being evaluated as potential interconnection techniques in ongoing and future prototypes.

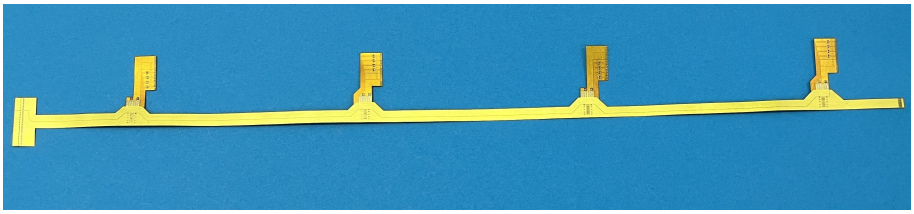

**Figure 8.32:** An example of a low technology readiness level prototype for the FPC of the OB L4. Prototype made by RPE LTU. The figure shows the main FPC with four bridge FPCs.

E&D status and outlook – Powering: The need to regulate voltages for the MOSAIX sensors as close to the IB (to minimise losses) dictates the need for a(t least one) powering board. Considerations for the design and development of these boards are ongoing; this includes deciding how many regulation stages give the best balance between power losses (fewer stages is likely to mean longer lengths of the most lossy cables, when delivering low voltage and high current), versus additional material in the detector volume (more stages equals more high material powering board, and the final voltage regulation is likely closer to the active area of the IB).

Conceptual powering schemes were developed and used to define specifications for the AncASIC and FPC designs for the OB and Disks. Requirements are being iterated based on limitations introduced by these designs so that they can be iteratively improved. Testing and confirmation of requirements will occur as prototypes become available; this includes:

- Verifying output voltages and current capacity of the individual SLDOs.
- Verifying output voltages of NVGs.
- Daisy-chaining AncASICs to verify serial powering chain performance.
- Quantifying performance of the FPCs in terms of current carrying capacity and voltage-drop along the conductor lengths.
- Combining the above elements to test full serial powering chain prototypes (1 FPC feeding current to 4 AncASICs, each loaded with an EIC-LAS-like structure).

E&D status and outlook – Powering: The need to regulate voltages for the MOSAIX sensors as close to the IB (to minimise losses) dictates the need for one or more types of powering board. Considerations for the design and development of these boards are ongoing; this includes deciding how many regulation stages give the best balance between power losses (fewer stages is likely to mean longer lengths of the most lossy cables, when delivering low voltage and high current), versus additional material in the detector volume (more stages equals more high material powering board, and the final voltage regulation is likely closer to the active area of the IB).

The design of the serial powering scheme is evolving alongside the AncASIC and FPC designs for the staves and disks, to define length of serial powering chain, the data and slow control transmission schemes.Testing and confirmation of requirements will occur as prototypes become available. This includes:

- Verifying output voltages and current capacity of the individual SLDO regulators.

- Verifying output voltages of the NVG.
- Daisy-chaining AncASICs to verify current flow in the powering chain.
- Quantifying performance of the FPCs in terms of current carrying capacity and voltage-drop along the conductor lengths.
- Combining the above elements to test full serial powering chain prototypes (one FPC feeding current to four AncASICs, each connected to a load mimicking the EIC-LAS current consumption ).

E&D status and outlook – Readout: Work on readout electronics has mainly concentrated on testing evaluation boards of the various components being considered for SVT readout: lpGBT, VTRx+, radiation tolerant FPGA PolarFire, optical FireFly. An initial prototype for the fiber aggregator board was discussed and is now under development using a commercial FPGA board (ZCU102) mated with the optical FireFly FMC card to provide up to 8 fiber inputs and multiple fiber outputs. The VLDB+ board from CERN (containing both lpGBT and VTRx+) was used to setup a full chain starting from a Skyworks clock generator board as a stand-in for the Global Timing Unit (GTU), a Xilinx ZCU102 board running lpGBT-FPGA firmware as a stand-in for the FELIX board, and the VLDB+ board as the RDO. A measurement of the jitter of the clock recovered by the lpGBT demonstrated adequate performance of this chain to provide a low-jitter clock to the sensors.

We are currently developing a test system for the serializer chiplet of the ER1 prototype submission in collaboration with ITS3 colleagues. This serializer is a prototype for the 10Gbps serializer to be deployed in the LEC the MOSAIX. The test system consists of an FMC card which contains the bonding pads for the serializer chiplet, as well as various drivers and connectors including the possibility to drive the high-speed signal onto a Flex-PCB to test the signal integrity over those traces. The FMC card itself will connect to a commercial Xilinx FPGA board for pattern generation and checking.

Another prototype development is the "MOSAIX Mock-up" board, consisting of an FMC daughter card which contains the various readout components (2 data VTRx+ and an lpGBT / VTRx+ combination for the slow control interfaces). It will interface to a ZCU102 board where firmware will simulate the responses to slow controls commands, while also allowing to simulate data packets to be sent over the up to 8 fiber optic lines of the 2 VTRx+ interfaces in order to develop both data acquisition protocols and slow controls interfaces of the readout electronics to the MOSAIX sensor without the need of an actual MOSAIX sensor.

E&D status and outlook – Cooling: Our prior work has shown that foam can be an important factor in the cooling and thermal performance of staves and disks. This is an integral part of the OB stave design and is being pursued as an option for under the LEC and AncASIC in the disk design. Both will be tested using thermal and thermo-mechanical dummies with upcoming prototypes.

The final air cooling system will be designed based on the overall air volume of the SVT. Current estimates put the total air volume around 1000 cfm total, which would require a pressurized system. The air will be pressurized before entering the ePIC detector volume and then regulated down to various pressures as required by the different parts of the SVT (e.g. OB design requires air above 1 atm).

Simulations from LBNL and JLab have shown that during beam-pipe bake-out a 5 mm distance from the beam-pipe can keep the silicon below 30 °C with air flow below 10 m/s. However, air flow between the beam-pipe and L0 brings down the temperature of the beam-pipe and can affect ability to reach the 100 °C required inside. Studies are ongoing to determine what hot gas temperature is needed to bring the beam-pipe to temperature and what effect that has on the silicon. We also plan to study if airflow only between L0 and L1 is sufficient to

keep the detector below the current 30 °C requirement as this will help mitigate the effect of the air cooling on the beam-pipe itself. Simulations will be paired with thermo-elastic studies in a climate chamber that will study cycling, longevity, and assess the point of failure.

Other activity needed for the design completion: We are continuing our testing characterization of the products from the ITS3 sensor development sequence. We are currently preparing for the first tests on MOSAIX at CERN, in collaboration with ITS3, using a high-frequency wafer probe setup that we are jointly developing. Laboratory tests of thinned and diced wafers are also being planned, as well as beamtests and irradiation efforts.

The AncASIC will be manufactured in a different process than the MOSAIX and EIC-LAS sensors. We are readying an initial MPW submission in this 110 nm process and are planning for its testing and validation. Test structures and the main functional modules of AncASIC, the SLDO, NVG and Slow Control, will undergo irradiation to verify their correct functioning in the expected radiation environment.

Status of maturity of the subsystem: The SVT underwent an incremental Preliminary Design Review (PDR1) in March, 2024. The maturity of the SVT is currently estimated to be at the 45% level overall, with considerable variation for different elements. The development of the EIC-LAS requires access to the MOSAIX design database, which is subject to a BNL-CERN agreement that has not been signed to date. The project identified the need for early procurement of the VTRx+ optical link module for data transmission and the lpGBT low power gigabit transceiver in the SVT readout and slow-control chain as part of potential CD-3B scope. The Final Design Review (FDR) for these elements was successfully passed in June 2024. The remaining effort, while substantial, is progressing and is anticipated to be more than 60% ready by the EIC CD-2 project phase at the end of 2025.

**Environmental, Safety and Health (ES&H) aspects and Quality Assessment (QA planning):** We will follow and adhere to all applicable ES&H standards during the development, construction, installation, and ultimately commissioning and operation of the SVT. Hazards include those associated with adhesives, carbon composites, flammables, wafer-probing and wire-bonding, use of radioactive sources, testbeams, and irradiation facilities, and electrical safety. Where possible, we will work across institutions to implement standardized controls and mitigations, as well as documented safety procedures.

System tests in the development phase of the SVT are integral to our quality assessment. Quality Control forms an integral part of the work breakdown structure (WBS) and schedule during construction and assembly.

**Construction and assembly planning:** The L0-L1 half-barrels will be manufactured in Italy by INFN: the current plan is to have a main assembly site in Bari and a second one in Padova currently being equipped. The L2 production half-layers will be built in the US. Both construction activities will rely on a first step fo QC of the sensors through wafer probing. They will also include a final QC step of the corresponding complete assembly: this will include operation with air-cooling to verify thermal performance and testing of readout and control lines. After a successful pass of the QC step, L0-L1 half-barrels and L2 half-layer will be shipped to BNL. The global IB mechanics will be produced by INFN in Padova, undergo a QC step based on a metrological survey and finally shipped to BNL. At BNL the L0-L1 half-barrels and L2 half-layers will be assembled to the global mechanics to form complete IB half-barrels. All the connections to services (powering, cooling and readout) will be put in place to allow a final QC step.

Modules and staves for the OB layers will be manufactured in the UK. Currently we plan to manufacture modules at two sites, Birmingham and Daresbury Lab. This production includes electrical bonding of the sensors and ancillary ASICs to the bridge FPC. Module construction concludes with a QC on the completed module before shipping to the stave loading sites. Stave production, which comprises manufacture of the stave composite structures, and gluing of modules onto the structures and electrical bonding of the bridge FPCs to the main FPCs, will be performed at Oxford and RAL. Again, the final step of the stave construction will be a QC of the completed stave. This will comprise operation with internal air cooling to verify thermal performance, operation of control lines and readout of modules. After successful pass of these QC steps, staves will be shipped individually to BNL. At BNL staves will be mounted on the support half-cones from the inside, starting with the outermost layer L4. This involves mechanical connection, connection of the air supply, and connection of the FPCs to the RDO boards on the support cones, and mounting of the RDOs on the outside of the support cones. After the mounting of the L4 staves they will be tested, and after that the same procedures will be repeated for the inner OB layer, L3.

Disks and their modules will be produced and assembled in the US. LBNL, Purdue, and LANL are expected to be disk assembly sites, with LBNL and Purdue also serving as module assembly sites. Assembly of modules includes gluing of sensors to carbon composite structures, as well as electrical connection (wire or tab bonding) to a bridge FPC and the AncASIC. Modules will undergo QC before being assembled onto disk structures. The corrugated carbon composite disk structures and module flat sheets will be produced at LBNL and shipped to LANL and Purdue. Disk support rings will be produced by an outside vendor, validated at LBNL, then shipped to disk assembly sites. Disks will be assembled in halves, first on one side and then the other. Disk assembly includes gluing modules and common bus FPCs onto the front and rear sides of the discs and making electrical connections. QC is planned for each corrugated row assembly and then again after completion of the front and rear sides of each disk. Disks will be shipped in halves to BNL, where they will be installed into the larger SVT assembly. Disks are the last piece to be installed, after the IB and OB. Installation will occur from the inner disks outward. ED0 and HD0 will be mounted to the SVT support cones. ED2–4 and HD2–4 will be mounted to the support cylinder. ED1 and HD1 could be mounted to either and will be iterated with global mechanics. Installation must include the connection of the services, connecting of the air supply, and mounting of the RDOs. Each half disk will be tested after installation.

The IB, OB, and disks can thus be constructed concurrently. We plan to produce the outer global support structures at Purdue and/or LBNL. Readout will be led by ORNL with testing at multiple sites. The construction of the SVT can be completed in three to four years in a technically driven schedule.

**Collaborators and their role, resources and workforce:** The SVT currently has collaborators at 20 institutions with the main institutional roles and resources outlined above.

**Risks and mitigation strategy:** The SVT depends crucially on its sensors, the ITS3 sensor used in the IB and the ITS3-based EIC-LAS used in the OB, EE, and HE, since they form the only known way to meet the full performance requirements within ePIC. Their development is ongoing and thus presents a risk. The project and institutions involved in the SVT have identified one main branchpoint, related to the possibility that the EIC-LAS development is delayed and becomes incompatible with the overall EIC project schedule. If this branchpoint were triggered, the SVT OB will be replaced with two MPGD barrel layers derived from the outer MPGD tracker, specifically its innermost (micromegas) layer. The SVT EE and HE will in this case each be replaced with in total up to seven near-identical MPGD disks, specifically based on the existing uRWELL disks.

The SVT IB remains based on the wafer-scale sensor of the ALICE-ITS3 upgrade in this case. The ALICE-ITS3 project is about to submit the second engineering run of its wafer-scale sensor and its timelines are compatible with those of the EIC project. In case of unforeseen future (sensor) delay, we will need to reprioritize ePIC efforts towards the ALICE-ITS3 sensor.

#### 8.3.3.2 The MPGD trackers

##### Requirements

**Requirements from physics:** Micro-Pattern Gas Detector (MPGD) technologies have been chosen to complement the Si based tracking layers. MPGDs are relatively fast detectors able to provide precision space point measurements with good timing resolution, while also maintaining the overall conservative material budget that is required of the ePIC detector [45]. MPGDs will play a role in pattern recognition for central tracking system in the required pseudorapidity range of $-3.5 \leq \eta \leq 3.5$, and aid in PID reconstruction.

The EIC collider is expected to deliver collisions with bunches crossing every ∼10 ns [46], which will require the MPGD detectors to provide timing resolution of 10-20 ns to separate events from adjacent bunches. For ep collisions of 10 × 275 GeV, the DIS physics rate is expected to be around 500 kHz, while hadron and electron beam gas backgrounds rates are estimated to be 32.6 kHz and 3.17 MHz, respectively [47]. These rates are well within the rate capabilities of MPGDs. Combining the timing information from the MPGDs with information from the Si detectors will allow pattern recognition algorithms to discriminate between physics and background signals. In addition to providing hit information with good timing resolutions, the MPGDs will provide

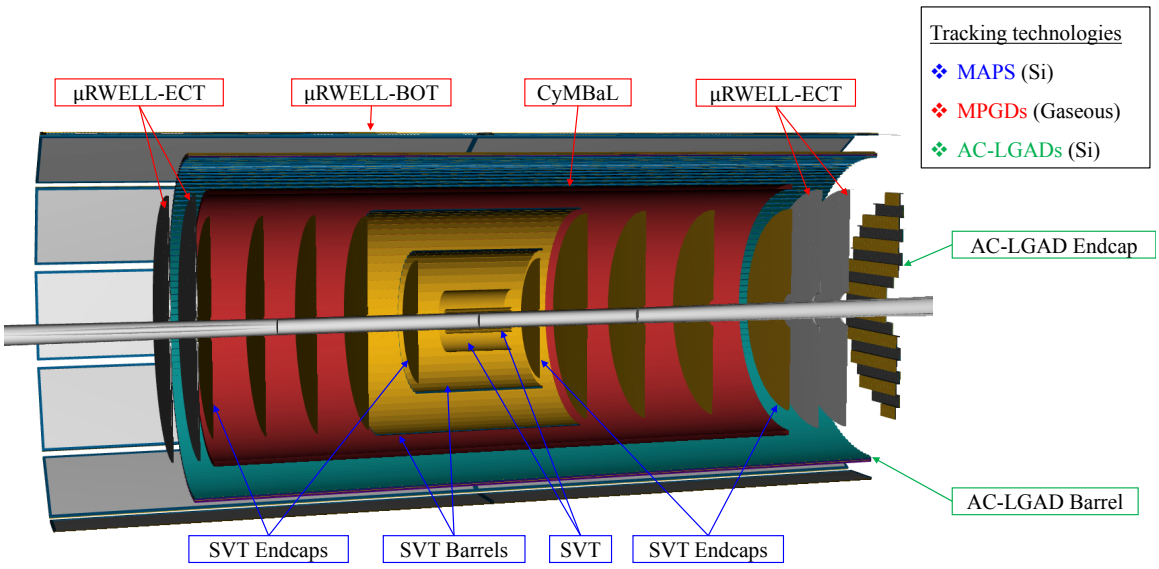


**Figure 8.33:** ePIC tracking subsystems.

additional hit points needed for robust track reconstruction. Early simulations showed that the number of hit points used in the track reconstruction reduced from around 6 hits near $\eta = 0$, to