Brookhaven National Laboratory

Jefferson Lab

U.S. DEPARTMENT of ENERGY | Office of Science

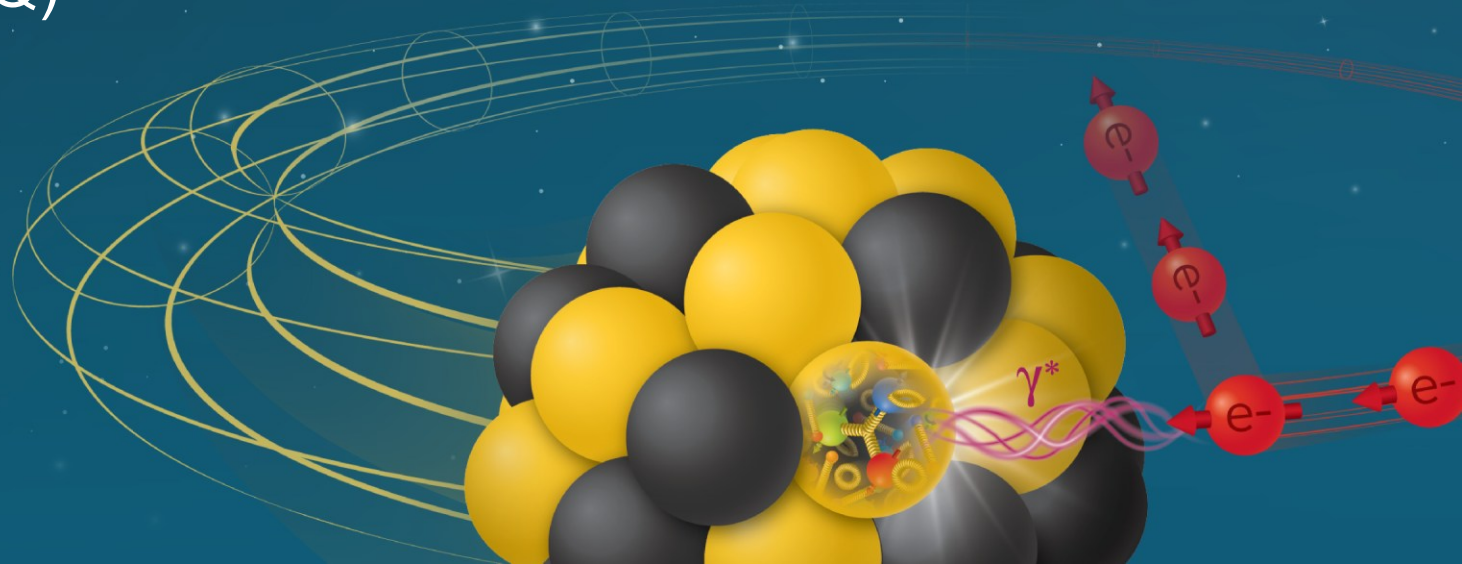
DAQ/Computing

David Abbott (JLAB) & Jeff Landgraf (BNL)

L3 Managers WBS 6.03.08 (DAQ)

10th EIC DAC Review

June 11th – 13th, 2025

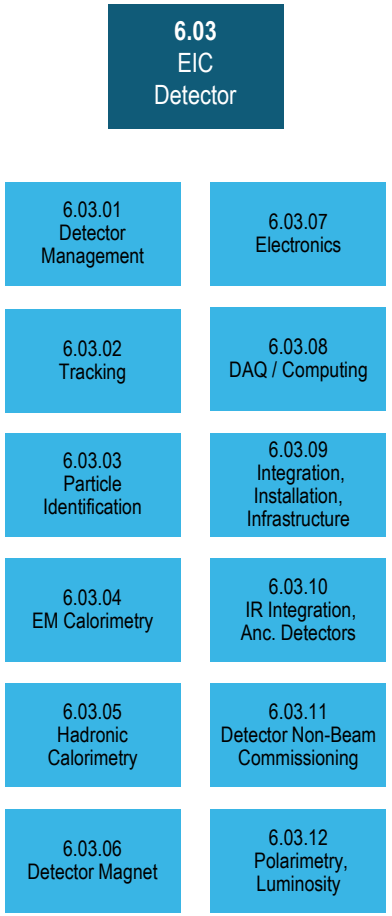


Electron-Ion Collider

Charge Questions Addressed

1. Is the design of the ePIC detector and its sub-systems appropriate and progressing well?
2. Are the remaining work and technical, cost and schedule risks adequately understood? Are there opportunities?
3. Will the detector be technically ready for baselining by late 2025?
4. Are the detector integration and planning for installation and maintenance progressing well? Are there areas where further ideas should be pursued?
5. Will the detector be ready for start of construction by late 2026?

Scope: WBS 6.03.08 – DAQ/Computing



WBS 6.03.08	DAQ/Computing	D. Abbott/J. Landgraf

Scope Definition:
This WBS covers the effort for the data-acquisition (DAQ) and computing necessary to collect all data from the front-end detector electronics as well as from relevant slow control and accelerator systems. The DAQ will support a streaming (triggerless) readout model, collecting all the data from the different subdetectors and suppress detector pedestals and noise.

Deliverables:
A DAQ-system compatible with a streaming readout approach of the EIC detector.

WBS 6.03.08.01	Data Acquisition	D. Abbott

Scope Definition:
This WBS specifically covers the efforts associated with the primary DAQ related infrastructure and requirements including the development of the global timing and synchronization system and the front-end link aggregation hardware (FPGA Based). It also addresses the online computing requirements associated with zero suppression, background and noise filtering as well as event identification.

Deliverables:
Custom hardware and firmware, COTS computing and networking as well as software necessary for readout, beam and detector Q/A and intermediate data storage

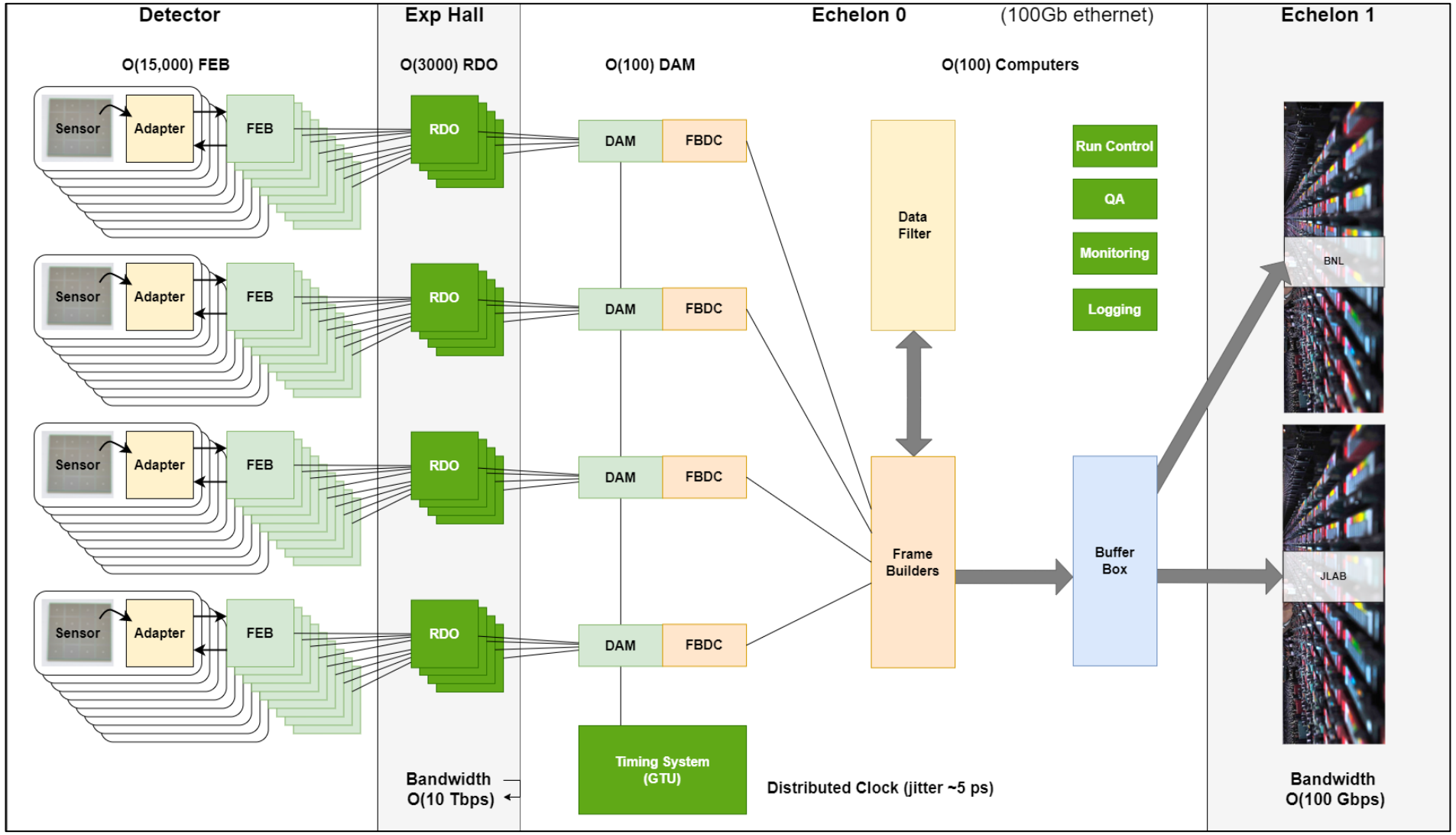
WBS 6.03.08.02	Slow Controls Integration	D. Abbott

Scope Definition:
This WBS addresses efforts necessary for the integration of all detector-related slow controls information. This includes the general network infrastructure in both the experimental hall and the counting house, computing and database resources and manpower to coordinate subdetector slow control software applications and DAQ integration.

Deliverables:
A controls system and network infrastructure for the DAQ and all the subdetectors

EIC Streaming DAQ/Computing Architecture

- Bunch Crossing
  ~10.2 ns/98.5 MHz
- Interaction Rate
  ~ 2 us/500 kHz
- Low occupancy



Streaming in ePIC

DAQ

Definition of streaming is “No L0 trigger”

- All data is zero suppressed by the front-end electronics
- No system wide deadtime in normal operation
- Collaboration should have the full ability to make data selection cuts on the widest possible criteria
  - Flexible event selection, data selection and background characterization
- But subject to an overall throughput budget of ~100Gb/sec

ePIC Streaming will include

- Capabilities for hardware and firmware-based triggering / data selection
- Capability for flow control
- Zero suppression & aggregation within data packets

Greater sensitivity to noise than triggered system

Greater sensitivity to backgrounds than triggered system

Computing

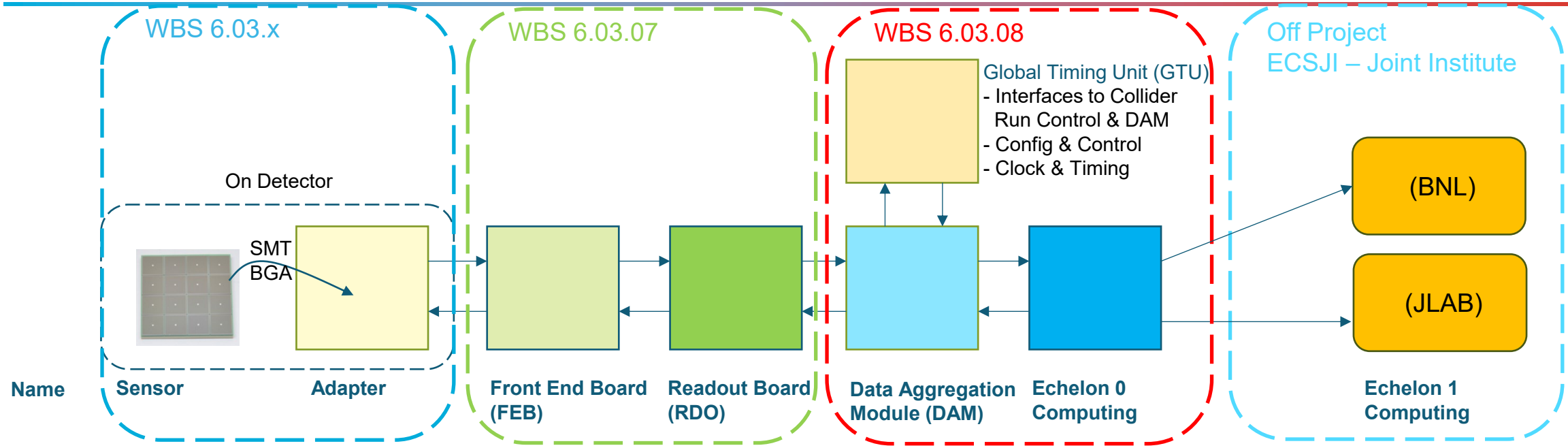
Definition of streaming is “Process data as it arrives”

- Fast Reconstruction (~3 weeks not months or years) using automation of calibration and reconstruction.

Requires some overlap between DAQ/computing

- Automation of calibrations
  - Mapping calibration dependencies
  - Mapping application of calibrations
  - Mapping evolution of calibrations
- QA and monitoring can make use of full offline structure
- Consistent schemes and language for data/metadata
- Event selection / tagging / and accounting
- Global data taking state model, including data types & quantity available, state of calibrations, and reconstruction goals is required for automation

ePIC Readout Chain

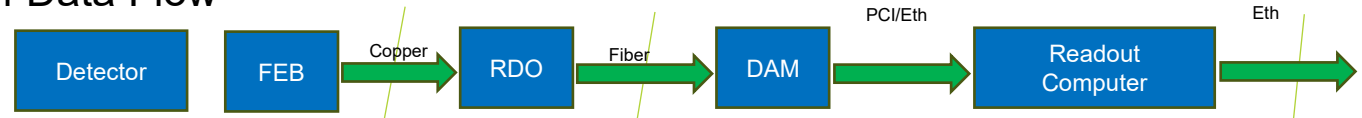


Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Echelon 0 Computing	Echelon 1 Computing
Design	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common	Common
Function	Multi-Channel Sensor	-HV/Bias Distribution -HV divider -Interconnect Routing	-Amplification -Shaping -Digitization -Zero Suppression -Bias Control & Monitoring	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Config & Control -Clock & Timing	-Data Buffering and Sinking -Calibration Support -QA/Scalers -Collider Feedback -Event ID/Building -Software Trigger -Monitoring	- Archive - Reconstruction - Analysis
Attributes	MAPS, AC-LGAD MPGD, MCP-PMT SiPM, LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA or lpGBT -Fiber Link	-Large FPGA -PCIe -Ethernet	-COTS -Ethernet	

Summary of Channel Counts and Data Flow

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					183	5863	183	183	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364		1364	30	50	12
PID Cherenkov			318k		143k	1334	1334	1242	1334	33	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		3.4k					25	289	11	37	8
Lumi		128k	5.1k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**2,657**	**11,121**	**2,253**	**3,973**	**113**	**1,774**	**109**

Summary of Data Flow



Aggregate	2.0 Tb/sec
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	2.0 Tb/sec
Per RDO (Avg)	0.7 Gb/sec

Aggregate	115 Gb/sec
Collision Signal	62 Gb/sec
Synchrotron Rad	6 Gb/sec*
Electron Beam	4.5 Gb/sec
Hadron Beam	1.0 Gb/sec
Noise	41 Gb/sec

Scale of the system:

- **Electronics**
  - ~ 24 detectors
  - ~ 5 Readout Technologies
  - ~ 3000 RDOs (on detector/in racks)
  - ~ 100 DAM boards (DAQ room)
  - GTU (with interface boards)
- **Maximum Data Volume**
  - ~ 2 Tb/sec digitized
  - ~ 115 Gb/sec recorded
- **Online Computing**
  - ~200 nodes (DAQ Room/SDCC)

* Synchrotron radiation caveats:
1. Rates are based upon hit rate for all ePIC detectors. In fact, data volumes depend upon specific detector hit (64 bits/hit assumed)
2. Highest Synchrotron radiation / electron beam gas will correspond to lower values for collision signal
3. Plan to analyze by component soon

Schedule

- A functional DAQ will be necessary for small scale detector testing as well as commissioning and pre-ops.
- Computing resources are staged to make purchases when the hardware is needed, taking advantage of price savings and performance improvements in time.
- **Hardware and software development early in the construction phase will involve a series of releases with increasing functionality.**

Detector Install: FY29Q2 - FY31Q2
Cosmics: FY31Q3
Early CD-4: FY32Q4

DAQ Releases:

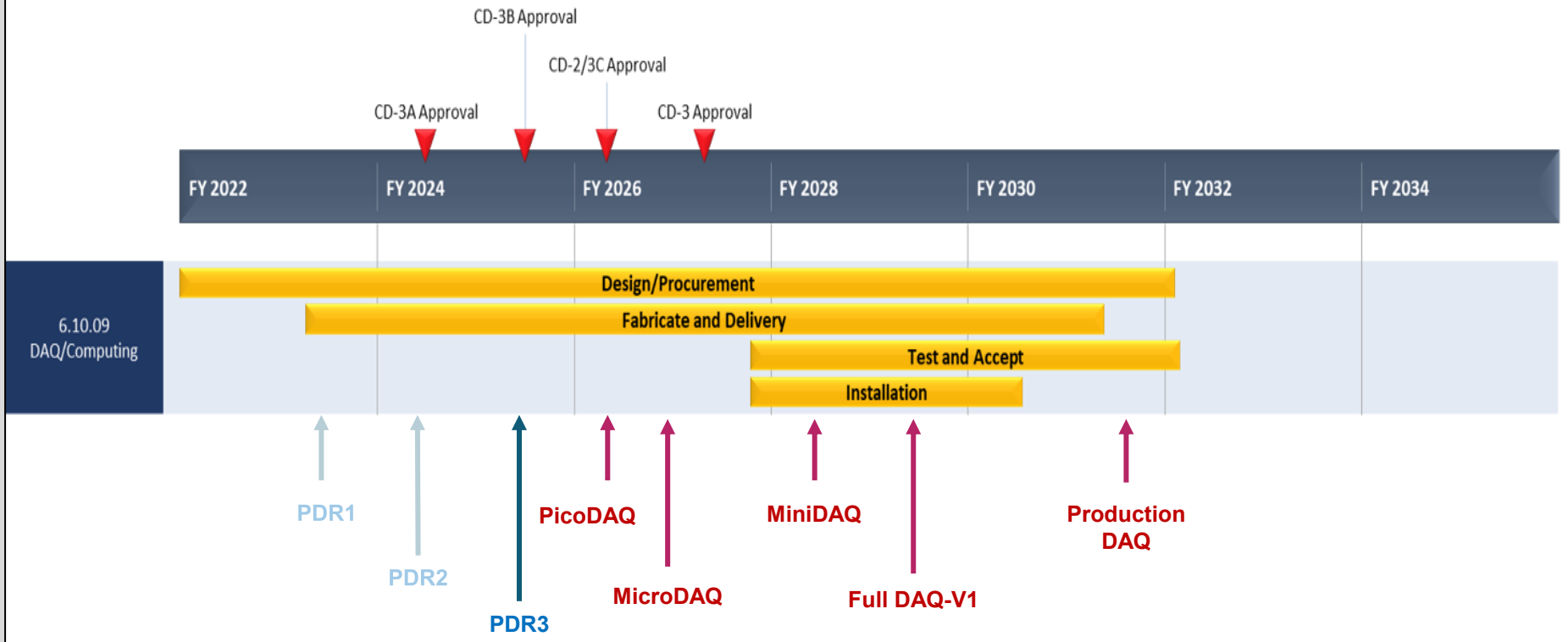
PicoDAQ **FY26Q1**
Readout test setups

MicroDAQ: **FY26Q4**
Readout detector data in test stand using engineering articles

MiniDAQ: **FY28Q1**
Readout detector data using full hardware and timing chain

Full DAQ-v1: **FY29Q2**
Full functionality DAQ ready for full system integration & testing

Production DAQ: **FY31Q3**
Ready for cosmics



Non-LLP pre-baseline schedule is in progress

Schedule

- A functional DAQ will be necessary for small scale detector testing as well as commissioning and pre-ops.
- Computing resources are staged to make purchases when the hardware is needed, taking advantage of price savings and performance improvements in time.
- **Hardware and software development early in the construction phase will involve a series of releases with increasing functionality.**

Detector Install: FY29Q2 - FY31Q2
Cosmics: FY31Q3
Early CD-4: FY32Q4

DAQ Releases:

PicoDAQ FY26Q1
Readout test setups

MicroDAQ: FY26Q4
Readout detector data in test stand using engineering articles

MiniDAQ: FY28Q1
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics

SRO Computing (Off Project)

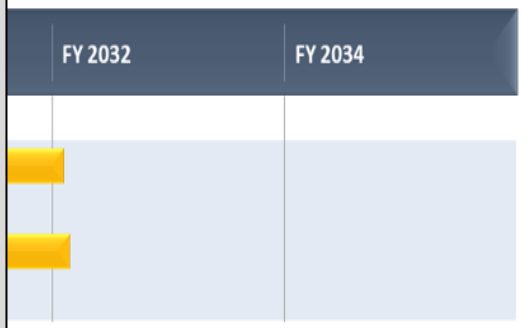
PicoDAQ
- No direct connection to DAQ.
- Stand alone testbed development:
  - Transfer / Data Management (Ruchio)
  - Orchestration / State Model (e.g. Panda)
  - Streaming Reconstruction (JANA2)
  - Calibration workflows

MicroDAQ:
- No direct connection to test stands
- Data formats defined. Data sharing

MiniDAQ:
- Data path in place, integrated data testing starts.
- Shared state model in place.
- Only Small fraction of final computer resources are in place limits full scale tests.

Full DAQ-v1:
- Full functionality DAQ ready for full system integration & testing

Production DAQ:
- Running system fully in place



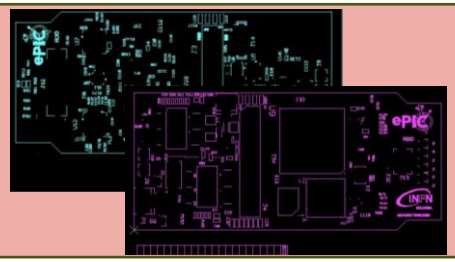
re-baseline schedule is in progress

System Component Status (Hardware)

RDO

FPGA/SFP+
- TOF Pre-prototype was used for timing studies
- TOF moved to lpGBT/VTRX+ (direct)
- Continue for Calorimeters

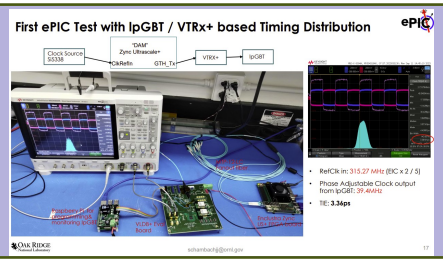
FPGA/VTRX+
- INFN Bologna for dRICH
- 12 Populated PCBs expected June
- FPGA: Artix Ultrascale+ Class



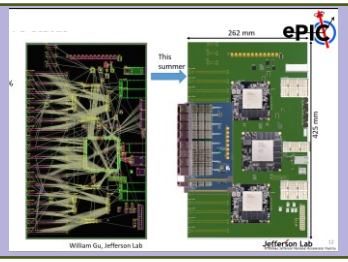
Fiber Aggregation (MAPS)
- (ITS3/AC-LGAD/others)
- lpGBT based FEBs
- Component Counts
- Pending

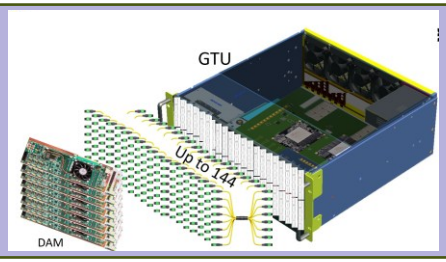
GTU

Reconstructed Clock Timing Tests:
- Mocked up with dev-kits
- < 5ps jitter measured with Ultracale+ FPGA and with lpGBT/VTRX+



Electronics Design:
- JLAB Designing
- Draft Specification
- Schematics 80%
- PCB placement 85%
- PCB routing 10%

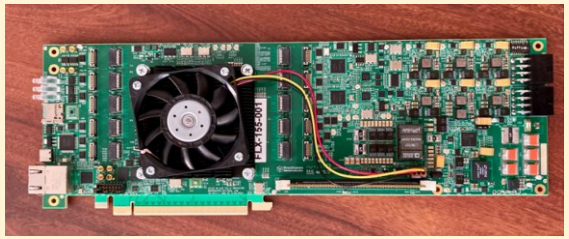




DAM

FLX-182
- Developed by ATLAS (Omega Group at BNL)
- 2 FELIX engineering articles obtained

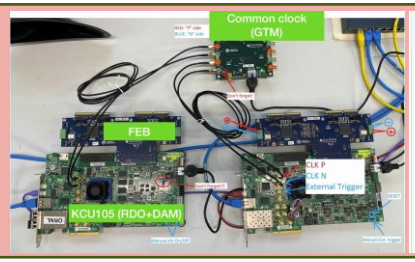
FLX-155
- Targeted for ePIC use
- Undergoing testing in Omega Group
- Test articles expected 2025

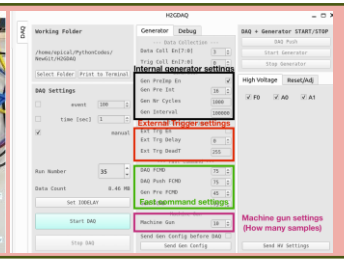


System Component Status (Collab Support)

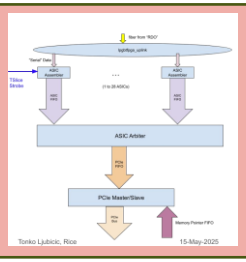
Test Setups

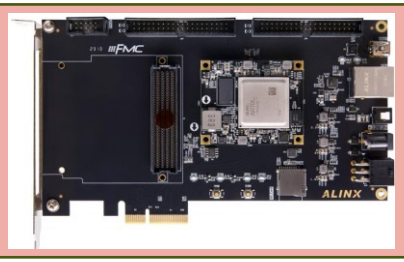
BHCAL --- (H2GCROC)
- KCU105 (RDO+DAM) (kintex)
- Python Config/Control
- rcdaq integration
- Norbert Novitzky, Miklos Czeller, Gabor Nagy, Shihai Jia, Martin Purschke



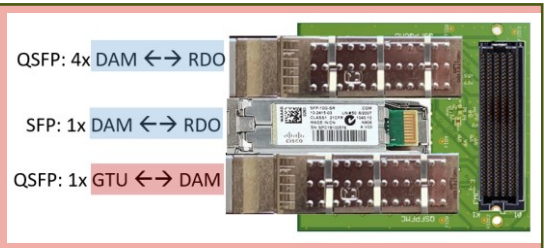


TOF DAM-Lite: (ETROC)
- Alinx AXAU15 (artix)
- Reads from lpGBT
- Follows FELIX development scheme
- (RICE)





FMC - Q(SFP) Adapter
- Stand alone (single board) GTU
- Allows use of prototype GTU with dev boards (such as AXAU15)
- 4-Boards (June)
- (JLAB)



PicoDAQ

Jan 2026
- First of O(Yearly) DAQ releases
- Documented, software & hardware
- Each release has increasing functionality

Goals
- Readout test stands
- Development Base for ePIC DAQ

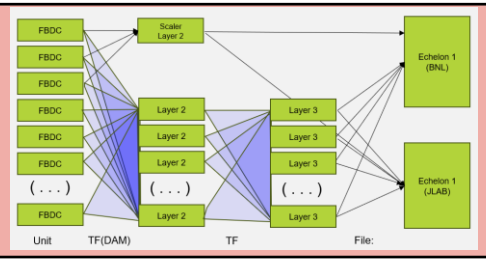
Currently defining PicoDAQ
- Target AXAU15 with FMC adapter as both RDO / DAM
- No aggregation needed but intend to provide (RDO, DAM, RDO=DAM in same hardware package)
- Ethernet communication to computer
- Will document integration tasks to incorporate new FEBs
- Control software adapted from BHCAL setup

System Component Status (Compute)

Echelon 0 Hardware / Software Components

- Run Control
- Readout
- Frame Building (2 levels)
- Data Reduction
  - Compression
  - High Level Filtering

- Logging
- Monitoring
- QA
- Configuration
- Slow Controls interface (IOC)
- Buffering and Data Transfer



Echelon 0 Software Design

Run Control Model:
- State model incorporates continuously running components (i.e.. scalers)
- "Run" structure to configure / select enabled detectors
- Slow Control status part of state model

EIC / LHC clock:
- DAM selects 39.4 MHz or 98.5 MHz
- GTU distributes 19.7 MHz to avoid phase problems when dividing clock
- Fast commands restricted to EIC bunches at multiple of 5 (2 cycles of 39.4 MHz or 5 cycles of 98.5 MHz)

Time Frames:
- 2^{16} Bunch Crossings ~ .6 ms
- Not synchronized to Bunch 0 (Minimize correlation between edge effects and spin states)
- Build all detector to each time frame
- Group O(1000) TF into Super Time Frames

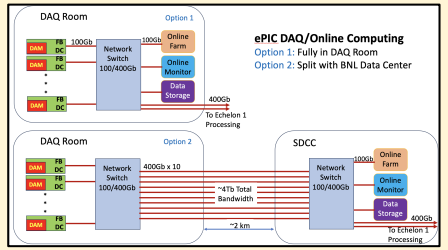
Data Banks:
- RDO / lpGBT produced data formatted but not processed produce raw data banks
- Processing (data reduction / or additional information) produces new data banks (no modification)
- Fraction of raw banks always retained

Echelon 0 location

DAQ Computing:
- ~100 Readout computers in DAQ Room
- ~100 computers located anywhere with sufficient network

Splitting farm between DAQ / SDCC:
- reduces DAQ room power/ cooling renovations
- Increases (slightly) network requirements
- Requires agreements with SDCC for access / control

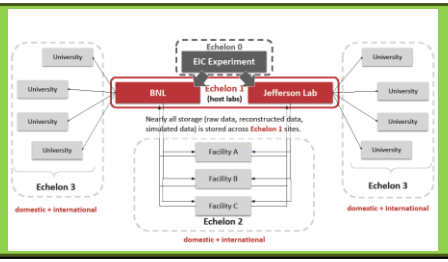
Details of splitting to be done according to cost benefit analysis



Echelon 1 Compute Interface

Streaming Readout WG (off project):
- Requirements Document Draft In Progress
- Test Beds to be developed
  - TX / Data management (e.g. Rucio)
  - Orchestration / State Model (e.g. Panda)
  - Streaming Reconstruction (JANA2)
  - Calibration workflows

Interface:
- Full Data to be streamed to JLAB/BNL echelon 1
- Full Data to be archived at both facilities for redundancy



Use Case	Echelon 0	Echelon 1	Echelon 2	Echelon 3
Streaming Data Storage and Monitoring	✓	✓		
Alignment and Calibration		✓	✓	
Prompt Reconstruction		✓		
First Full Reconstruction		✓	✓	
Reprocessing		✓	✓	
Simulation		✓	✓	
Physics Analysis		✓	✓	✓
AI Modeling and Digital Twin		✓	✓	

Integration Issues to Resolve

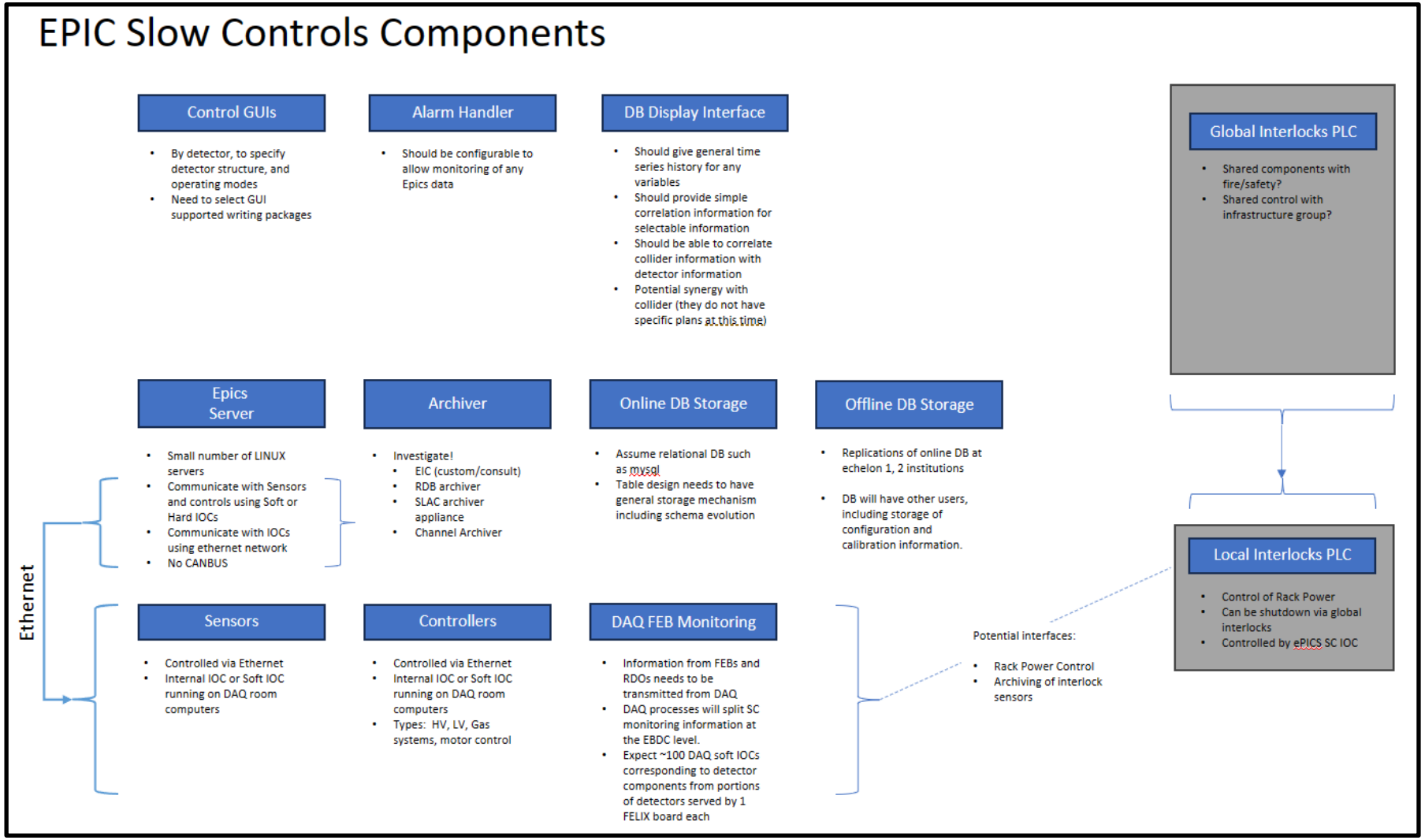
1. ePIC requires 25-30 ps timing for most sensitive detectors. This is an integration challenge.

Issue	Significance	Potential Remediation
Need clear definition of time reference requirement	Not all factors in control of DAQ	❑ Variation of calibrated, measured time of hit with respect to collision time → physics observables ❑ Need to be framed in terms of measurable requirements for each component
Jitter through GTU/DAM/RDO chain	<5 ps	✓ Timing measurements using development kits and engineering articles
Phase reproducibility on electronics restart	<5 ps	✓ Timing measurements using development kits and engineering articles
Temperature fluctuations along fiber path	IP6 historical measurements O(8K) variations estimated to produce O(30 ps) time variations	❑ TcLink implementation between DAM / RDO ❑ Continuous calibration ❑ Beam transit induced signal used by crab-cavities may be available for comparison
Temperature fluctuations within ePIC Detector	lpGBT ~5ps / K variation	❑ Detector Integration / temperature control requirements ❑ Compensation via measured temperature (lpGBT / FEB) ❑ Continuous calibration
RF Signal delivery	Basis for ePIC clock	✓ 8 ps phase stability requirement / interface has been communicated to EIC Controls
Bunch length / T0 measurement	ESR $\sigma_z = 23\ -30$ ps HSR $\sigma_z = 200 - 250$ ps	✓ T_0 Determination using vertex – simulations show 20-25 ps could be possible
Transitive Loading	Bunch dependent variations of bunch crossing time with respect to RF clock	❑ EIC guidance to estimate size of effect ❑ Calibration

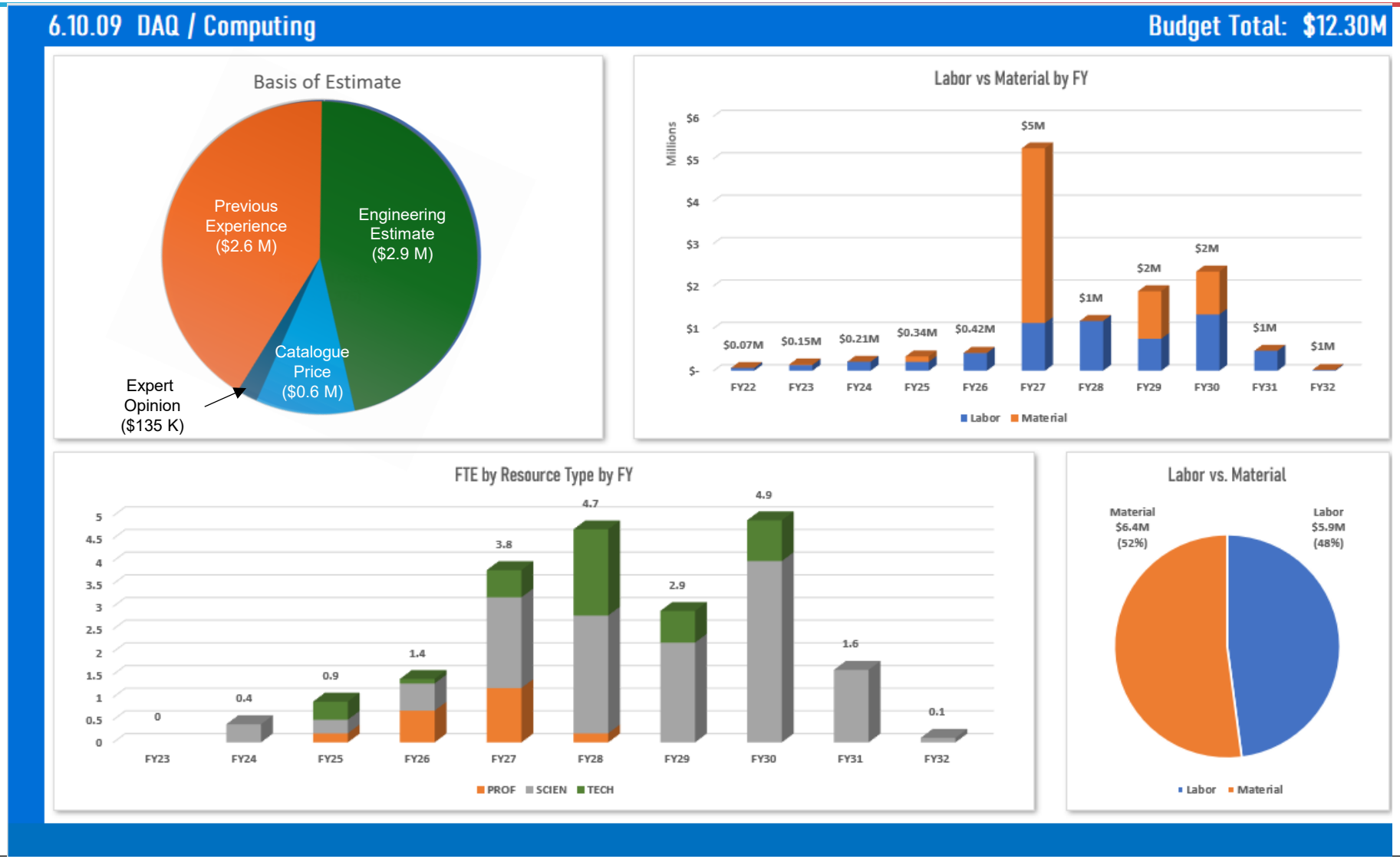
2. ASIC behavior
   - ASIC zero suppression defines front-end data volumes and affects the resource allocation for fiber/RDO counts/DAM board counts
   - Have had many discussions with ASIC developers, but do not yet have documentation for digital interfaces to final ASICs
   - Working meetings June 2-3 expected to make progress on these interfaces

Slow Controls Status

- Slow Controls Components and architecture are identified
- EPICs Base
  - Allows use of existing tools
  - Synergy with EIC Controls
- Detector DSCs have been surveyed for detector requirements
- Resource Requirements have been Documented
  - ~ 500k variables to be tracked
  - ~ 55 TB/year
  - ~ 73 Mbps network traffic
- Preliminary hardware recommendation policies / lists drafted
- PLC schemes have been investigated



Cost: WBS 6.10.09 - DAQ/Computing



ES&H and QA Considerations

ES&H

- **Custom Electronics and electronics from outside US**
  - Follow JLab & BNL procedures for equipment not certified by Nationally Recognized Test Labs (NRTL)
  - Registration and safety reviews
- **BNL experimental Safety Review Process**
  - Expect readout electronics to be part of each detector review
  - Installations will be covered by work planning process
- **Slow Controls**
  - PLC control integrated with Zero Current Detectors for electronics racks
  - Interface to detector safety interlocks TBD

QA

- **Installed fiber runs between DAQ room and WAH patch panels**
  - Testing incorporated as part of fiber termination / patch panel installation tasks
  - Test temperature dependence of phase on fraction of each lot
- **Electronics requiring QA**
  - lpGBT and VTRX+ testing part of WBS 6.03.07
  - RDO testing part of WBS 6.03.07 (6.03.08 role in RDO is with respect to the firmware)
  - DAM acceptance testing (~130 boards)
  - GTU testing part of development and production
- **Compute Nodes**
  - Compute nodes will be COTS computers subject to warrantee, and verified during installation

Outlook to CD-2

- **Resolve details of echelon 0 components in computing enclave**
  - Cost benefit analysis of DAQ room upgrades vs SDCC partitioning in progress
- **DAM production**
  - Felix model155 will be fully designed and tested during 2025
  - Plan to produce several engineering articles for DAM testing and development in 2025
  - Production is roughly aligned with Omega group production schedules but need to refine and finalize schedules / responsibilities
- **GTU project engineering design in 2025**
  - GTU engineering article to be produced prior to CD2
- **Firmware and Software development**
  - Finalize protocol definitions
  - Fully define and schedule the RDO firmware development in light of RDO variations
  - Document software & firmware components
  - Define development teams
- **Slow Controls integration**
  - Fully define scope

Outlook to CD-2

- **Resolve details of echelon 0 components in computing enclave**
  - Cost benefit analysis of DAQ room upgrades vs SDCC partitioning in progress
- **DAM production**
  - Felix model155 will be fully designed and tested during 2025
  - Plan to produce several engineering articles for DAM testing and development in 2025
  - Production is roughly aligned with Omega group production schedules but need to refine and finalize schedules / responsibilities
- **GTU project engineering design in 2025**
  - GTU engineering article to be produced prior to CD2
- **Firmware and Software development**
  - Finalize protocol definitions
  - Fully define and schedule the RDO firmware development in light of RDO variations
  - Document software & firmware components
  - Define development teams
- **Slow Controls integration**
  - Fully define scope

- **Tasks for CD-3 in backup slides**

Summary

- Detailed scope and high-level design of the ePIC DAQ is understood
- Component status varies but is progressing
  - DAM boards are selected. The FELIX board is mature technology and the updated version, FLX-155, is being tested
  - Reconstructed clock has been tested and meets requirements for both Xilinx Ultrascale+ FPGA and lpGBT implementations
  - RDO flavors are understood and being refined. Prototypes for two FPGA based RDO flavors are well advanced. Plans for lpGBT and fiber aggregators are being developed. All RDO flavors have significant similarities
  - GTU electronics design is in progress
  - Protocol design and documentation has begun and is being iterated
  - Slow Controls requirements are documented. Planning to hire to increase progress

- **Planning 60% PDR For Summer 2025 → on track for CD-2**

Backup

Tasks for CD-3 Readiness

- **Full Chain Testing with Engineering Articles**
  - Both 39.4 Mhz and 98.5 MHz systems
- **Final Design Reviews**
  - GTU
  - DAM Boards
- **Procurement Plans**
  - GTU
  - DAM Boards
- **Echelon 0 computing test beds**
  - Evaluate scalability of time frame building
- **Slow Controls Definition and Development**

ePIC Detector Scale and Technology Details

Detector System	Channels	ASIC	FEB	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking: Inner Barrel (IB)	1.8B Pixels	160	592*	24	2.36	2.36	1	ITS-3 sensors &	ASIC corresponds to VTRX+ counts
Outer Barrel (OB)	5.0B Pixels	495	1870*	55	3.52	3.52	2	ITS-2 staves / w	FEB corresponds to detector fiber
Backward Disks (EE)	4.7B Pixels	462	1744*	52	4.68	4.68	2	improvements	RDO is off detector Fiber aggregator
Forward Disks (HE)	4.7B Pixels	462	1744*	52	4.68	4.68	2		
MPGD tracking: Electron Endcap	16,384	256	64	16	2.86	0.58	1	uRWELL / SALSA	VTRX+ based FEB
Hadron Endcap	16,384	256	64	16	4.01	0.80	1	uRWELL / SALSA	
Inner Barrel	32,768	512	128	32	4.10	0.82	1	MicroMegas / SALSA	
Outer Barrel	98,304	1536	384	96	15.81	3.16	2	uRWELL / SALSA	
Forward Calorimeters: LFHCAL	63,280	1130	1130	74	18.54	2.47	2	SiPM / CALOROC	CALOROC:
HCAL insert	8k	142	142	9	17.72	2.36	1	SiPM / CALOROC	56 Ch/CALOROC
ECAL W/SciFi	18,320		574	72	14.75	7.36	2	SiPM / Discrete	16 CALOROC / RDO
Barrel Calorimeters: HCAL	1,536	28	28	2	0.87	0.12	1	SiPM / CALOROC	
ECAL SciFi/PB	5,760	102	102	4	11.45	1.52	1	SiPM / CALOROC	Discrete:
ECAL ASTROPIX	500M pixels			340	1.25	1.25	8	Astropix	32 Ch/FEB,
Backward Calorimeters: NHCAL	3,256	58	58	4	3.46	0.47	1	SiPM / CALOROC	8 FEB/RDO conservative (16 estimate).
ECAL (PWO)	2,852		102	13	2.00	0.99	1	SiPM / Discrete	
Far Forward: B0: Crystal Calorimeter	135		5	1	2.3	2.3	1	SiPM/APD / Discrete	
4 AC-LGAD layer	688,128	672	168	42	12.75	2.1	1	AC-LGAD / EICROC	4 layer x 42 module x 4 EICROC x 1024 ch
2 Roman Pots	524,288	512	128	32	14.53	2.1	1	AC-LGAD / EICROC	2 stations x 2 layer x 32 module x 4 EICROC x 1024 ch
2 Off Momentum	294,912	288	72	18	3.53	0.7	1	AC-LGAD / EICROC	2 stations x 2 layer x 18 module x 4 EICROC x 1024 ch
ZDC: Crystal Calorimeter	900		30	4	2.30	4.5	1	SiPM/APD / Discrete	
HCAL	9,216	165	165	11	0.22	.22	1	CALOROC	
Far Backward: 2 x Low Q Tagger	66M pixels	3456	288	24	37	.3	10	Timepix4	Firmware Trigger to reduce output rate
2 x Low Q Tagger Cal	3,360			1	-	-	1	SiPM / CALOROC	Low Q Calorimeter doesn't run at high luminosity
2 x Lumi PS Calorimeter	5,040			1	19	7	1	SiPM / Discrete	
2 x Lumi PS tracker	128k	1000	16	16	45	2	2	AC-LGAD: FCFD	
Direct Photon Lumi Cal	100		24	24*	200	7	1	SiPM / fADC250	Direct Photon: commercial digitizer, no RDO
PID-TOF: Barrel	2,359,296	18,432	288	-	15.95	4.79	24	AC-LGAD: FCFD	bTOF 128 ch/ASIC, 64 ASIC/RDO
Endcap	3,719,168	3,632	212	-	33.92	7.34	6	AC-LGAD: EICROC	eTOF 1024 pixel/ASIC, up to 28 ASIC/RDO
PID-Cherenkov: dRICH	317,952	4968	4968	1242	1240	13.5	30	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction Firmware trigger
pfRICH	69,632	544	68	-	24	12.5	2	HRPPD / FCFD	
DIRC	73,728	576	24	-	11	6	1	HRPPD / FCFD	

Data Bottlenecks

Detector	Channel Max Hit Rate (Hz)	Noise To RDO (gbps)	Noise Per RDO (gbps)	Noise To Tape (gbps)	RDO (max) (gbps)	RDO_max / with Noise (gbps)
SiBarrelTracker	4.13E-04	3.25	0.06	3.25	0.00	0.06
SiBarrelVertex	5.22E-03	1.15	0.05	1.15	0.17	0.21
SiEndcapTracker	2.78E-03	6.02	0.06	6.02	0.23	0.29
BackwardMPGDEndcap	2.19E+02	1.74	0.11	0.35	0.42	0.52
ForwardMPGDEndcap	4.44E+02	1.74	0.11	0.35	0.86	0.97
MPGDBarrel	8.67E+01	3.26	0.10	0.65	0.04	0.14
OuterMPGDBarrel	1.29E+01	15.23	0.16	3.05	0.01	0.17
LFHCAL	2.10E+04	10.33	0.14	1.38	1.30	1.44
HcalEndcapPInsert	6.18E+04	1.31	0.15	0.17	2.78	2.93
EcalEndcapP	1.51E+05	0.78	0.01	0.35	2.69	2.70
HCcalEndcapN	7.81E+04	0.53	0.13	0.07	2.64	2.77
EcalEndcapN	8.07E+04	0.14	0.01	0.06	1.06	1.07
HcalBarrel	1.30E+03	0.25	0.13	0.03	0.08	0.21
EcalBarrelImaging	2.92E-02	0.32	0.00	0.32	0.01	0.01
EcalBarrelSciFi	1.52E+03	0.94	0.07	0.13	2.69	2.76
TOFBarrel	1.74E+00	13.59	0.05	4.53	0.01	0.06
TOFEndcap	8.34E-01	32.13	0.15	7.14	0.07	0.22
hpDIRC	2.35E+02	3.22	0.13	1.07	0.00	0.13
pfRICH	4.99E+02	3.05	0.18	1.02	0.00	0.18
dRICH	1.09E+02	1220.94	0.98	6.10	0.00	0.98
B0 Crystal Calorimeter	2.66E+05	0.00	0.00	0.00	0.00	0.00
B0 AC-LGAD	1.72E+01	5.95	0.20	1.32	0.00	0.20
RP	3.31E+01	4.53	0.21	1.01	0.00	0.21
OM	5.93E+00	2.53	0.21	0.56	0.00	0.21
ZDC Crystal Calorimeter	7.81E+04	0.02	0.00	0.02	0.00	0.00
ZDC HCAL	3.39E+01	0.20	0.02	0.20	0.00	0.02
DirectPhoton	2.00E+08	0.00	0.00	0.00	0.00	0.00
LowQ2Tracker	8.76E+00	0.04	0.00	0.04	0.00	0.00
LowQ2Calorimeter	0.00E+00	0.01	0.01	0.01	0.00	0.01
PairSpectrometerTracker	2.44E+02	0.74	0.07	0.25	0.00	0.07
PairSpectrometerCalorimeter	3.26E+04	0.07	0.07	0.07	0.00	0.07
Total		1334.01		40.67		

Evaluated Data Bottlenecks by tiling detector regions with RDO/ASIC combos

- RDO data volume spec 8 gbps
  - Several detectors with max RDO rate ~1/4 bandwidth
  - Potential data reduction in RDO
  - Use fewer populated FEB per RDO in strategic locations
- dRICH dark currents handled by firmware trigger
- Lumi Monitoring:
  - Direct Photon Calorimeter ~100 channels direct streaming, readout only summary
  - Track lumi by bunch
- Polarimetry
  - Readout by collider DAQ, not directly by detector

Preliminary Noise Assumptions

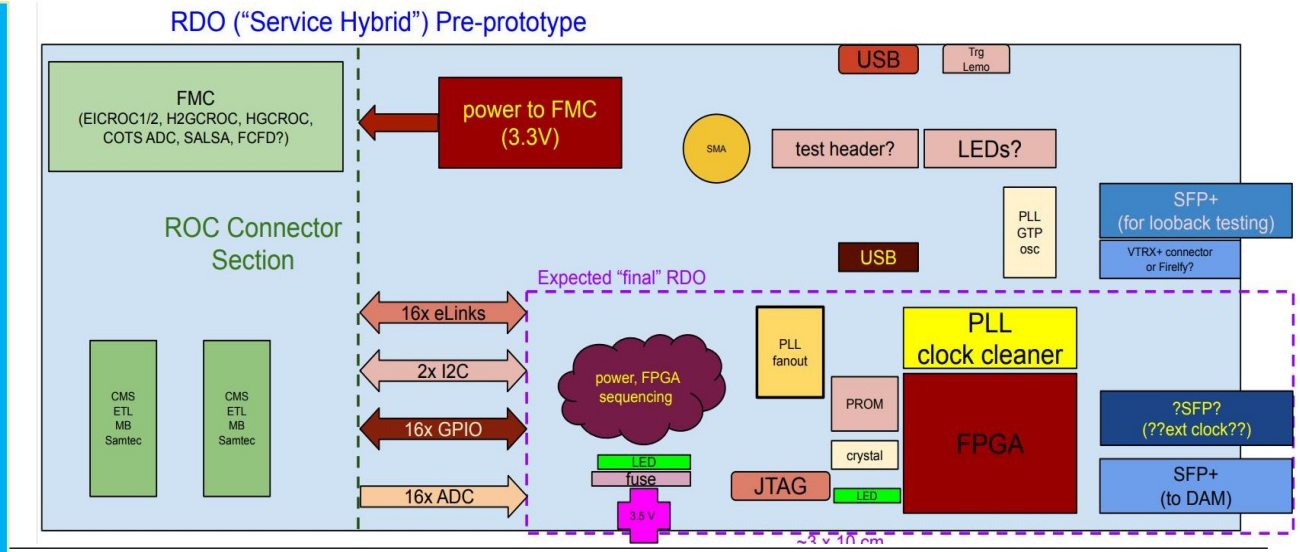
Detector	Noise (hz/channel)
ITS3	0.01
Astropix	0.01
Timepix	0.01
AC-LGAD	30
HRPPD	230
dRICH(initial)	3000
dRICH(Max)	300,000
All others	4.5σ = 340

RDO development – General plans

- The Readout Board (RDO) is the first processing interface of the DAQ with the front-end electronics/digitizers.
- There are currently 6 identified “flavors” of RDO - dependent on the detector subsystems (**see Pietro’s for dRICH example**)
- It must support both a common DAQ communication protocol as well as manage configuration and control with the different front-ends
- A pre-prototype board has been produced to support early DAQ and detector development (**See Tonko’s talk for more details**)

Readout Board Flavors

Detector	Characteristics
TOF	Highest Timing Requirement (Generic)
dRICH	Small Footprint (VTRX+ optics)
ITS-3	Detector side uses fiber (VTRX+)
Imaging Calorimeter	Integrated with ASTROPIX Sensor
Low Q Tracker	High Rates, 20 TX fibers expected / RDO
Direct Photon Calorimeter	Pure 200MHz Streaming (bypass DAQ protocol)

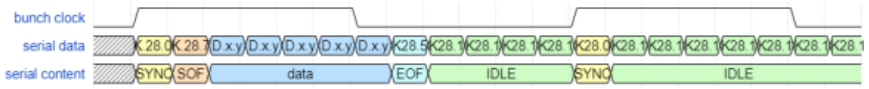


Timing Resolution with Reconstructed Clock

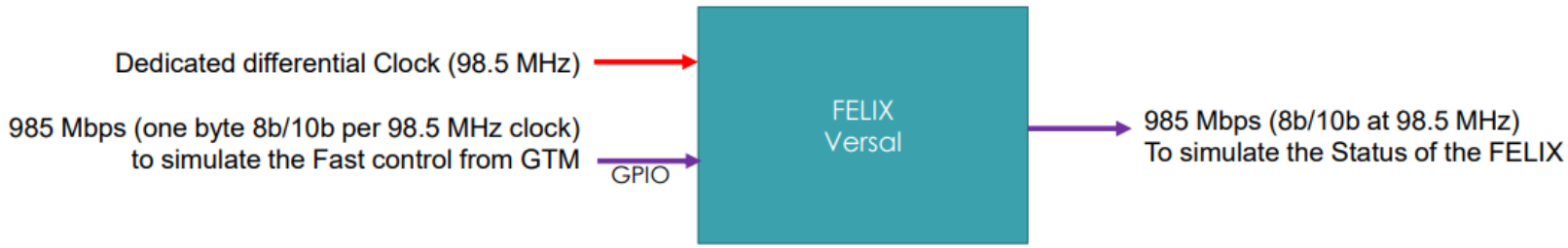
First Results (W. Gu, Jefferson Lab):

- Downlink Custom Protocol:
  - Eight bytes (8b10b) payload per Clock (98.5 MHz)
  - **7.88 Gbps** line rate (6.304 Gbps payload rate)
  - Clock embedded transmission via **GTH** transmitter
- **GTY** Clock recovery works OK
  - The TIE (σ) is below **4ps**
  - Phase is stable, recovered clock reproduces the original (GTH_Ref) Clock
- A **Clock Jitter Cleaner** further improves recovered clock with a TIE (σ) below **2ps**
- Future Tests: Use (Versal based) FELIX prototype

Encoding:



7.88 Gbps line rate
Eight 8b/10b payload per clock (98.5 MHz) equivalent (downlink)
control words: 6.304 Gbps
Control symbols as frame delimiters, BC markers, and IDLEs

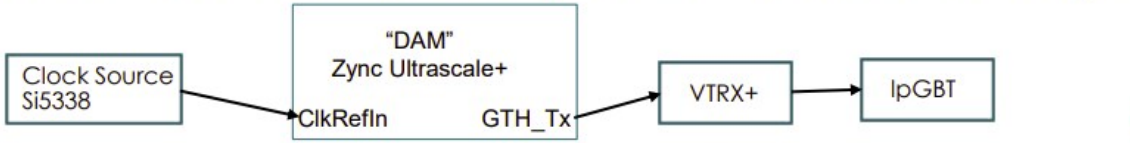


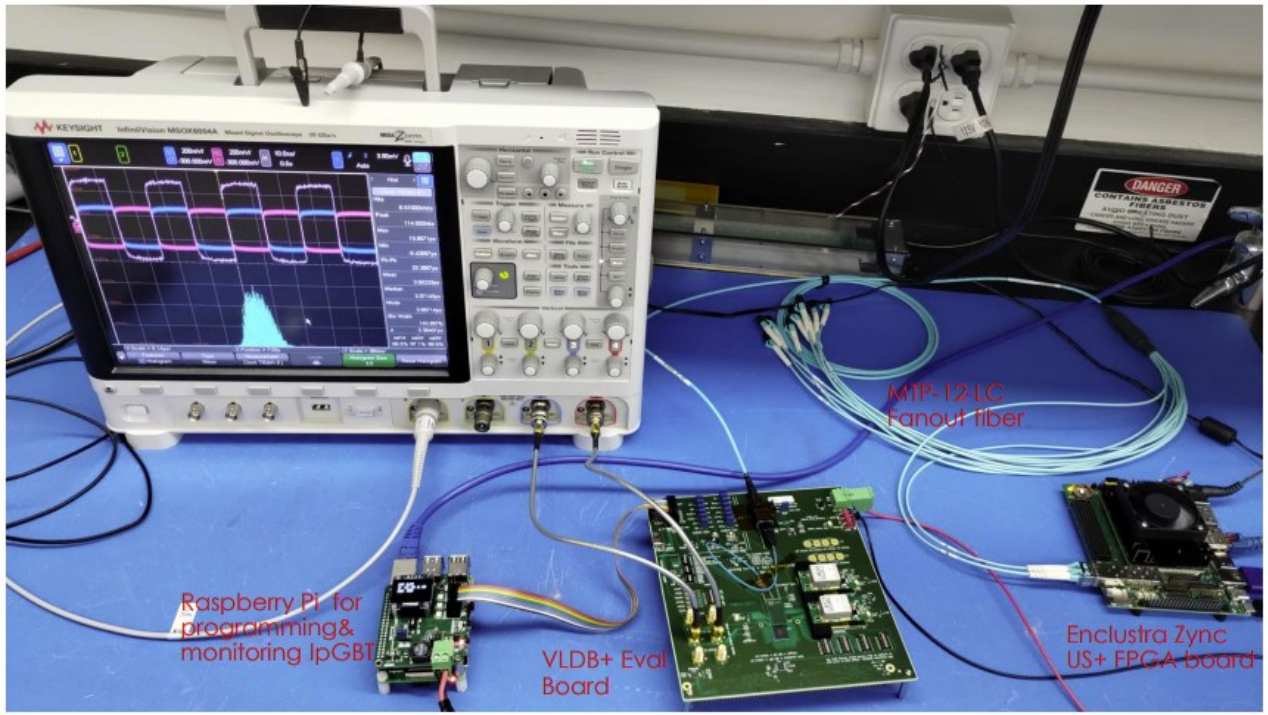
OAK RIDGE National Laboratory
schambachjj@ornl.gov

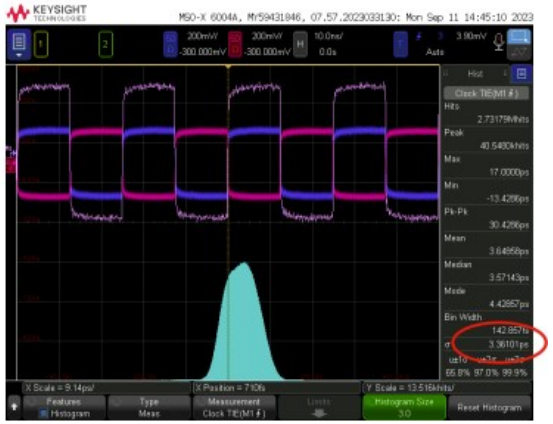
16

Timing Resolution with Reconstructed Clock

First ePIC Test with lpGBT / VTRx+ based Timing Distribution





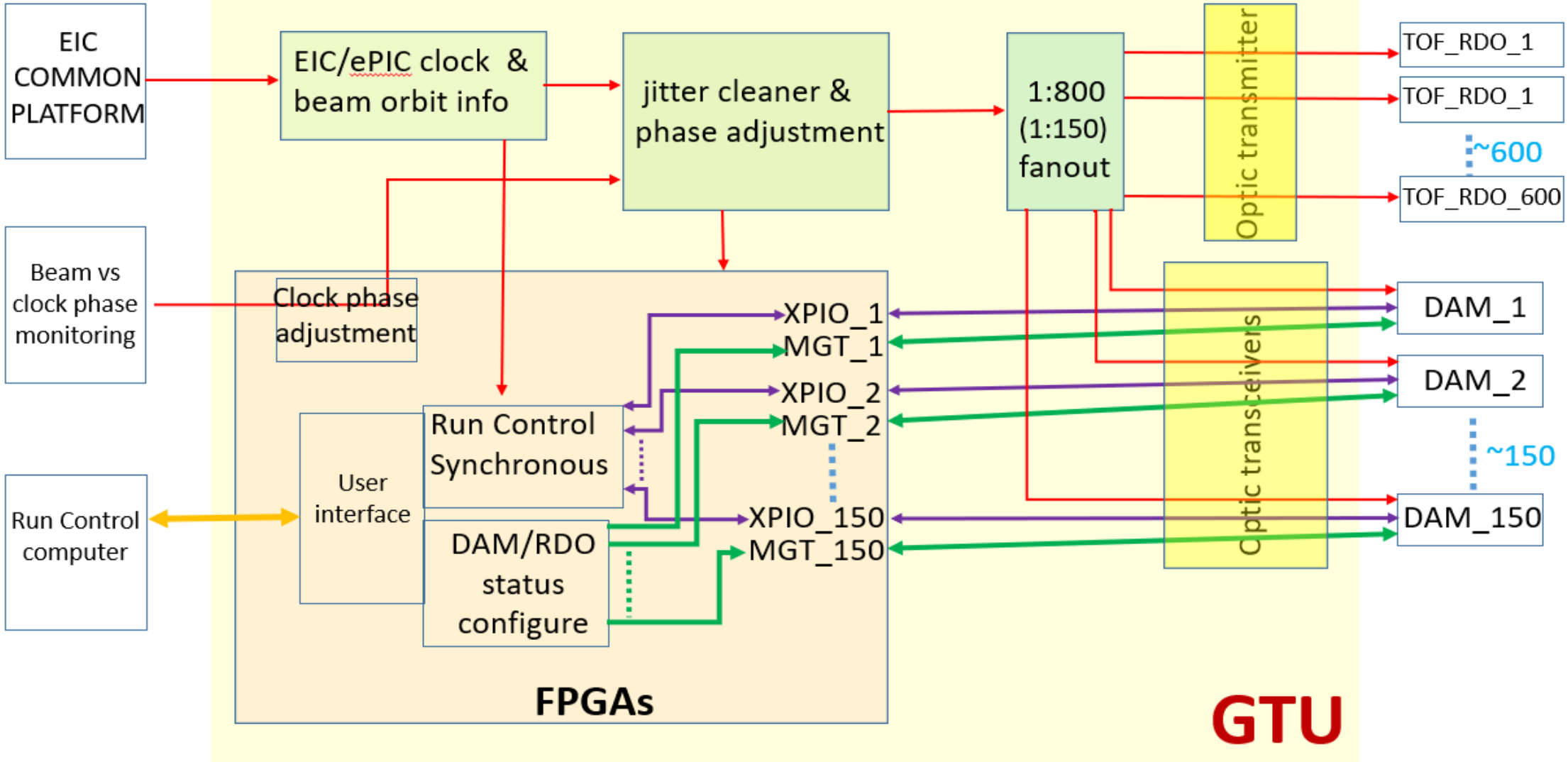


- RefClk in: 315.27 MHz (EIC x 2 / 5)
- Phase Adjustable Clock output from lpGBT: 39.4MHz
- TIE: **3.36ps**

OAK RIDGE National Laboratory
schambachjj@ornl.gov

17

GTU Design: functional diagram

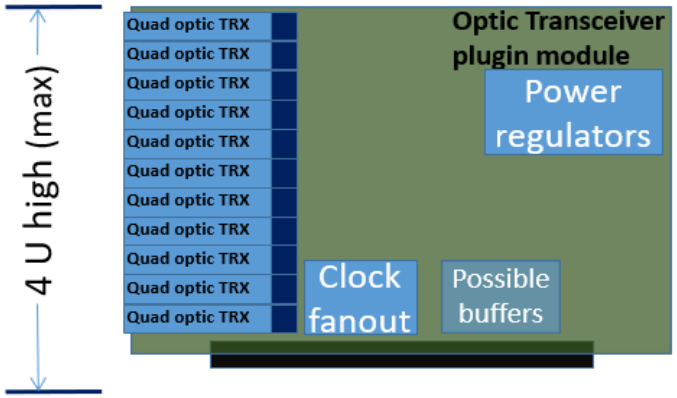


GTU Design

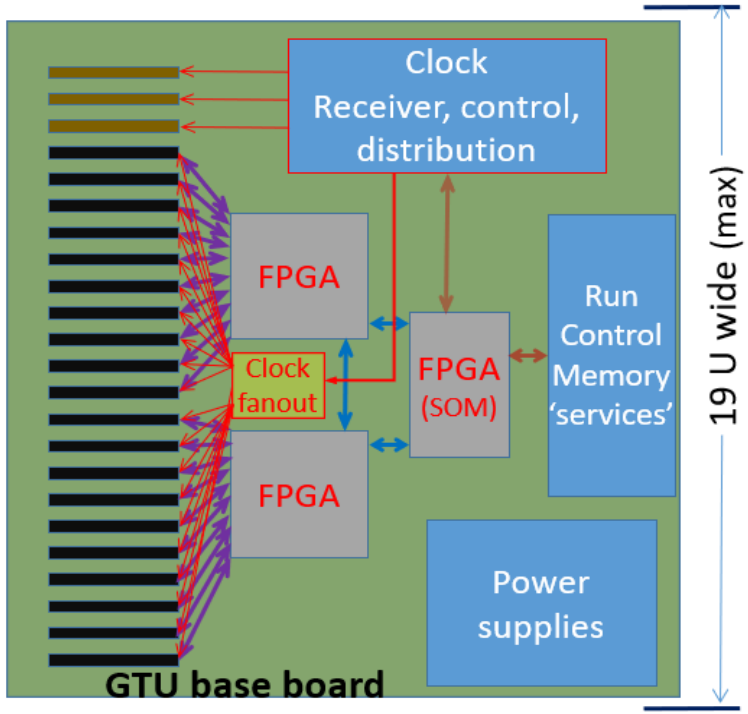
3. GTU design: modular design, a 4U(high) x 19U(wide) rack mounted box

GTU base board
Optic transceiver plugin modules (to DAM)

Fits in a 19U wide rack
Takes 4U high space
MTP fiber ports to DAM



Possible choice of Optic Transceivers:
QSFP, Finisar FTL410Q, 40GBASE-SR4
Possible choice of plugin connector: PCIe5x16

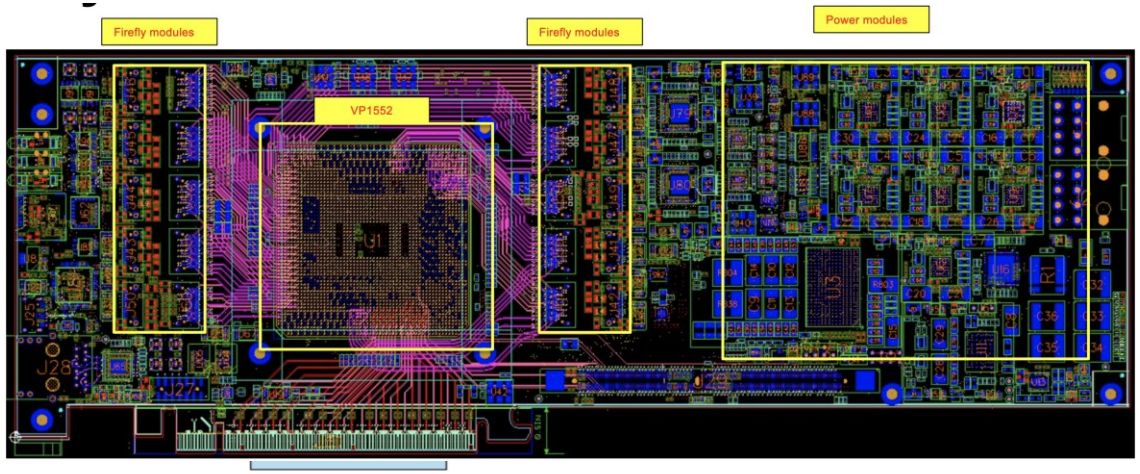


- All the electrical signals are differential signals (PCB and connector)
- The FPGA can be a single piece, or three pieces with fast interconnect.

FELIX Updates – FLX-155

- FELIX (Front-End Link Exchange) hardware for future ATLAS experiments at HL-LHC is being developed at BNL (Omega Group)
  - Long term support is insured. Development timelines are compatible with EIC.
  - ePIC is collaborating with Omega to use this design as our DAM board.
- Latest (FLX-155) design review completed by ATLAS and AMD
  - It has been sent out for fabrication. PCBs available by July.
- First 4 populated boards expected by late August/early September
  - We expect to receive at least one board by the end of this year

- Versal Premium: XCVP1552-VSVA3340
- Support PCIe Gen4 x16, 2 Gen5 x8
- 48 FireFly data links (10/25 Gb/s)
- 4 LTI links (10/25 Gb/s)
- 100GbE (4*25Gb/s)
- DDR4
- GbE
- White Rabbit
- Electrical IOs (single-ended)



Note: 4 fiber LTI Link supports receiving either reconstructed or a direct clock

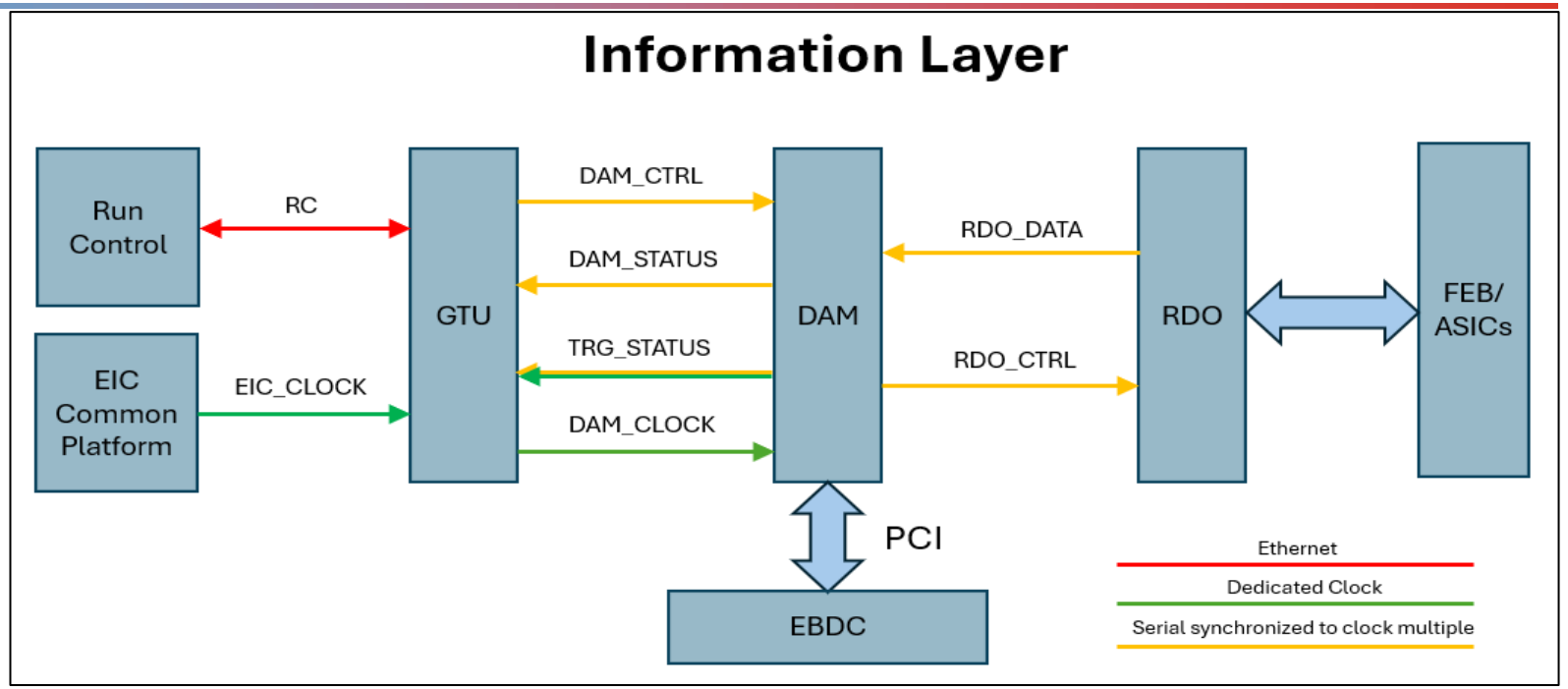
Versal FPGA is a SoC (Dual Core ARM) and can operate either standalone or in a Server

Fiber Protocol / DAQ operation

Synchronous Commands:

64 bits (80 bits 8b/10b encoded) per bunch

- Reconstructed clock
- Redundant BCO
- Distinct synchronous commands (eg)
  - RC
  - Time Frame Control & Definition
  - Flow Control
  - Trigger
    - Request special events
    - Data filter (firmware trigger)
  - Configuration (ASIC / RDO firmware)
  - Data Formatting
  - Data Transfer
    - Hits
    - Slow Controls



Trigger Operation:

- Support Max Data Volume to DAM / Readout computer Buffers
- Generate Trigger Signals in DAM
- Communicate triggered crossings via synchronous cmds through GTU

Time Frame Definition:

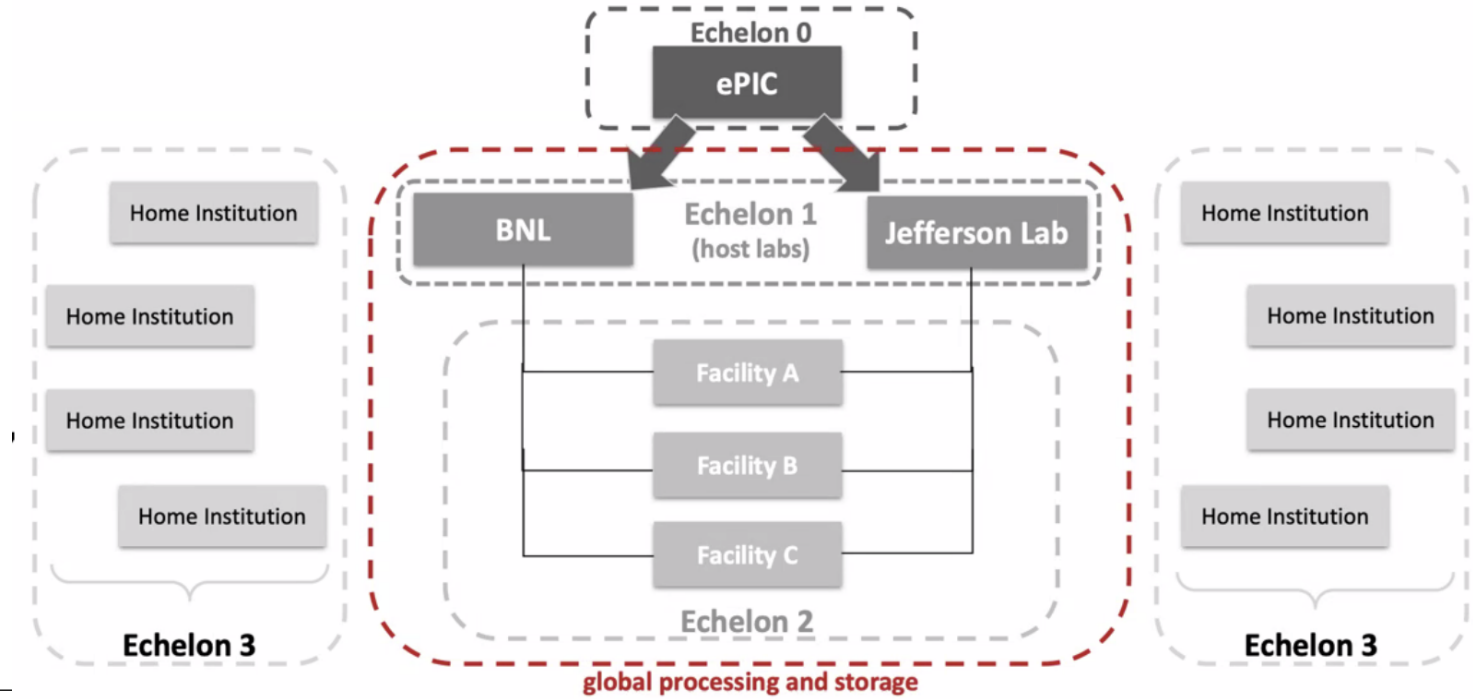
- 16 bits BCO (0.66ms -> 8MB @ 100Gbps)
- Flexible formatting
  - Filtered & Unfiltered data can coexist
- Time Frames are built, they contain the full set of detectors for the time period
- Tiered Data Format.
  - High level flexible, named navigation via banks (e.g. star SFS, sPHENIX DAQRC)
  - Low level supports direct, detector specific (eg ASIC) formats.

Boundary between Online and Offline

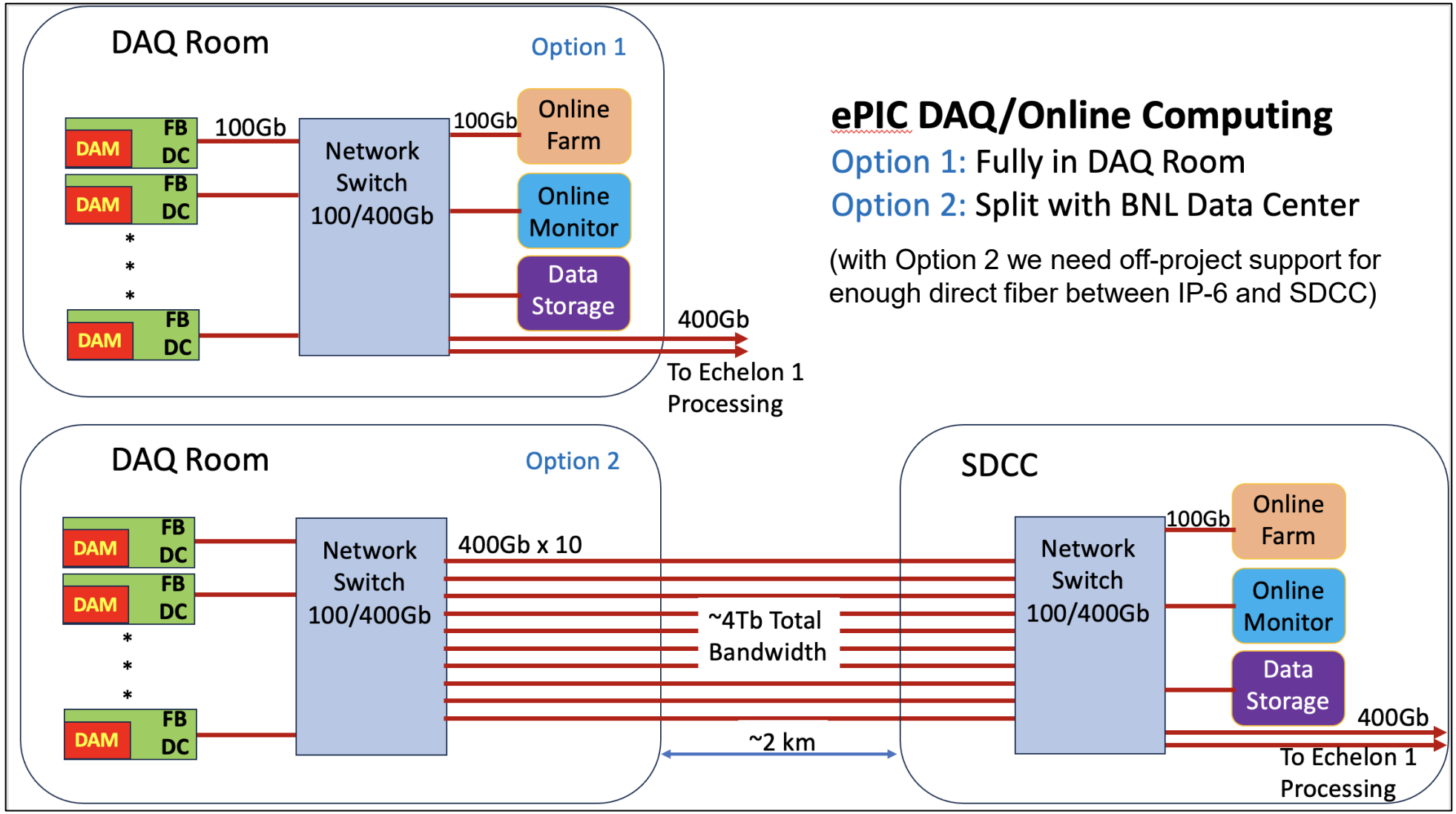
- The streaming architecture allows for some blurring of the offline and online processing with respect to calibrations, QA monitoring, and potential seed analysis to improve reconstruction turn around. These aspects are not yet fully specified.
- Require an interface to allow sharing of code between offline / online processing
- Local buffering (Echelon 0) provides elasticity in the transfer of data to computing facilities
- Offline buffering (Echelon 1) will allow several weeks for calibration and reconstruction.

ePIC Scientific Computing

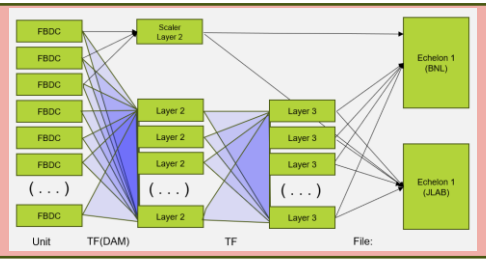
- Is a dependency for the project handled in conjunction with host labs.
- The Resource Review Board (RRB) looks at the international detector and computing resources.
- The ePIC computing groups are actively implementing scientific software as well as working with the DAQ to define the interface with the streaming DAQ system.

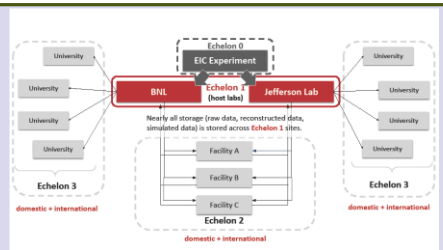
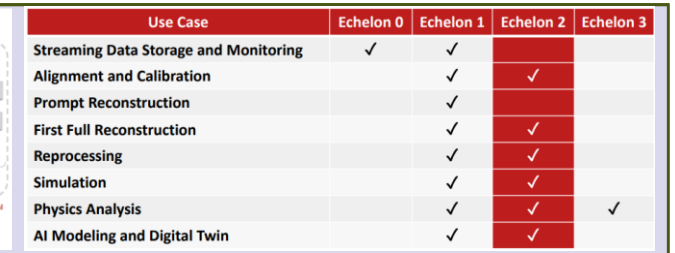
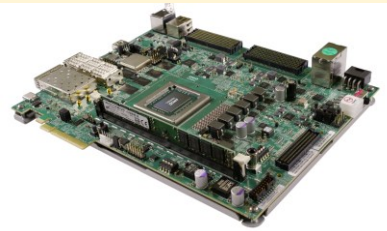


Echelon 0 Computing Options



System Components Status

Echelon 0 Compute	• Readout Computers
	• Frame Building Computers
	• Data Reduction
	  • Filters
	  • Compression
	  • High Level Triggering
		• DAQ Logging
		• DAQ Monitoring
		• DAQ QA
		• Configuration / Run Control
		• Slow Controls interface (IOC)
		• Buffering and Data Transfer
			

Echelon 1 Compute Interface	Interface: • Full Data to be streamed to JLAB/BNL echelon 1 • Full Data to be archived at both facilities for redundancy	Scientific software and computing is off project dependency: • RRB • ECSJI • Latest Collaboration Review Sept 26-27, 2024	
			
Detector Test Support	Firmware Support for Commercial Development Boards as FELIX substitutes for test stands (to be developed)	2 Port VD100 ($800)	
		48 port VMK180 ($10k)	
Echelon 0 location	DAQ Computing: • ~100 Readout computers in DAQ Room • ~100 computers located anywhere with sufficient network	Splitting farm reduces DAQ room renovations but increases network requirements, space in SDCC, and complicates access	Cost/benefit analysis to be done

Response to Recommendations (PDR not DOE…)

Review+A1:I560	Date of Review:	DOE Review (Y/N)	Recommendation	Response	Action Taken	Status	Updated
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	Include a dedicated overview and discussion on the slow-controls in a subsequent review	Agreed	The plan for the slow controls will be documented and presented in the next review.	in progress	9/2/2024
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	To achieve the next level of maturity of the RO/DAQ architecture & based on the experience of recent experiment upgrades, recommend the following steps: oFix the definition of protocol between DAM & RDO. oThe general architecture of the command (and trigger) distribution from GTU to DAMs/RODs must be developed and specified further. oThe trigger (foreseen as a mitigation of excessive data volume) is not yet mature and may introduce as yet unforeseen complications. This should be developed. oDefine the performance requirements of DAQ systems at different stages of the development. oDefine the DAQ/control requirements from sub-detectors from the perspective of testing and validation. This was an important step during the evolution of the recent upgrades at the LHC. oIf many variants of RDO and or DAMs are indeed required, the division of responsibilities should be discussed and clarified. Central support must be properly resourced. This was massively underestimated in recent LHC upgrades. oPlans to evaluate techniques to reduce data volume should be developed in data challenges, as they might have large impact on the data rate and performance of the DAQ system. oA table showing how many DAM boards and readout server are assigned to each detector should be provided for completeness. oDataflow from the FEE to the STORAGE must be better described	Agreed	The first three bullets will be addressed by the development and agreemend upon a detailed protocol document describing the GTU/DAM/RDO communication. A draft has been produced, but many aspects of it are still under discussion. The following two relate to DAQ support of detector development. This is the subject of discussion at the next collaboration meeting, and will be documented following that meeting. We agree that the RDO variant responsibilies do need to be clarified, and we also need to ensure that common firmware and hardware aspects are shared. The table mapping DAM boards to readout servers can be produced from currently existing information, and will be shown in the next review. Finally, the DAQ computing farm specification and development will lead to data challenges and specification of the Echelon 1 storage, in conjunction with the ePIC computing groups.	in progress	9/2/2024
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	Documentation of interfacing between RDOs and DAMs should be finalized, from the perspective of both DAQ and controls	Agreed	An initial draft of the of the GTU/DAM/RDO protocol document has been written and aspects of it are under discussion and will be further developed.	in progress	9/2/2024
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	For RO/DAQ, we recommend the outstanding protocol definitions to be fixed to allow progress, as well as the clear definition of responsibilities, synergies and sharing	Agreed	An initial draft of the of the GTU/DAM/RDO protocol document has been written and aspects of it are under discussion and will be further developed.	in progress	9/2/2024
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	We strongly recommend a clearer definition from the sub-detectors of their DAQ/control needs and quantities, and how these develop in time (short-term for prototyping and long-term for scaling up of the sub-systems)	Agreed	This is the subject of discussion at the next collaboration meeting, and will be documented following that meeting.	in progress	9/2/2024

Response to Recommendations

Review+A1:I560	Date of Review:	DOE Review (Y/N)	Recommendation	Response	Action Taken
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	Include a dedicated overview and discussion on the slow-controls in a subsequent review	Agreed	The plan for the slow
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	To achieve the next level of maturity of the RO/DAQ architecture & based on the experience of recent experiment upgrades, recommend the following steps: oFix the definition of protocol between DAM & RDO. oThe general architecture of the command (and trigger) distribution from GTU to DAMs/RODs must be developed and specified further. oThe trigger (foreseen as a mitigation of excessive data volume) is not yet mature and may introduce as yet unforeseen complications. This should be developed. oDefine the performance requirements of DAQ systems at different stages of the development. oDefine the DAQ/control requirements from sub-detectors from the perspective of testing and validation. This was an important step during the evolution of the recent upgrades at the LHC. oIf many variants of RDO and or DAMs are indeed required, the division of responsibilities should be discussed and clarified. Central support must be properly resourced. This was massively underestimated in recent LHC upgrades. oPlans to evaluate techniques to reduce data volume should be developed in data challenges, as they might have large impact on the data rate and performance of the DAQ system. oA table showing how many DAM boards and readout server are assigned to each detector should be provided for completeness. oDataflow from the FEE to the STORAGE must be better described	Agreed	The first three bullets protocol document de but many aspects of it detector developmen will be documented need to be clarifi are shared. The table existing information, specification and dev storage, in conjunctio
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	Documentation of interfacing between RDOs and DAMs should be finalized, from the perspective of both DAQ and controls	Agreed	An initial draft of the it are under discussio
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	For RO/DAQ, we recommend the outstanding protocol definitions to be fixed to allow progress, as well as the clear definition of responsibilities, synergies and sharing	Agreed	An initial draft of the it are under discussio
Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics	June 10-11, 2024	No	We strongly recommend a clearer definition from the sub-detectors of their DAQ/control needs and quantities, and how these develop in time (short-term for prototyping and long-term for scaling up of the sub-systems)	Agreed	This is the subject of following that meetin

More Development needed!
- Slow controls based on EPICS
- Preliminary Counts of components/Variables/Frequencies
- Preliminary list of “recommended/supported” equipment
- Plan to hire

Summary of recommendations:
- Document detailed protocols/algorithms to make the full system work
  - Electronics (GTU → DAM → RDO → FEB)
    - Configuration, SC monitoring, Triggering, Flow Control, Special running modes
  - Computing (Time Frame Building, Logging Monitoring, QA, Data Reduction, Data Formats, Data Sinking)

Response:
- This is a significant current effort
- Preliminary protocol document drafted but evolving
- Initial GTU design effort (conceptual -> detailed)

Risk Mitigations
- High Data Volume due to Dark Currents in dRICH
- Noise/Background

Response
- Efforts to study backgrounds (Synchrotron Radiation Continuing)
- Bandwidth for front ends / firmware trigger protocol iteration

Strategy:
- Further define “release schedule” of firmware / software
- Recommended supported development kits for DAM components
- Generic RDO (TOF pre-prototype FPGA based RDO)
- DAQ will provide services but detailed development/test plans for 24+ detectors outside of current DAQ scope