Status of Ancillary ASIC Design

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10th EIC DAC Review
June 11th – 13th, 2025

Introduction

SVT Silicon Scheme

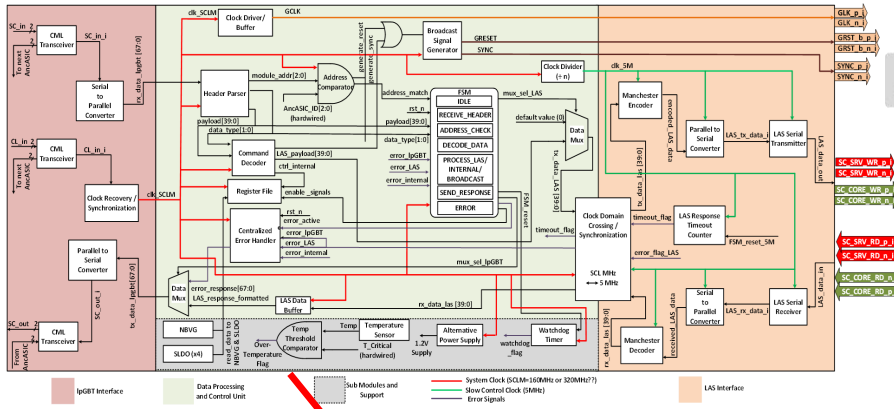
- Plans
- Why AncASIC?

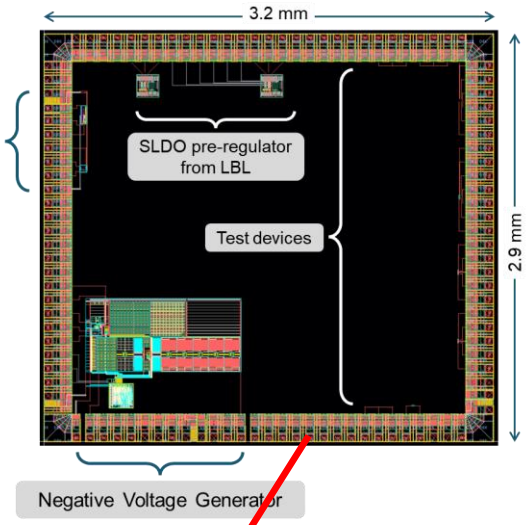
Design Overview

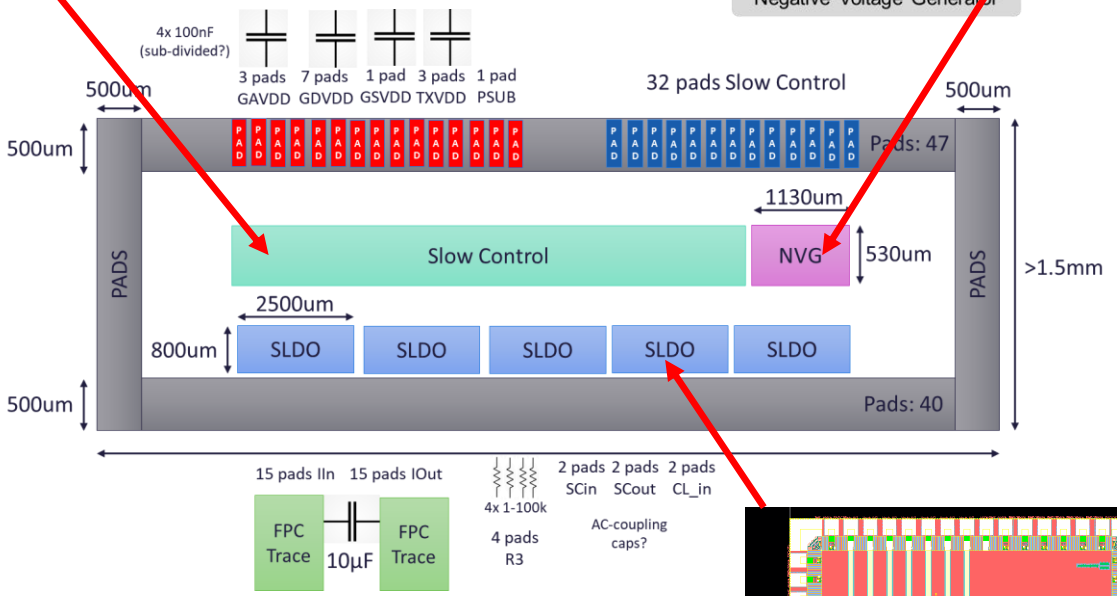
- Technology Selection
- Shunt LDO
- Negative Voltage Generator
- AncBrain
- Overview

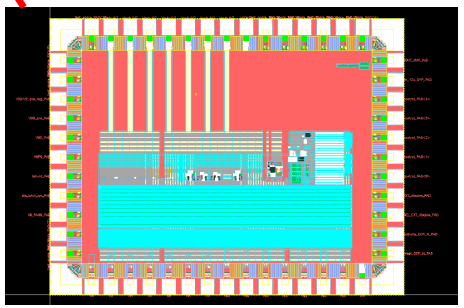
Progress, Next Steps and Ongoing Challenges

- Progress to date
- Current work and future plans
- Ongoing challenges









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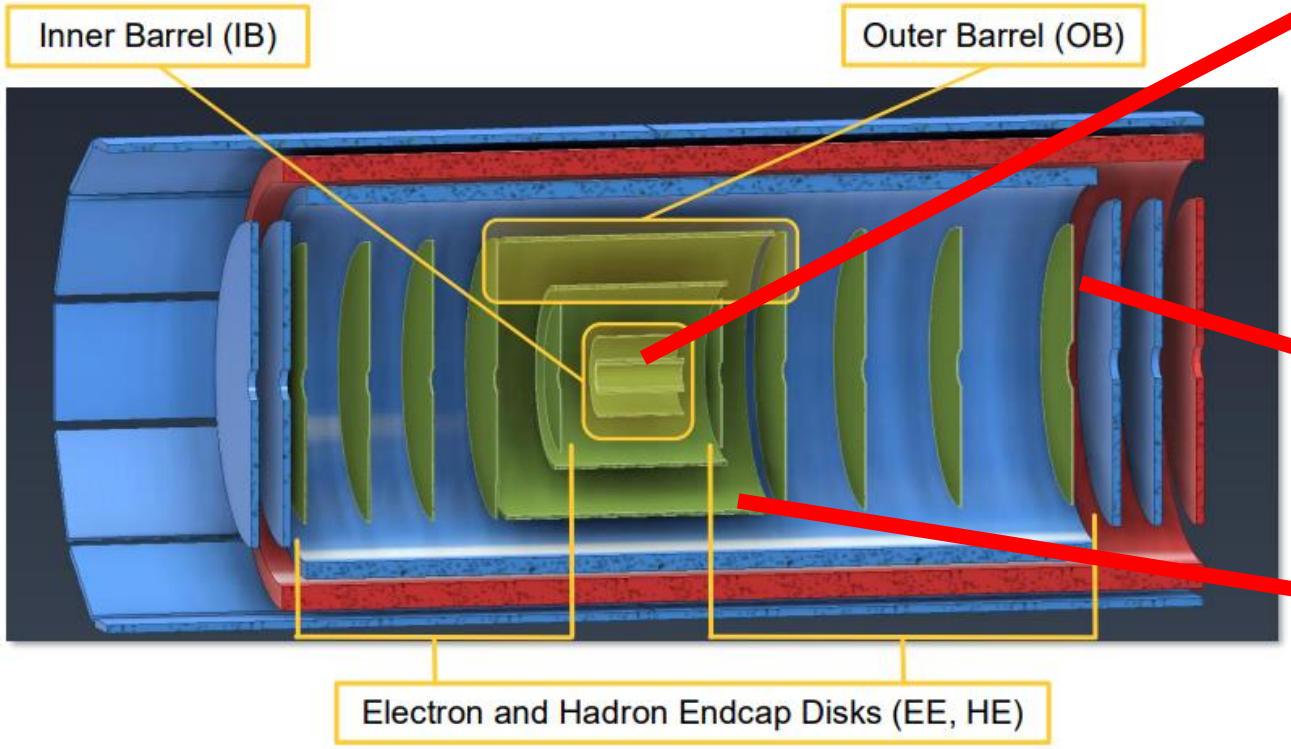
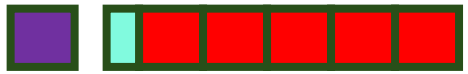
Introduction
SVT Silicon Scheme



Inner Barrel

- Thinned silicon bent around beampipe
- Use wafer-scale MOSAIX from ITS3

Outer Barrel and Discs



- Smaller Version of MOSAIX with minimum necessary changes (EIC-LAS)
- Supporting AncASIC

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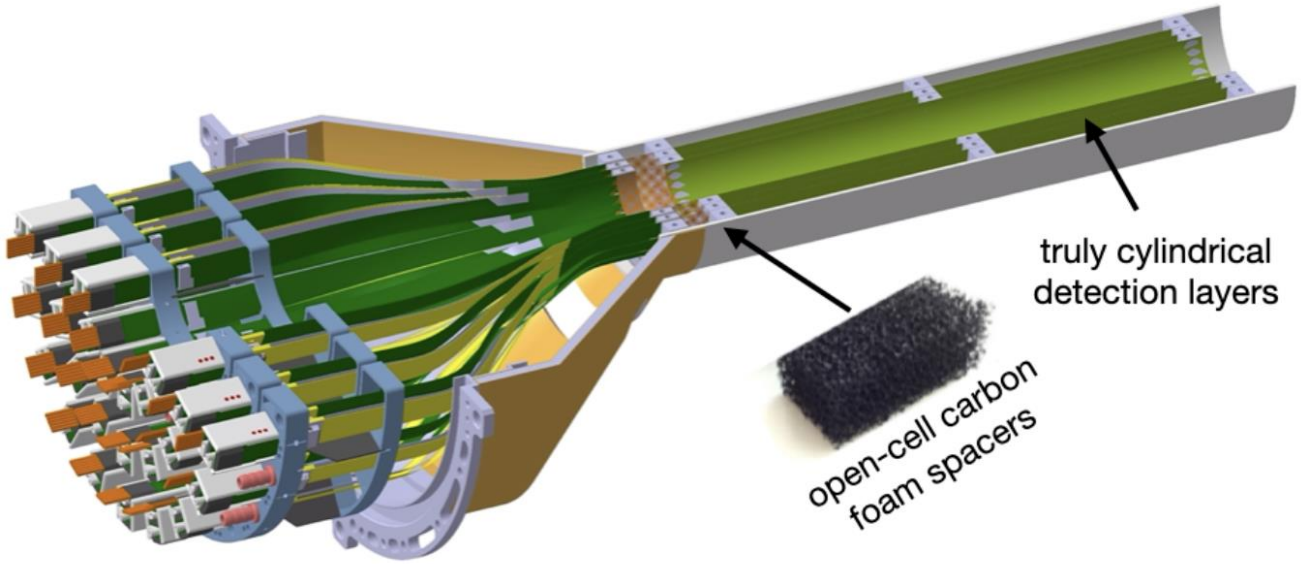
Ancillary ASIC

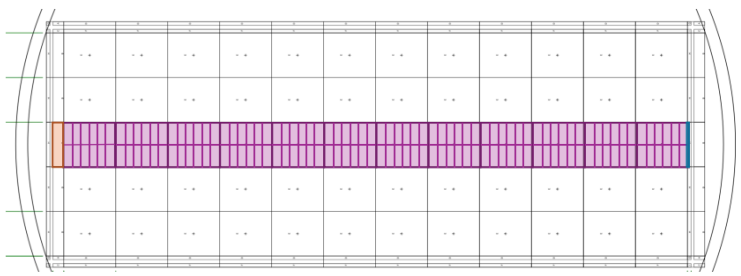
Why AncASIC?

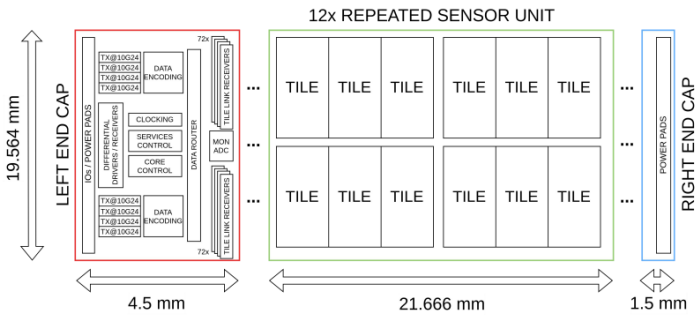
- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control
  - Point-to-point powering
  - Precise negative back bias
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency
- For these reasons, develop supporting ASIC instead



https://ep-news.web.cern.ch/content/alice-its3-clears-major-milestone

MOSAIX





https://indico.cern.ch/event/1381495/contributions/5988486/attachments/2869319/5164357/TWEPP2024.PVL.v11.pdf

Ancillary ASIC

Why AncASIC?

- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control → Serialised Slow Control interface from EIC-LAS to lpGBT
  - Point-to-point powering → SLDO for serial powering
  - Precise negative sensor bias → Local Negative Voltage Generator
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency

→ Develop independent supporting chip
  - Development decoupled from MOSAIX availability
  - No modification of MOSAIX needed
  - 110nm XFAB process
    - 4 MPW runs a year
    - Cost effective
- For these reasons, develop supporting ASIC instead

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Ancillary ASIC

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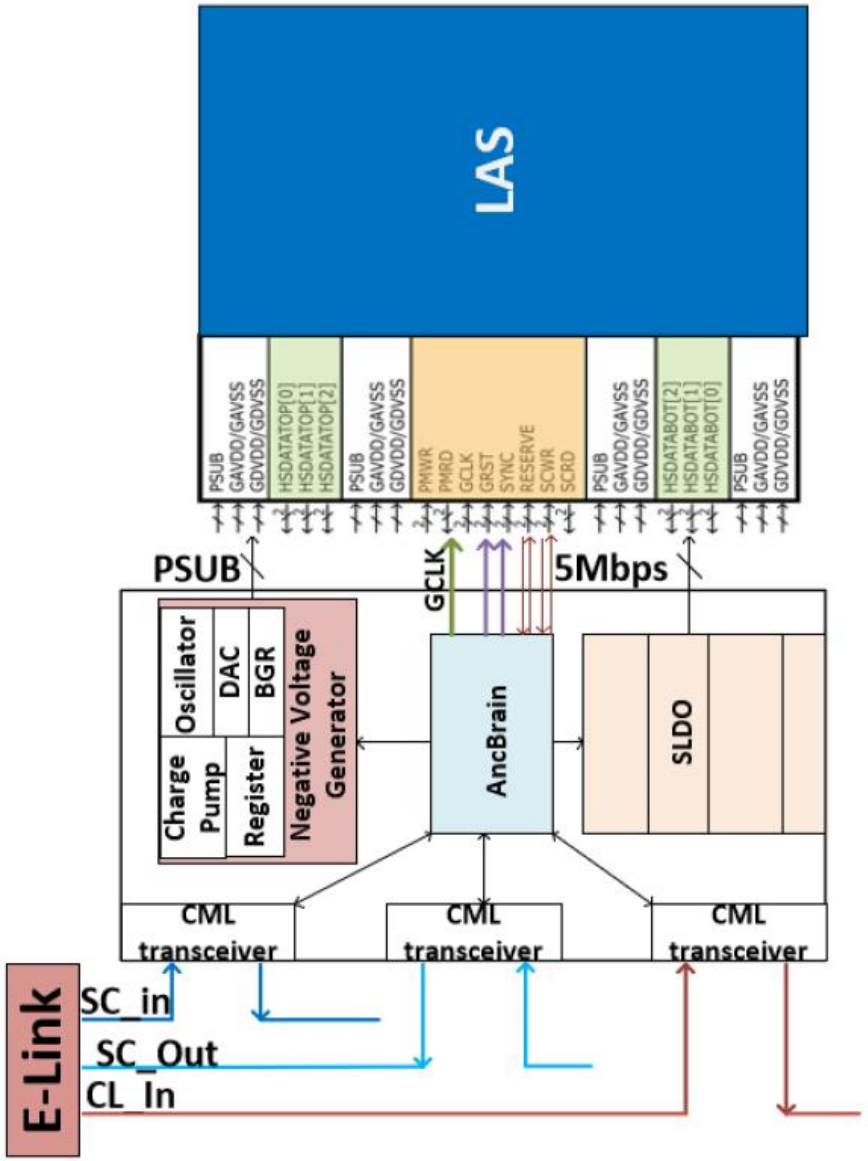

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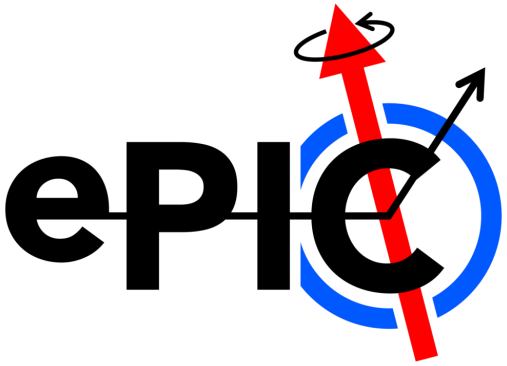

Design Overview

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Technology Selection

XFAB XT011

- 110nm BCD-on-SOI Technology
  - SOI – permits floating grounds for negative voltage generation
  - Thick copper top layer – very low resistance for power dissipation
  - High gate density – suitable for AncBrain
  - All design sites have experience with XFAB
  - Radiation hardness untested
    - ePIC radiation requirement low [1]
    - Derived from a previously tested technology [2]
    - Test structures in fabrication

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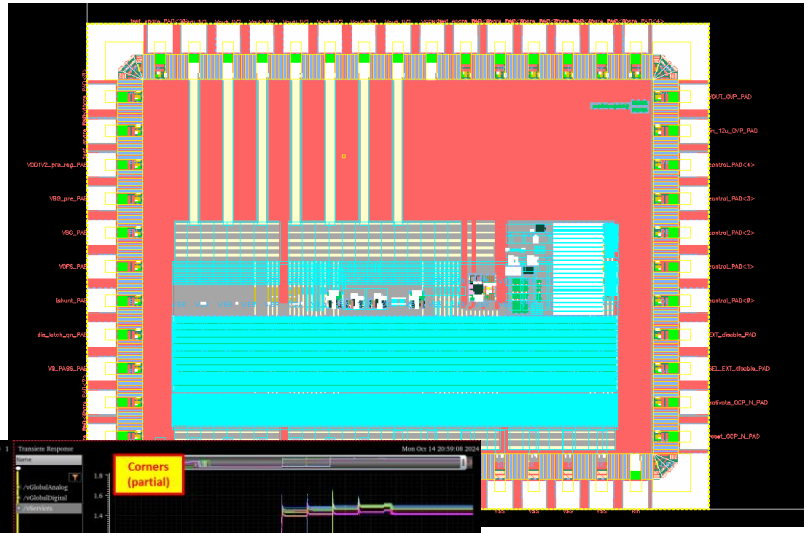
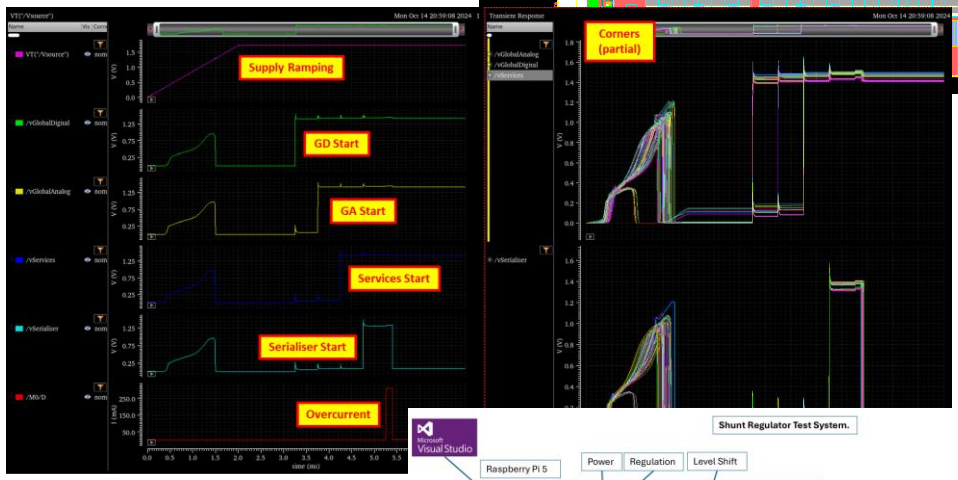
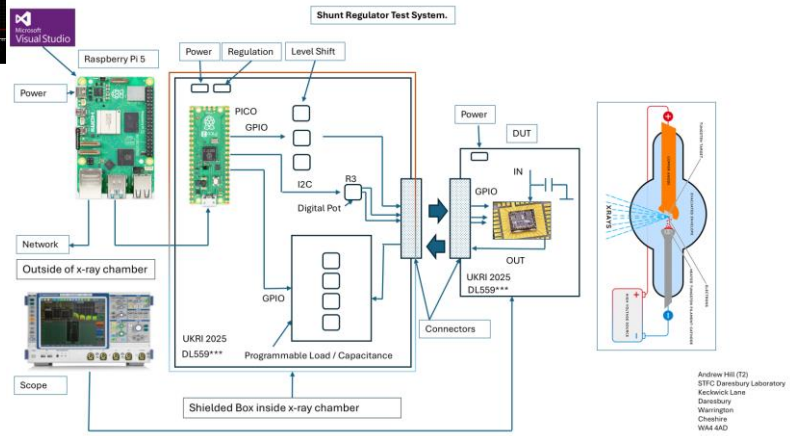
Shunt LDO

SLDO

- Serial powering required for services reduction
- Reviewed with external participants
- SLDO test structure (including pre-regulator) submitted March 2025 (UK funded, submitted via Europractice)
- Expected back September 2025
- Test system in preparation







Prototype currently in fabrication!

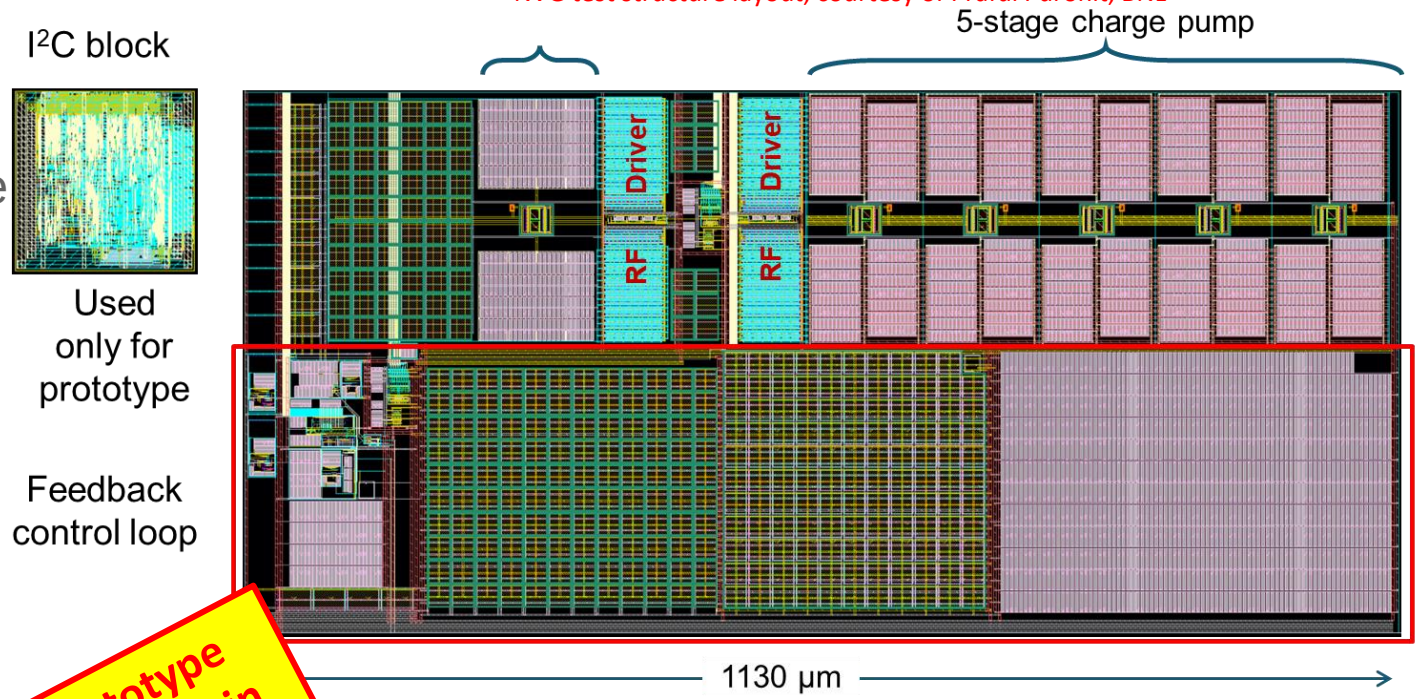
SLDO Test System Plan, courtesy of Andrew Hill, UKRI-STFC Daresbury Laboratory

Negative Voltage Generator

NVG

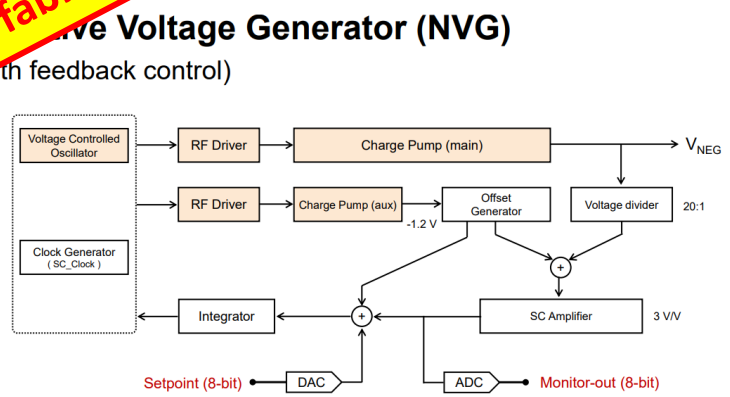
- Local generation of sensor bias voltage needed due to combination of serial powering and low bias level (~1V)
- Reviewed with external participants
- Test structure submitted March 2025
- Also included transistor test structures and other blocks
- Expected back September 2025
- Test system in preparation

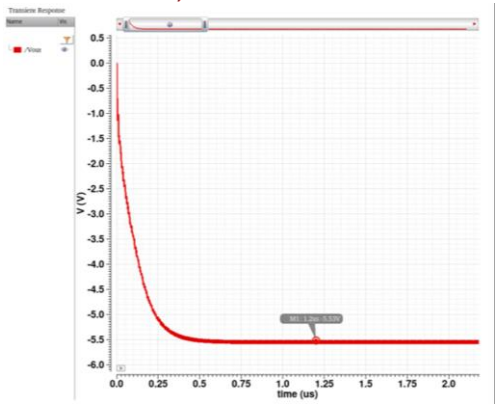
NVG test structure layout, courtesy of Praful Purohit, BNL



Prototype currently in fabrication!

* Size (not including the I²C block)





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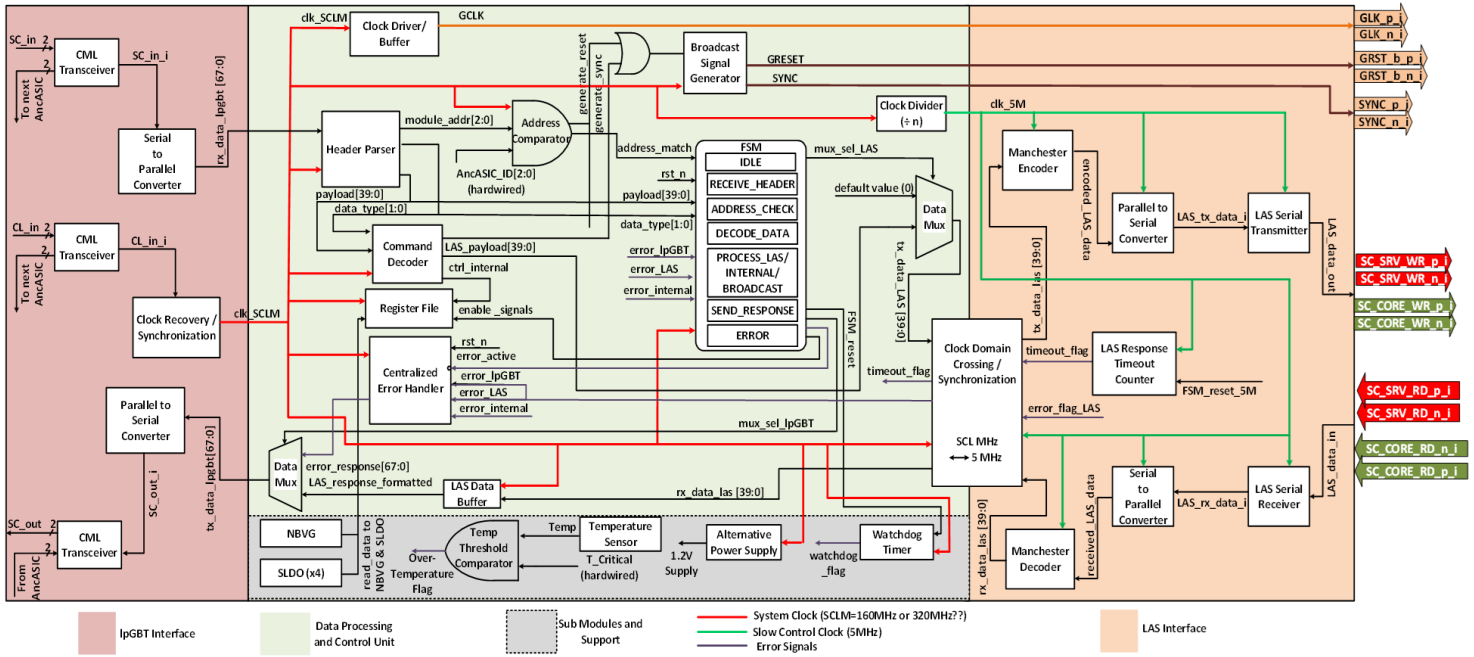
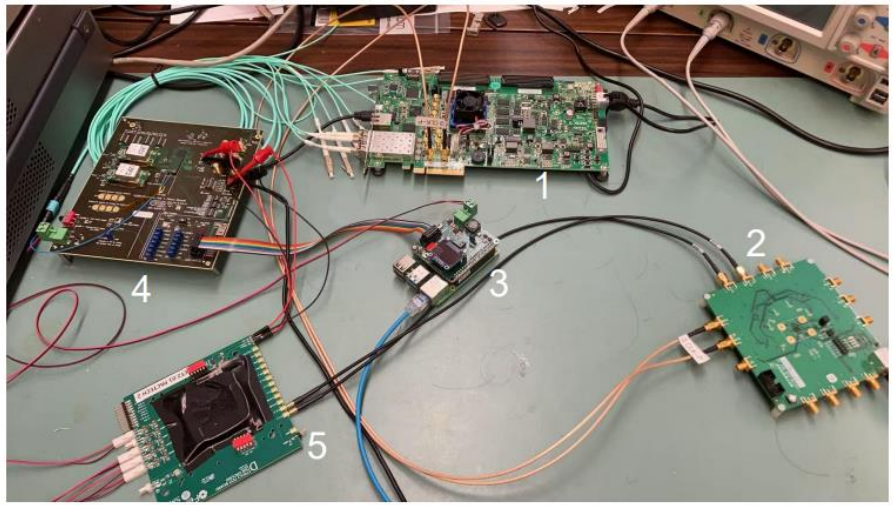
AncBrain

AncBrain

- Required for services reduction and control of NVG and SLDO
- Core modules complete, working on tests with MOSAIX emulator
- Plan to submit as part of first AncASIC
- Hardware emulator in preparation between LBNL, ORNL and BNL

AncBrain Plan, courtesy of Arif Iqbal, BNL

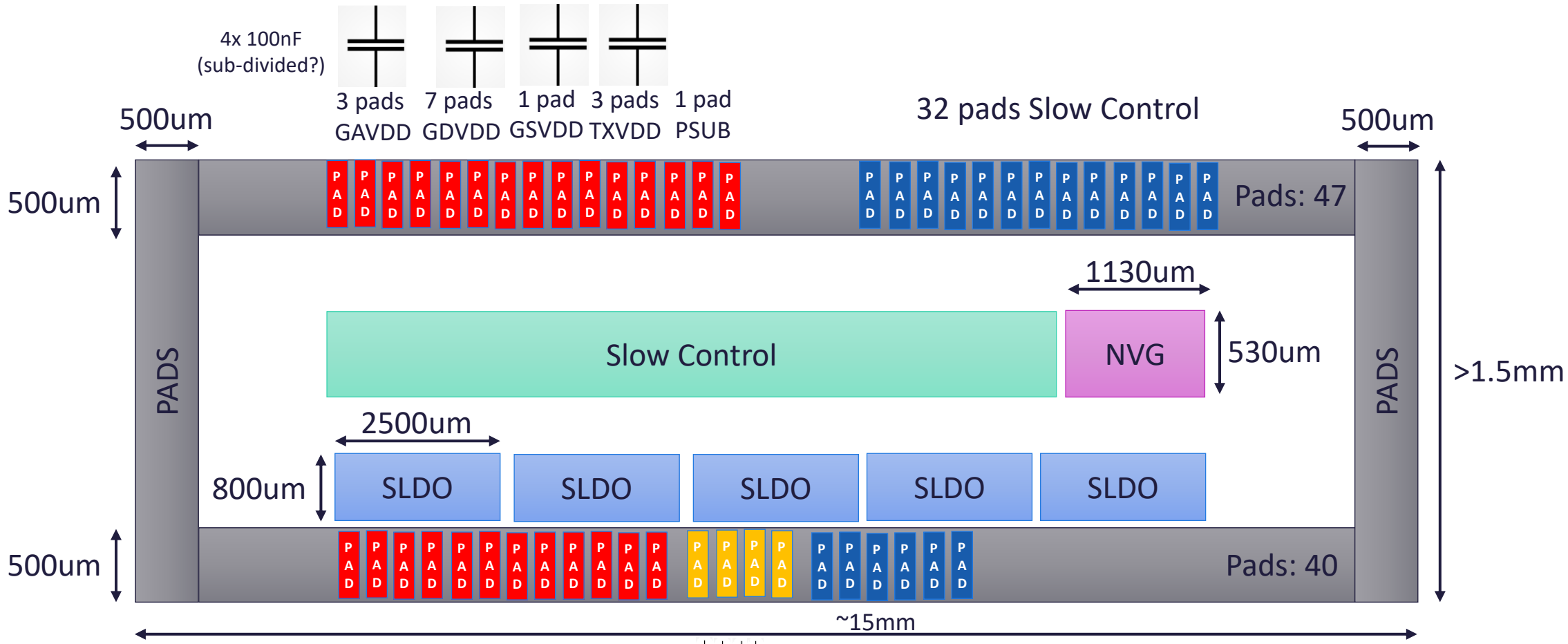




1. KCU105
2. Clock generator
3. PiGBT (status monitor only)
4. VLDB+
5. ETROC2 test board

Hardware mockup, courtesy of Zhengwei Xue, LBNL

AncASIC Overview



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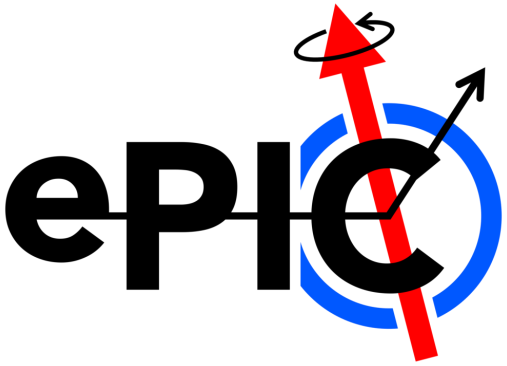
Preliminary



Progress, Next Steps and Ongoing Challenges

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Electron Ion Collider, 10th EIC DAC Meeting

Progress, Next Steps and Challenges

Progress and Next Steps

- AncASIC requires three main blocks. Prototypes for 2 have already been submitted:

• MPW1 (NVG)	March 2025
• MPW2 (SLDO)	March 2025

Work has started on the next components, and planning for further phases:

• Complete MPW1/2 Test Systems	September 2025 (to match out-of-fab date)
• Complete MPW1/2 Testing	March 2026
• Complete AncBrain Design and Validation	Q3 CY2025
• Submit AncASIC V1	September/November 2025
• Complete AncASIC V1 Test System	March/June 2026
• Complete AncASIC V1 Testing	Aug/December 2026
• Complete AncASIC V2 Design Modifications	Q1 CY2027
• AncASIC V2 Production	Q1 CY2027

Complete
In Progress
Not started

Progress, Next Steps and Challenges

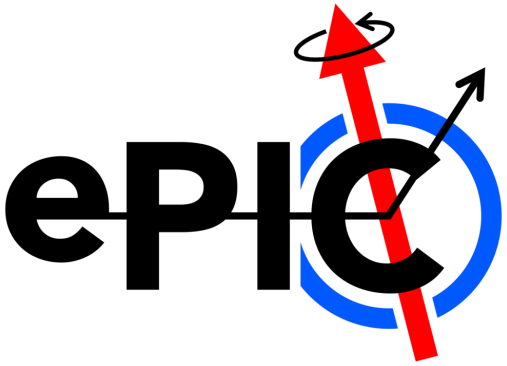
Ongoing Challenges

- Lack of Design Sharing Agreement
  - Condition of academic licences
  - Cannot transfer designs from RAL to BNL
  - Process ongoing for more than a year
  - As a result, exploring workarounds:

    - MPW2: Fully UK submission (Infrastructure Fund, submitted via Europractice)
    - Future: Visiting scientists, commercial licencing, US re-design, still pursuing DSA

  - All time consuming, key reason for uncertainty in MPW3 timeline

- Other (more usual) challenges
  - Long fab times, MPW cancellation, some specifications still evolving
  - Complex design



Conclusion

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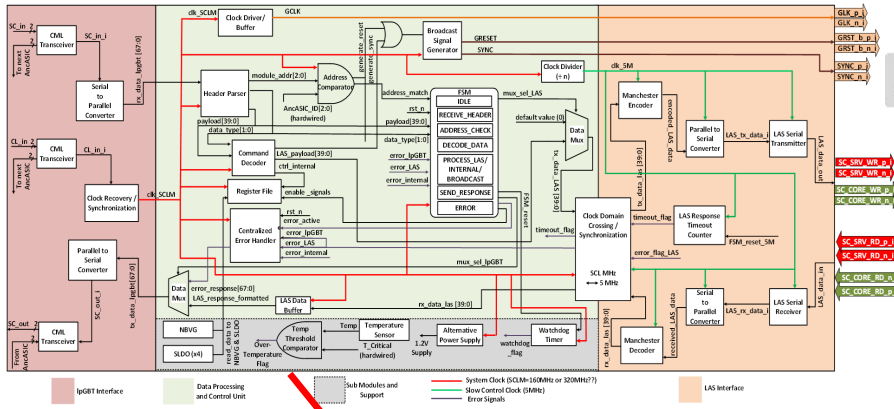
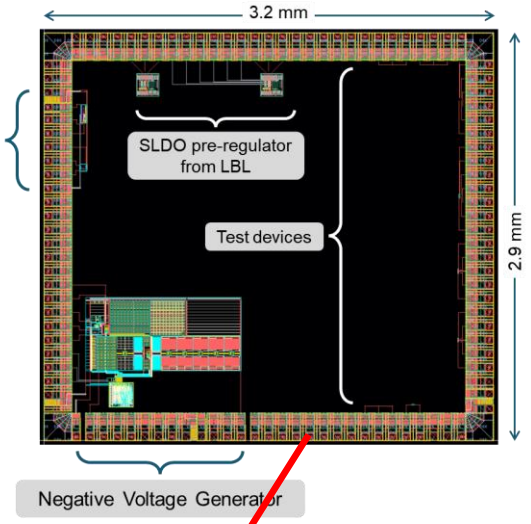
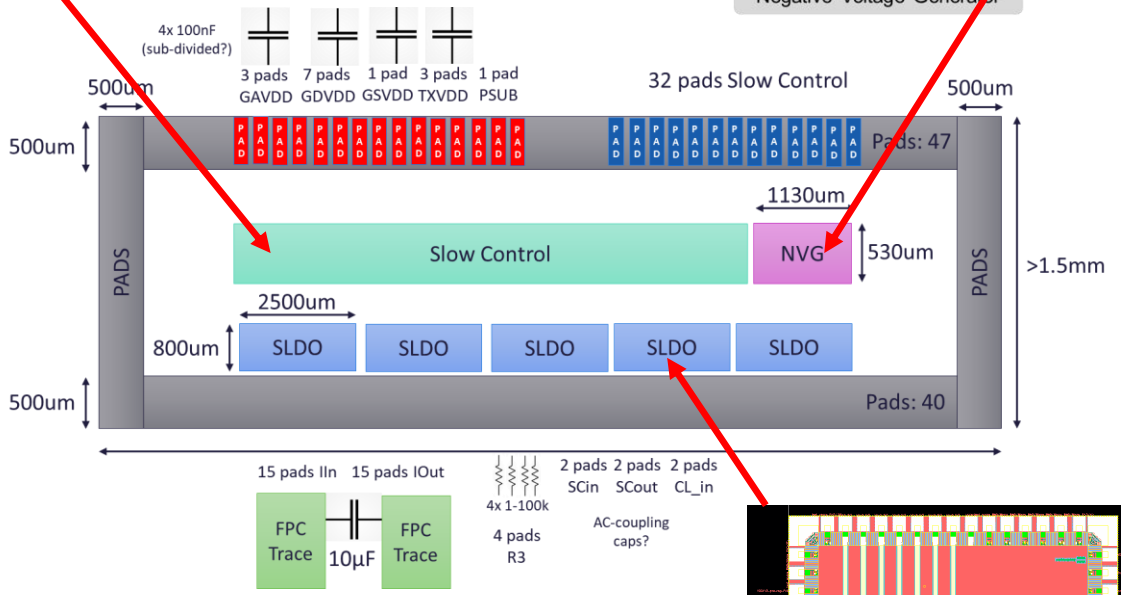
Conclusion

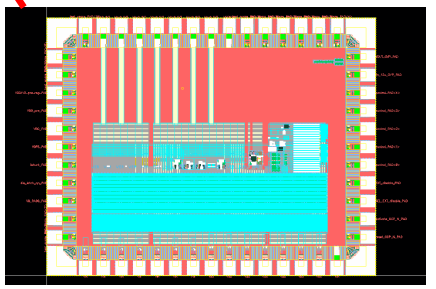
AncASIC Status

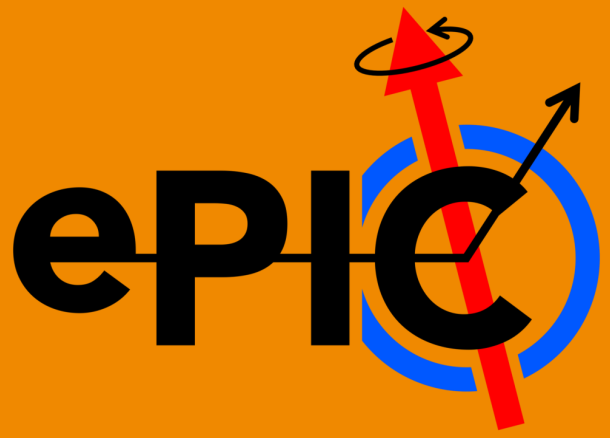
- Design progressing well
  - First test structures in fabrication
  - AncBrain design under way
- Next steps are testing, AncBrain completion and full integration
- Technical progress is good. Challenges remain around schedule and agreements. Working to mitigate.











Questions?

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References

[1] *Radiation and Rate Environment*, Gonella L., ePIC Collaboration Meeting, Argonne, Jan 9 2024, https://indico.bnl.gov/event/20473/contributions/84983/

[2] S. Fernandez-Perez, M. Backhaus, H. Pernegger, T. Hemperek, T. Kishishita, H. Krüger, N. Wermes, *Radiation hardness of a 180nm SOI monolithic active pixel sensor*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 796, 2015, Pages 13-18, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2015.02.066.