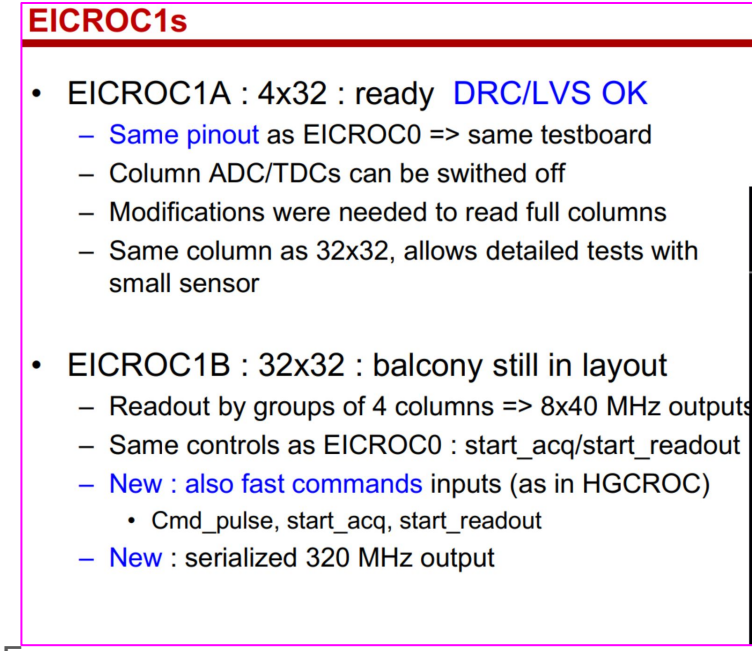
# A few items…

- Our PED request
  - Fernando read our preliminary document and is favourable
    - expects us to add more details in the cost and schedule so we should wrap this up
  - I would like us to standardize on the FELIX-lite
    - we said it will be a KCU105 but I'd like to change that to the **AXAU15** which is far more elegant (smaller, cheaper $600)
    - BTW, I purchased 1 and I have it in Zagreb
    - other groups started to use it as well!
    - I will implement lpGBT protocols (from Zhengwei) and PCIe master interface in due time…
      - goal is the full readout chain
  - The MPGD Detector (Irakli et al) are interested in our SHv1 for their SALSA readout chain
    - they are thinking amongst themselves but the expectation is that they would ask for 2 sets (both RBv1 and PBv1)
    - I think that helping them is in our interest as well… (the more the merrier)
- BNL EICROC0 testing
  - I started looking into providing the FW *to learn how this ASIC behaves*
  - currently using a ZCU106 in the BNL lab (Prashanth) to get myself off the ground quickly but hope that we can continue with AXAU15 (it has a FMC connector!) or ppRDO – TBD
  - we seem to have a small amount of engineering manpower available to make an adaptor card from the EICROC0 testboard to ppRDO – again, TBD
    - or the engineer can help Tim with the PB – TBD

# ASICs (news from various presentations and chats)

- FCFD will be supported from R&D for FY25
  - my understanding is that significant funds have been released to Artur so things should get moving…
- EICROC1 is still on schedule:
  - submission early March, delivery Jun/Jul
- EICROC1A of interest to BNL testing
- EICROC1B of interest for our SHv1
  - lpGBT readout will be supported
  - we need to start preparing
    - How do we get it? Who is “we”? ASIC module? Who makes it?
    - what about bump-bonding a sensor??
      - Who? How? When?
  - I think we need some more “formal” organization within TOF



# BTOF

- we should try to provide more details for the BTOF
- what we know so far
  - 64 FCFD ASICs per RB
  - spread over 4 lpGBTs (16 ASICs per lpGBT)
    - 1 master lpGBT, 3 slave lpGBTs
  - 1 VTRX+ with all 4 uplink fibers used
  - lpGBTs and VTRX+s are in Fernando's order
    - VTRX+ with the shortest pigtail
- What we need to know "soon"
  - location/space/size
  - power needs of the ASICs
  - cooling???
  - connection scheme to the stave FPC
- Japanese funding resources potentially available
  - this needs more formal interfacing and organization (in progress)