

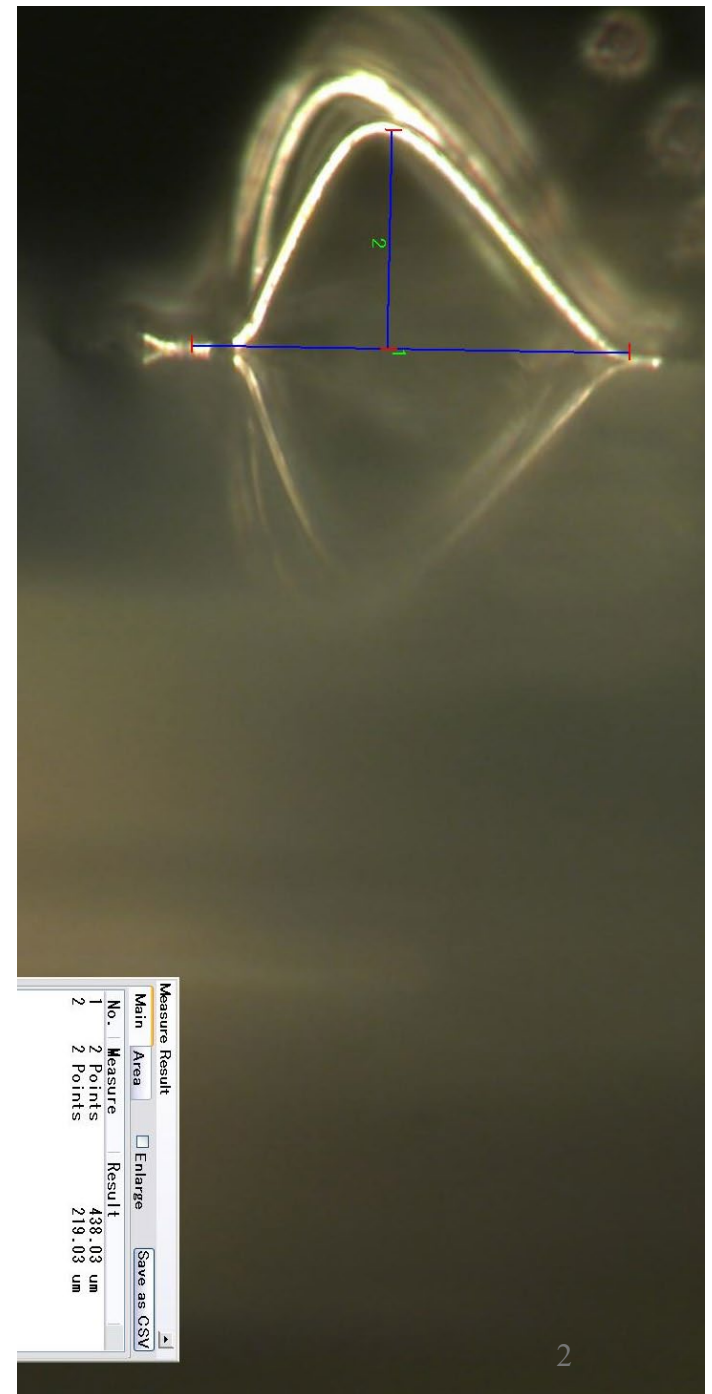
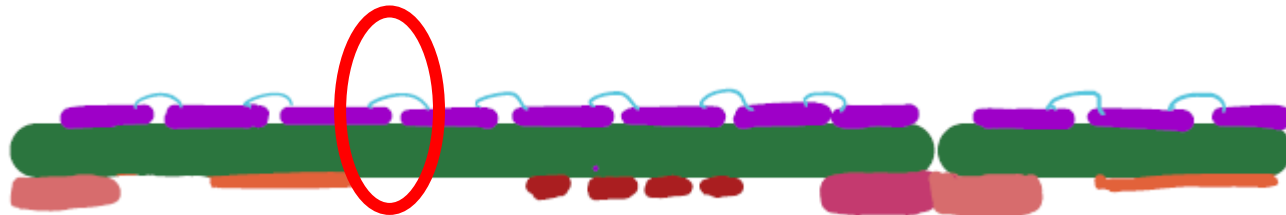
Bonding options for ePIC BIC

A follow-up from March 1st meeting:
checking on the bonding constraints

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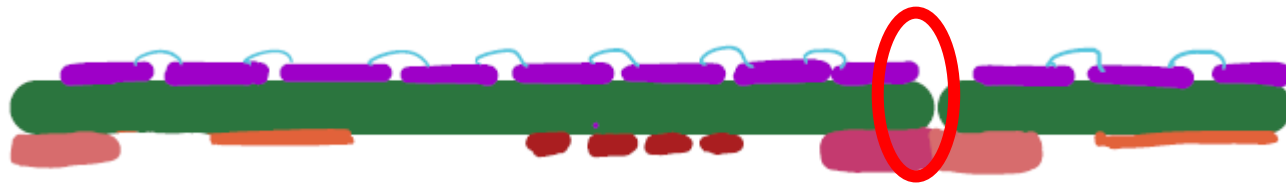
Checking on the bonding distances/constraints: chip-to-chip

- Have to have a bond height at the chip edge (which is at HV!)
- Assuming x2 safety factor and $\max(\text{HV}) = 400 \text{ V}$, would need 266 μm loop height.
- ➔ $> \sim 500 \mu\text{m}$ pad pitch distance for the same height.
- Is this the case for V4/5 chips?



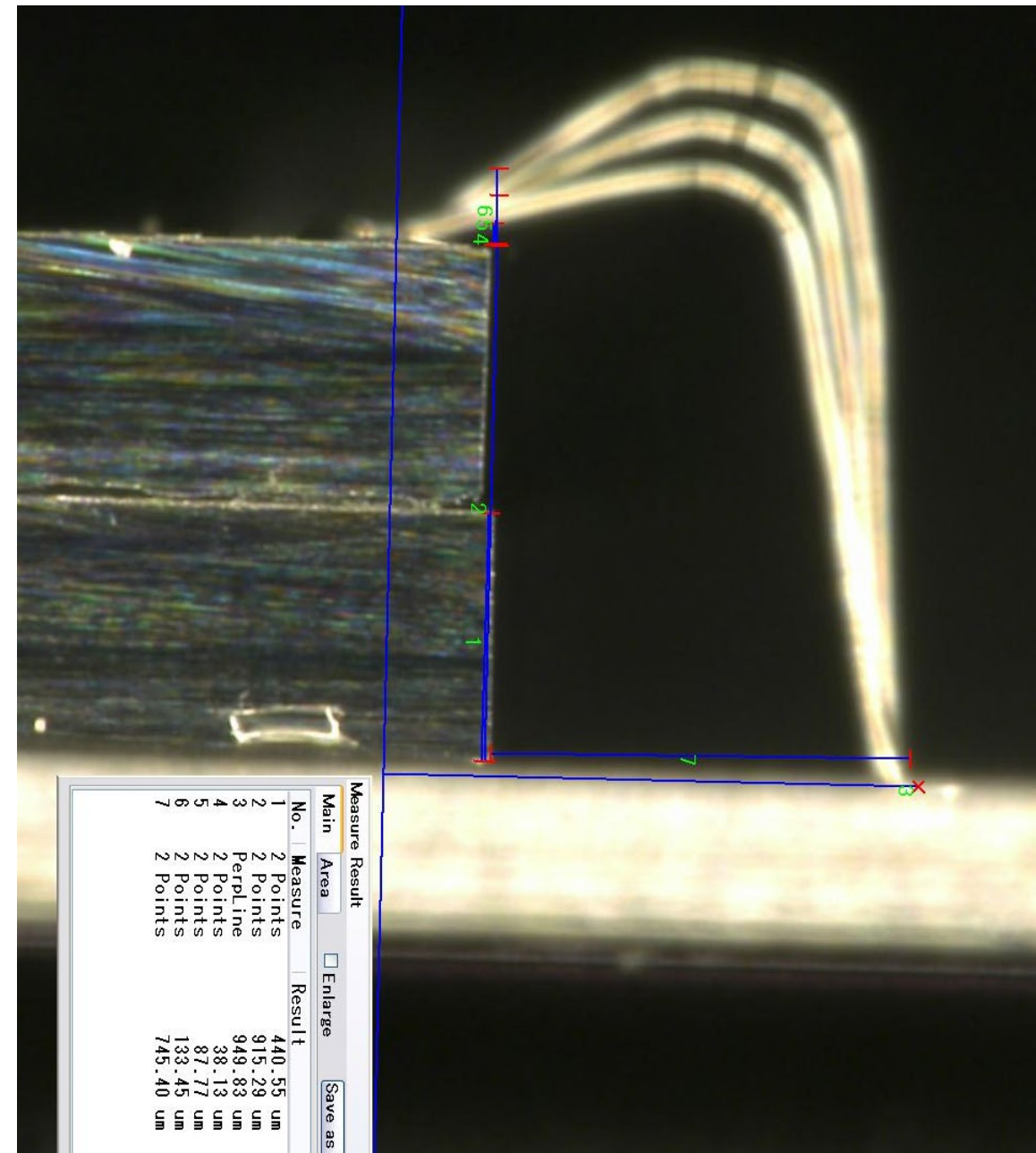
Chip-to-PCB bonding

- Still need the loop height (HV)
- Cannot get too close to the chip edge without making unreliable bond due to kinks at **both** source and destination locations.
 - Note the horizontal distance limits the max loop height to avoid “vertical” portion of the wire and a large part of the wire pressing against the bonding wedge.
- Would prefer ~1 mm. This is probably too much.



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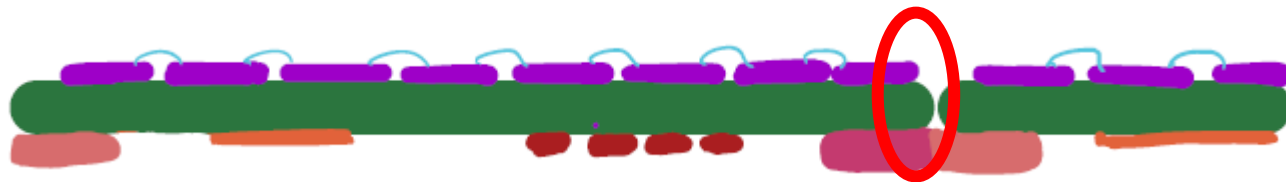
ePIC bonding



Measure Result		
Main Area <input type="checkbox"/> Enlarge <input type="button" value="Save as"/>		
No.	Measure	Result
1	2 Points	440.55 um
2	2 Points	915.29 um
3	Perpl. line	949.83 um
4	2 Points	38.13 um
5	2 Points	87.77 um
6	2 Points	133.45 um
7	2 Points	745.40 um

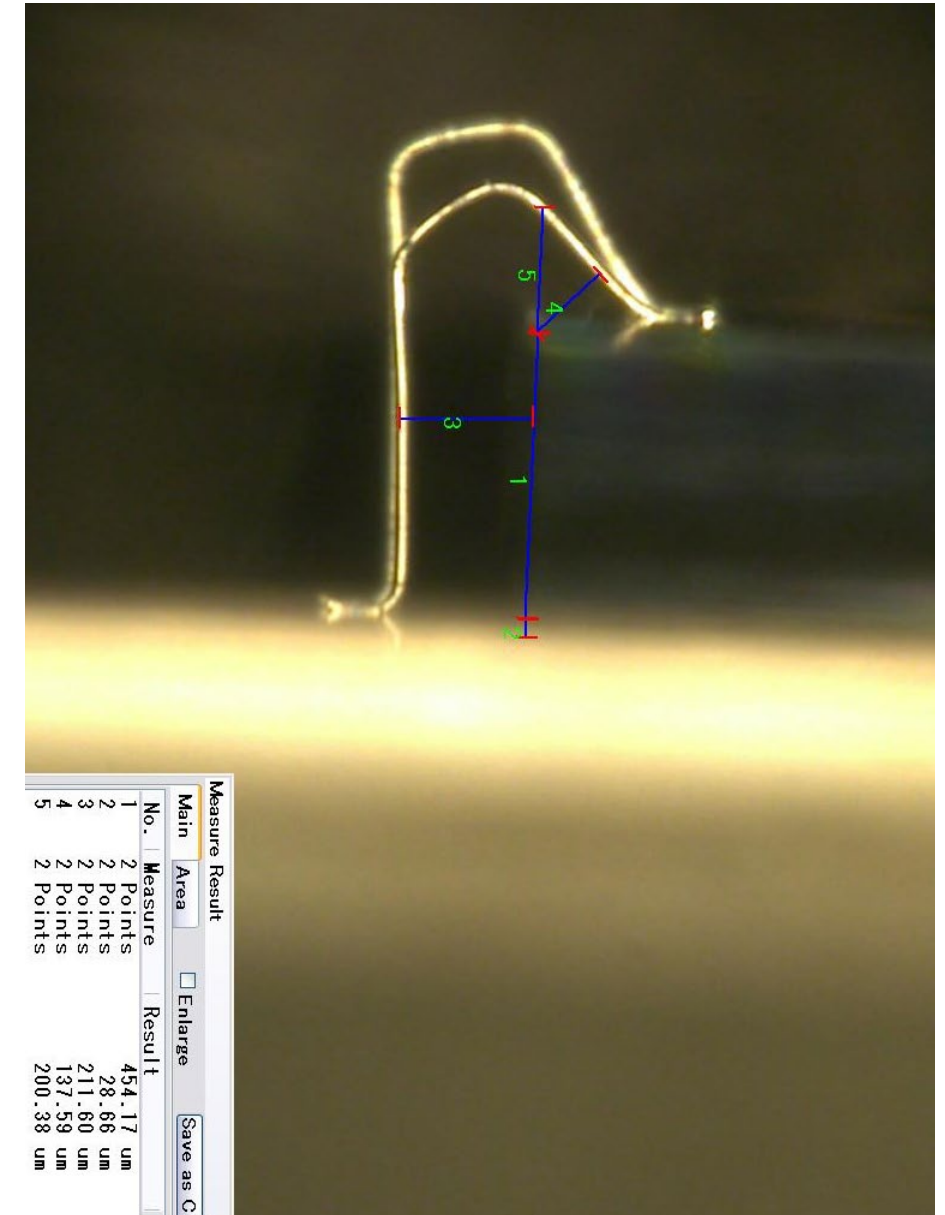
Chip-to-PCB bonding (2)

- An extreme case – got very close, but:
 - Wire against the wedge, kinks.
 - Limitations on the wire pitch (due to the wedge width)



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ePIC bonding



Chip-to-PCB bonding (2)

- To stagger the SPI bond pads, to be able to bond to the other side?
- This would allow to limit the length of the hybrid required.

