Ancillary ASIC - testing preparations
with focus on MPW1 and MPW2

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March 4, 2025, SVT meeting

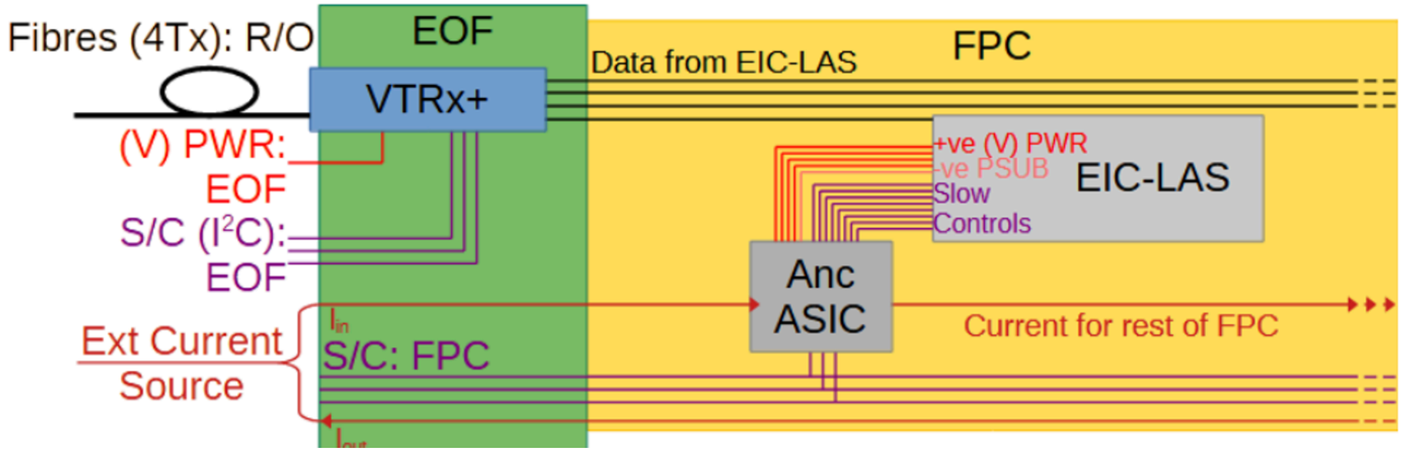
AncASIC

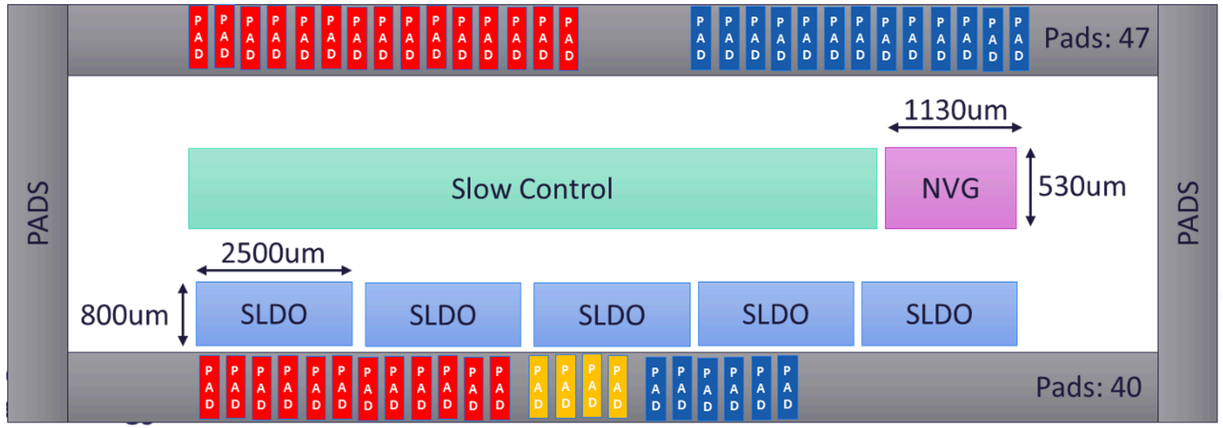
Main blocks:

- Negative Voltage Generator NVG
- SLDO
- AncBRAIN with slow Control

(4) development stages (preliminary):

- MPW1, 2, 3, x - prototype (chiplets)
- ER AncASIC production on 8“ wafers





MPW1/MPW2

Main blocks MPW1:

- Negative Voltage Generator (NVG)
- SLDO Pre-Regulator
- CML Transceiver
- Transistor Test Structures (for radiation hardness validation of XT011 process)

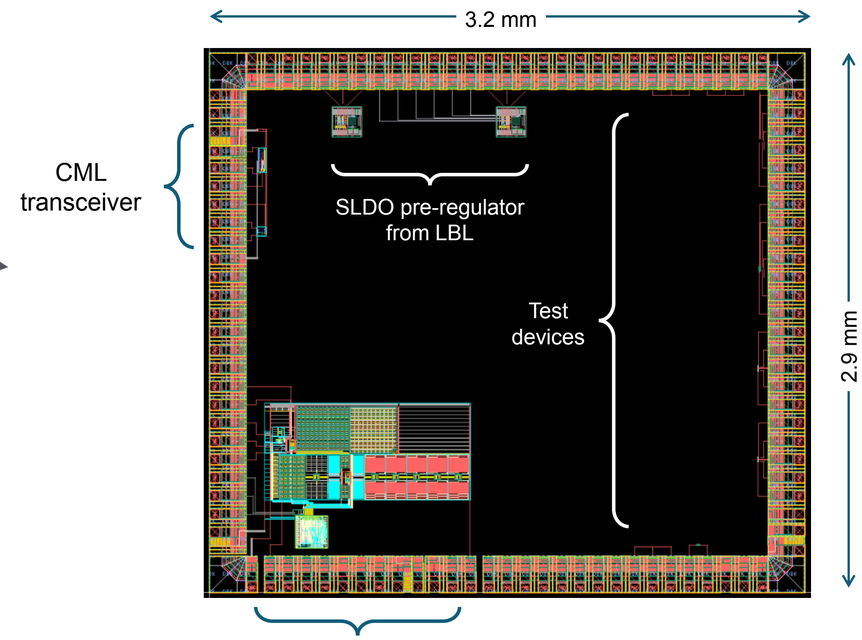
MPW2:

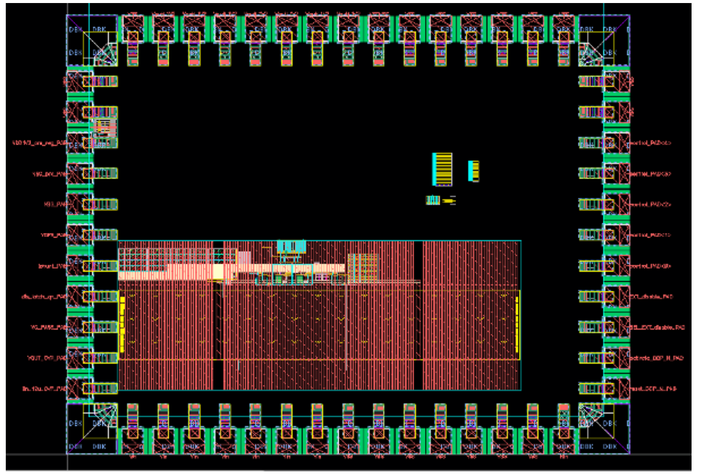
- SLDO

Details:

- 45 individual chiplets for each MPW
- Submission is planned to May 2025
- **Delivery from the fab in September 2025**

1st Prototype: AncASIC sub-blocks and test devices





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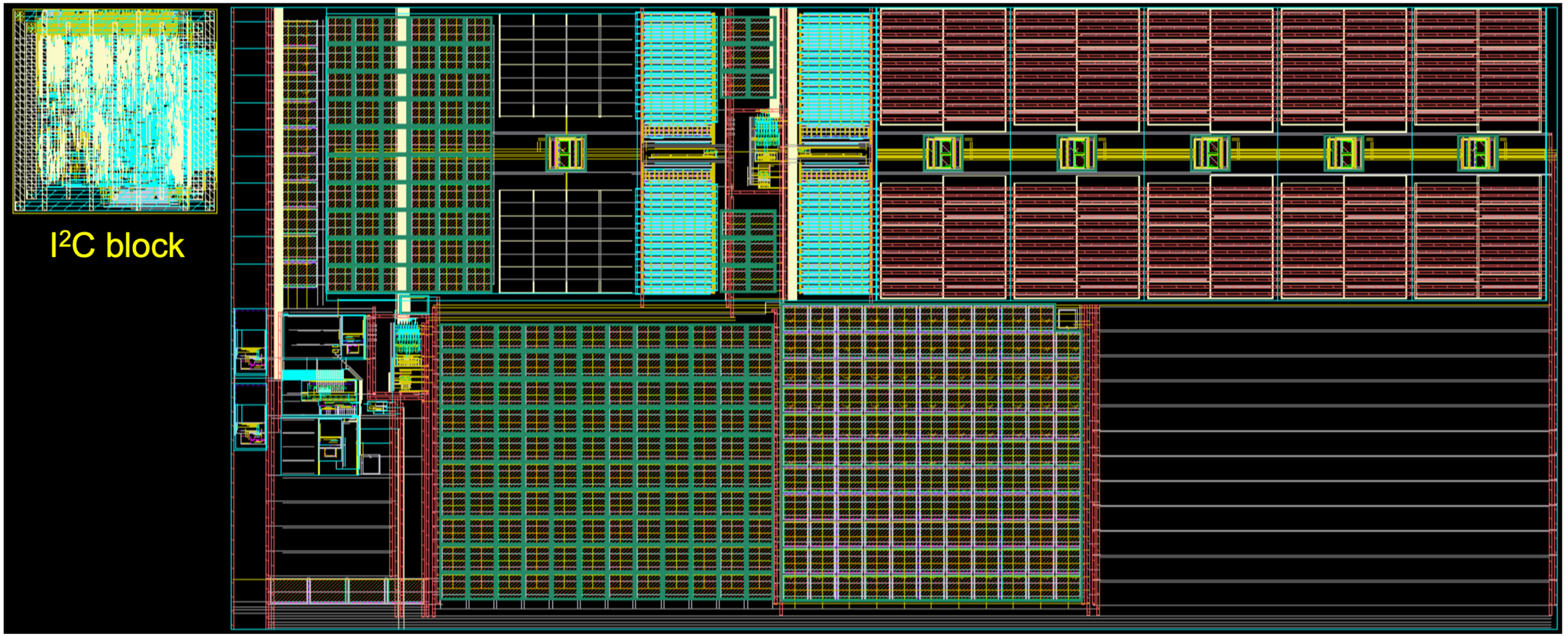
MPW1 - NVG



- Power source
- I²C control via FPGA
- Measure output voltage (default -3V)

MPW1 - Transistor Test Structures

- LVT MOSFETs
- Bipolar Junction Transitors
- Varactor
- POLY Resistor

- Transistor characteristics scan
- IV measurement
- LCR meter

- nelvt
  - W=1u, L=110n
  - W=1u, L=150n
  - W=1u, L=500n
  - W=1u, L=1u
- pelvt
  - W=1u, L=110n
  - W=1u, L=150n
  - W=1u, L=500n
  - W=1u, L=1u

- BJT
  - qpva
  - qpvb
- mosvc (7u x 7u cell)
- Rpp1 (w=3u and l=20u)
- nelvt, pelvt
  - Weff. = 100um, L=150nm
  - Interdigitation layout to measure leakage
  - Two copies
    1. minimum DTI enclosure spacing
    2. 1.0um DTI enclosure spacing

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MPW1/MPW2 testing needs

- PCB carrier board
- Standard test equipment (power sources, voltmeters, ammeters, LCR meters, oscilloscope etc.)
- Transistor test structure IV setup
- Environmental chamber for temperature tests
- I^2C FPGA control for NVG
- Irradiation (X-ray, Cobalt-60) - TID up to 1MRad
- (SEE/SEU of I^2C in a proton beam)

Testing details defined by WP1:

- https://docs.google.com/spreadsheets/d/1VWeK98f8jZUxhvNr1PAeVBIMx0neTcvY2W6wPgqrf0A/edit?usp=sharing

AncASIC testing resources, group interests

- **BNL**
  - Carrier board design for MPW1
  - NVBG testing
  - AncBRAIN testing
  - AncASIC software mockup
  - (SLDO) – limited, investigating interfacing between AncBrain and SLDO for settings and diagnosis
  - TID irradiation (Cobalt60)
  - SEE testing

- **UK groups** (STFC Rutherford Lab, University Of Birmingham, STFC Daresbury Lab, Brunel)
  - Carrier board design for MPW2 SLDO - Marcello Borri
  - SLDO testing
  - Test Structures testing + TID irradiation (X-ray)

AncASIC testing resources, group interests - cont.

- **LBL**
  - SLDO preregulator from MPW1 (designed by LBL), SLDO from MPW2 (with contributions from LBL designers)
  - AncBRAIN hardware mockup
  - TID irradiation
  - SEE testing

- **CTU**
  - (PCB design if needed)
  - (NVG, SLDO testing if needed)
  - Test Structures testing + TID irradiation (X-ray, Cobalt60)
  - SEE testing with a proton beam

- **LANL**
  - Contribute to the FPGA I2C controller development for NVG. (Joellen Renck)
  - Contribute to the AncASIC slow control FPGA development. (Joellen Renck)
  - Temperature tests with existing environment chamber.

MPW1 - Task list PRELIMINARY!

	MPW1						
	Task	**Start date**	**End date**	**Testing details, conditions**	**Comments**	**Equipment**	**Responsible person/group (interest**
	MPW1 tapeout/submission (WP1 task)						**WP1**
	MPW1 testing						
1	**Test specs definition**						**WP1, WP2**
2	**Carrier board PCB design + manufacturing, pre-testing**						**BNL**
3	**Chip+PCB assembly, wirebonding**						**BNL**
4	**SLDO Pre-Regulator characterization**					Standard lab equipment (power supply, IV meters, oscilloscope etc.)	**UK, LBL**
	Output Ripple/Noise			Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)			ESR - **3.5k**			
	PSRR and line regulation			Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up			Standard Radiation Range	0 - 1MRad in 100kRad steps		
				Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
5	**NVG characterization**					Standard lab equipment (power supply, IV meters, oscilloscope etc.) **I2C control via FPGA**	**BNL, (LANL)**
	Output Ripple/Noise			Load Capacitance - RANGE?			
	Transient Response (overshoot and settling time)			Frequency - RANGE?			
	PSRR and line regulation			Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up			Standard Radiation Range	0 - 1MRad in 100kRad steps		
				Standard Supply Variation	Plus and Minus 20%		
				Ramp Rate - RANGE?			
	Test in combination with APTS/DPTS/ER1				Use NVG to generate back bias for already existing APTS and DPTS chips		
6	**Transistor Test Structures characterization**					Standard lab equipment (power supply, IV, LCR meters, oscilloscope etc.)	**BNL, UK, LBL, (CTU)**
	Ids vs Vgs					TTS characterization IV setup	
	Vt extraction						
				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
				Standard Radiation Range	0 - 1MRad in 100kRad steps		
				Standard Supply Variation	Plus and Minus 20%		
7	**CML transciever**						**BNL ?**
8	**Irradiation**						**BNL, UK, LBL, (CTU)**
				X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring		
				Standard Radiation Range	0 - 1MRad in 100kRad steps		
9	**SEE/SEU Tests in a proton beam**					Proton beam with XY table	**BNL, LBL, (UK), (CTU)**

MPW2 - Task list PRELIMINARY!

	MPW2						
	Task	**Start date**	**End date**	**Testing details, conditions**	**Comments**	**Equipment**	**Responsible person/group (interested p**
	MPW2 tapeout/submission (WP1 task)						**WP1**
	MPW2 testing						
1	**Test specs definition**						**WP1, WP2**
2	**Carrier board PCB design + manufacturing, pre-testing**						**UK (Marcello Borri)**
3	**Chip+PCB assembly, wirebonding**						**UK**
4	**SLDO characterization**					Standard lab equipment (power supply, IV meters, oscilloscope etc.)	**UK, LBL**
	Output Ripple/Noise			Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)			ESR - **3.5k**			
	PSRR and line regulation			Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up			Standard Radiation Range	0 - 1MRad in 100kRad steps		
				Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
8	**Irradiation**						**UK, LBL, (CTU)**
				X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring		
				Standard Radiation Range	0 - 1MRad in 100kRad steps		

Conclusion

- AncASIC testing tasks for MPW1 and MPW2 should be covered quite well mainly by the groups that contibuted to the design of main functional blocks of AncASIC (BNL, UK, LBL). There is also possible backup of some testing tasks by other groups where needed (CTU, LANL, ..)
- For now, there is only a list of preliminary tasks and interested parties. We will have to meet and specifically agree on the final plan who will test what, when and update the details of testing procedures and their parameters.
- Distribution plan especially for MPW1 with test structures for TID irradiation tests will have to be thought out (number of chiplets is limited).

- For the future submissions (MPW3..), the focus on preparing for AncBRAIN test is needed. The software+hardware mockup from BNL/LBNL necessary for AncBRAIN testing.