sPHENIX-INTT Silicon Tracker

A solution and relevance of half entry

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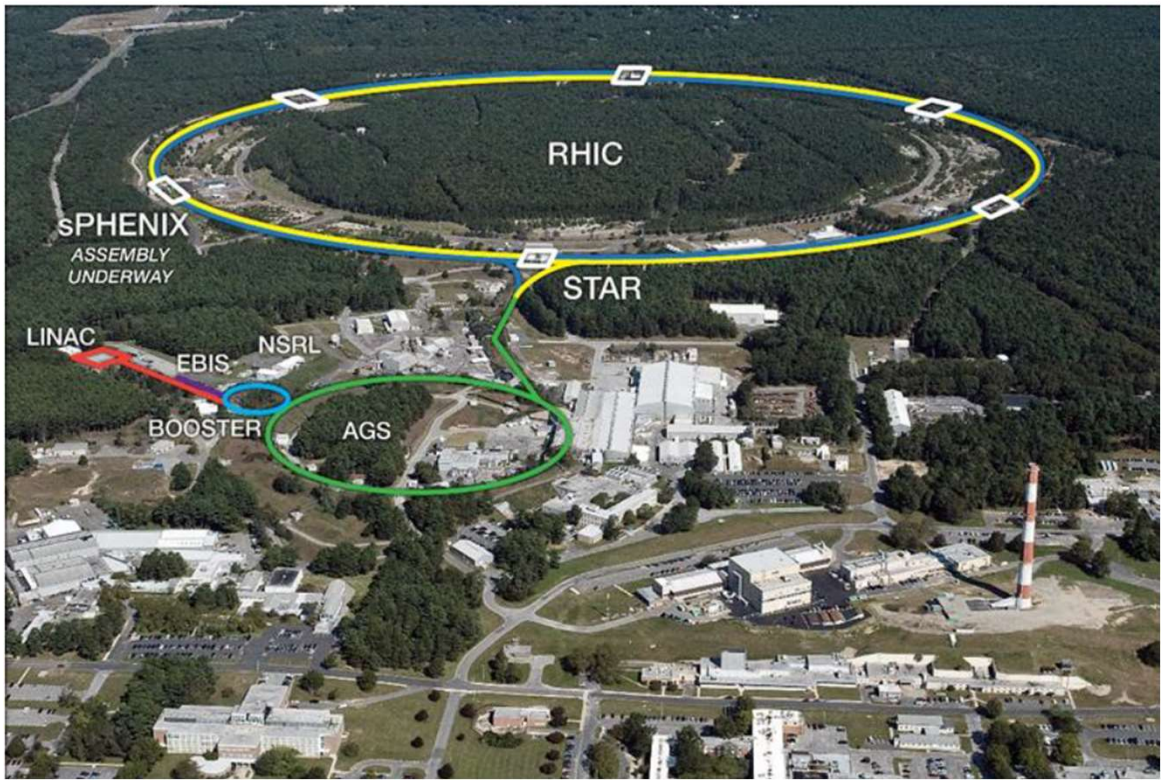
sPHENIX

sPHENIX

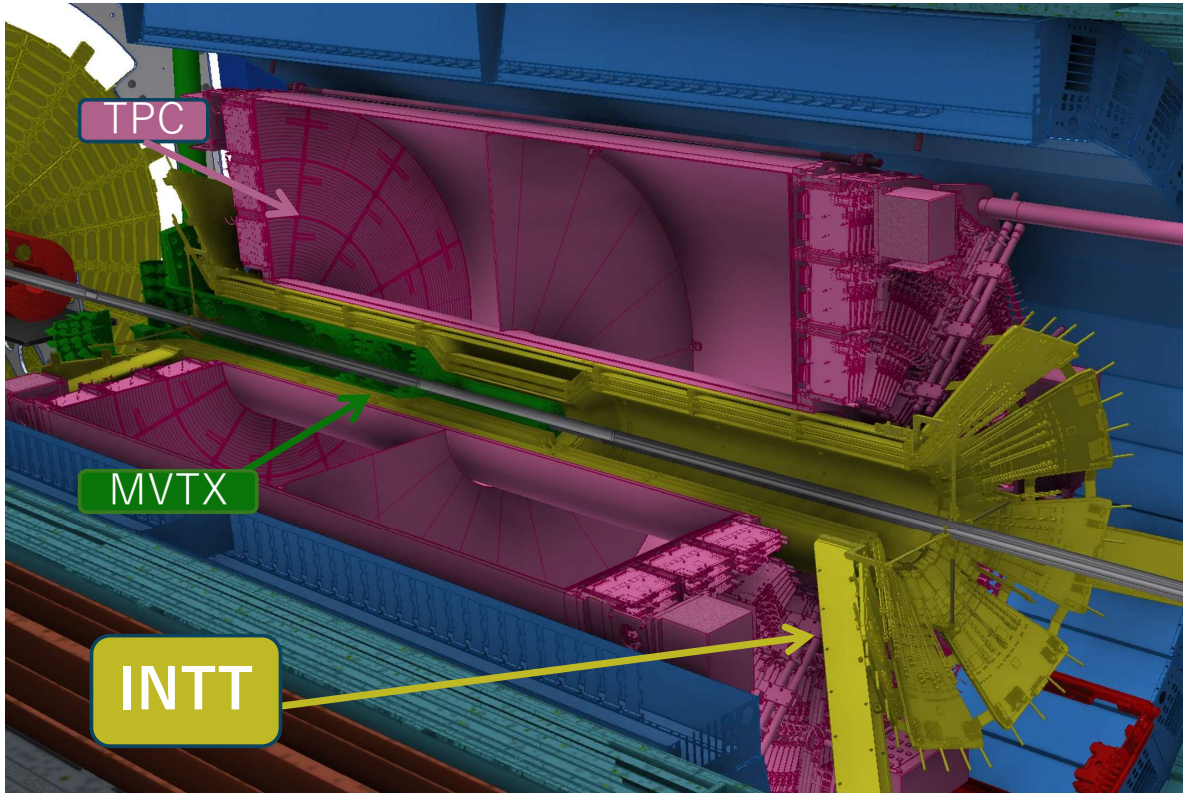


sPHENIX is an experiment at the Broolhaven National Lavboratory (BNL) to study the QGP state using the Relativistic Heavy Ion Collider (RHIC).

sPHENIX

There are three sPHENIX track detectors,
MVTX, INTT, and TPC
from the inside of the beamline.

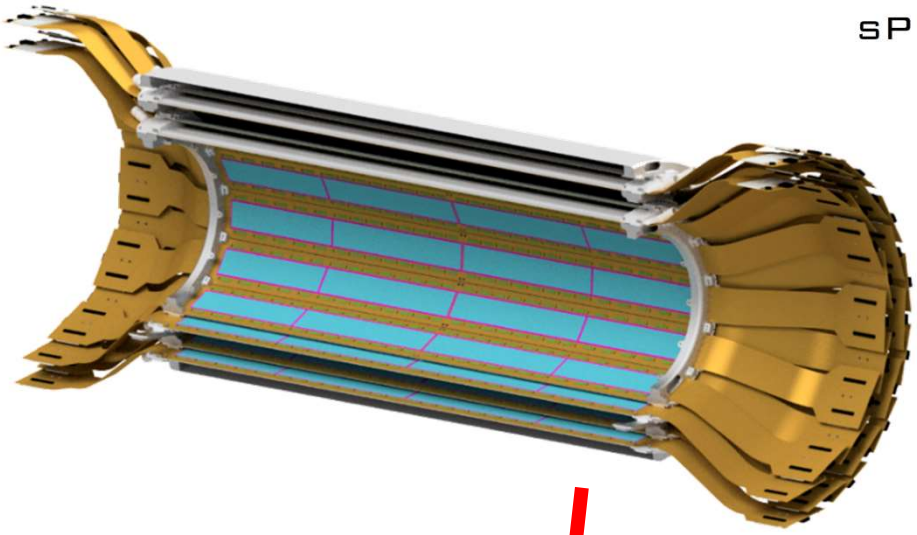
The Japanese group is in charge of the development, construction, and operation of the “INTT”.



INTT

INTT

INTT is a silicon strip detector consisting of 56 INTT ladders.



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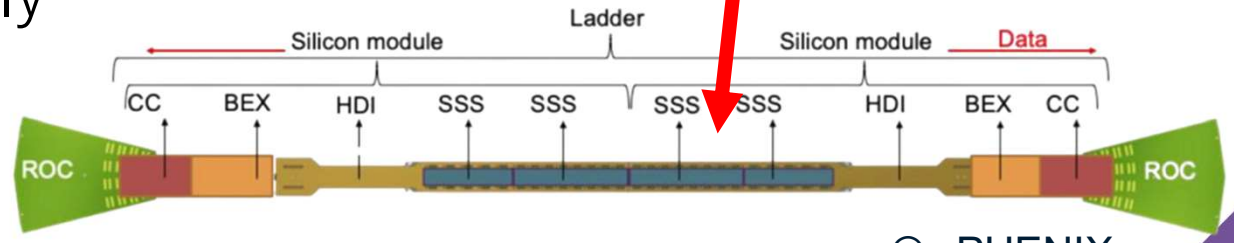
The signal detected by the silicon strip sensor is finally transferred to the ROC.



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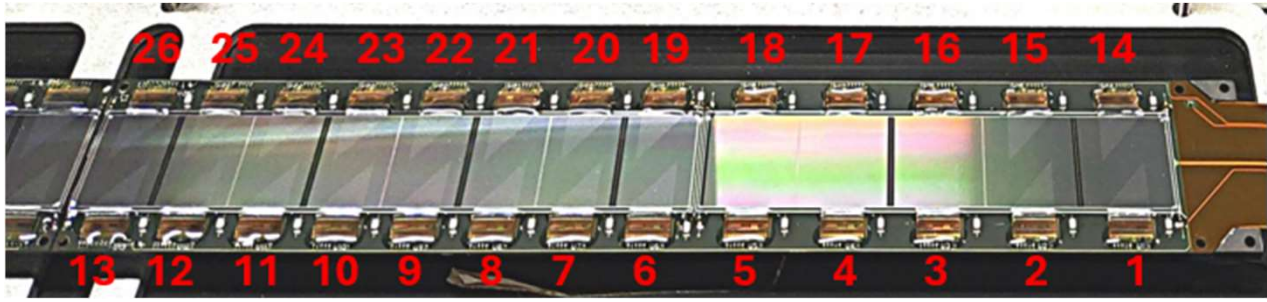
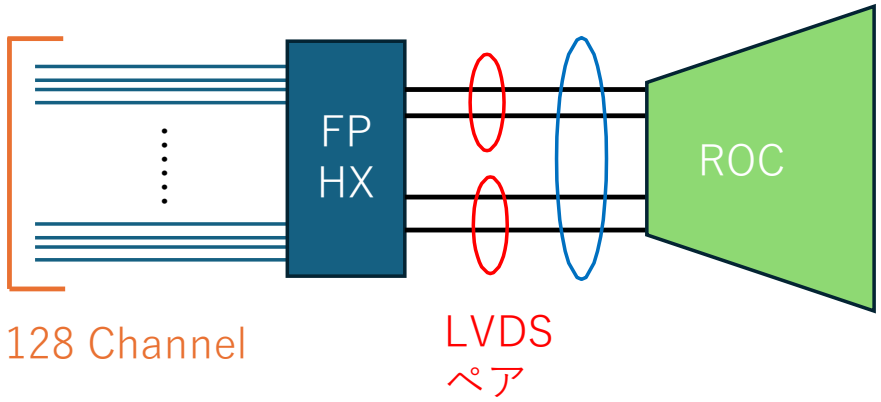
INTT

The INTT half ladder consists of 2 sensors and 26 FPHX chip. Each cell is divided into 128 strips (Channels).



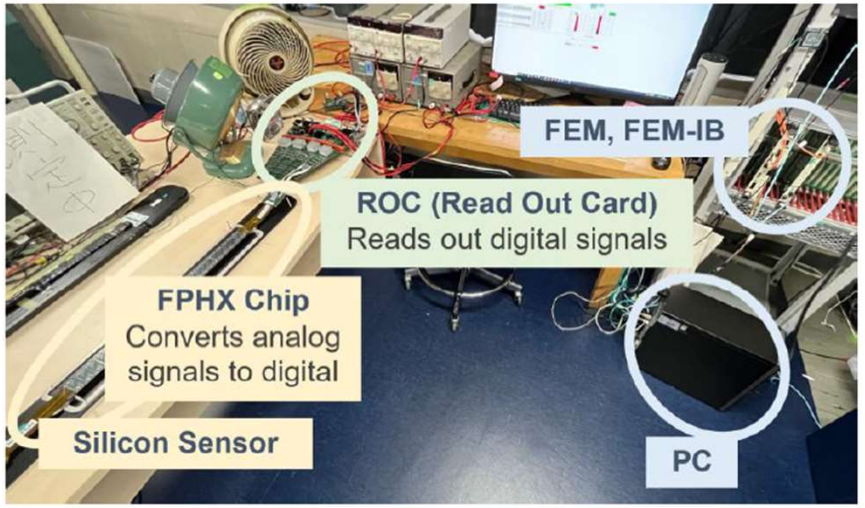
FPHX chip to ROC Data is transferred by two sets of LVDS standard output lines.



テストベンチ

RIKEN has a “test bench”
The operation of the INTT half ladder can be checked.

From silicon strip sensor toto ROC,
The setup is the same as in sPHENIX.



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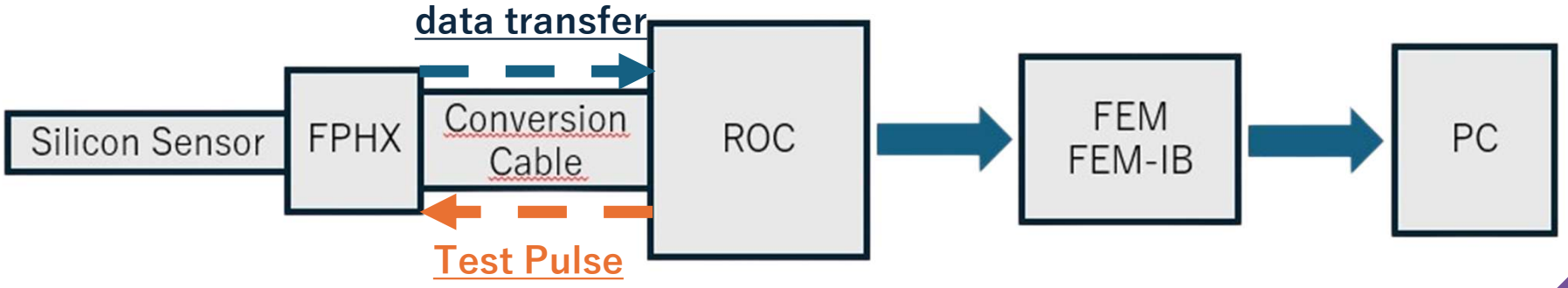
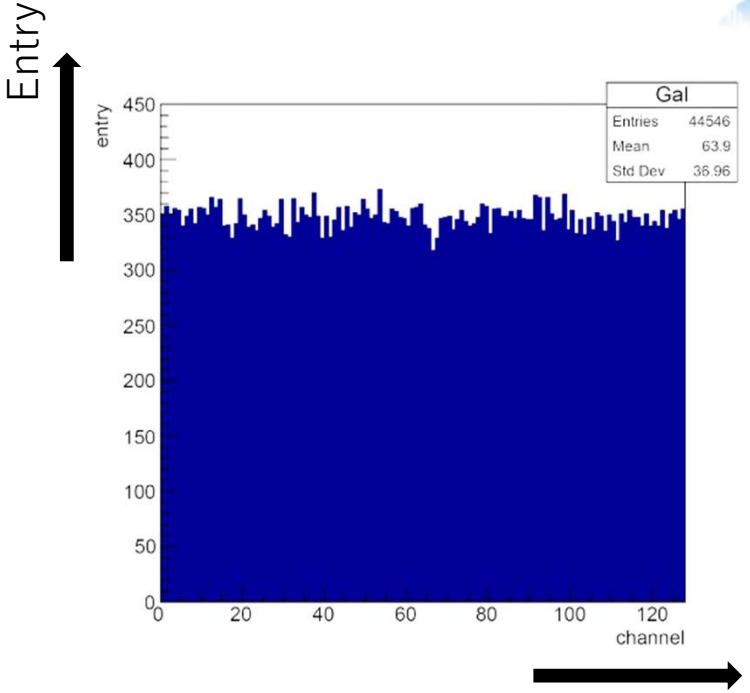
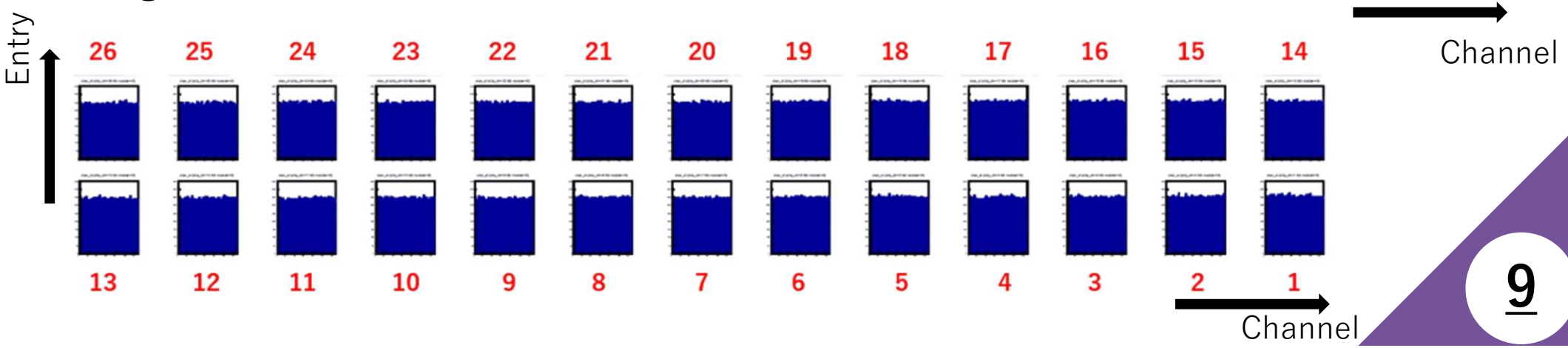


テストベンチ

The ROC has a function to send test pulses to the FPHX chip
to verify whether the readout system is properly transmitting signals.
This process is called a “calibration test”.
The figures show the histogram of
chip 1 and the histograms of all 26 chips
during the calibration test.

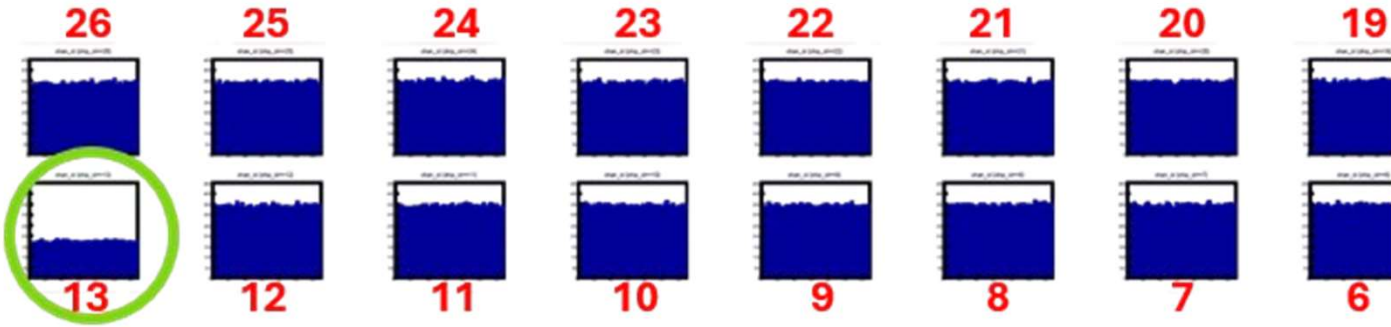




Causes and solutions of half entries

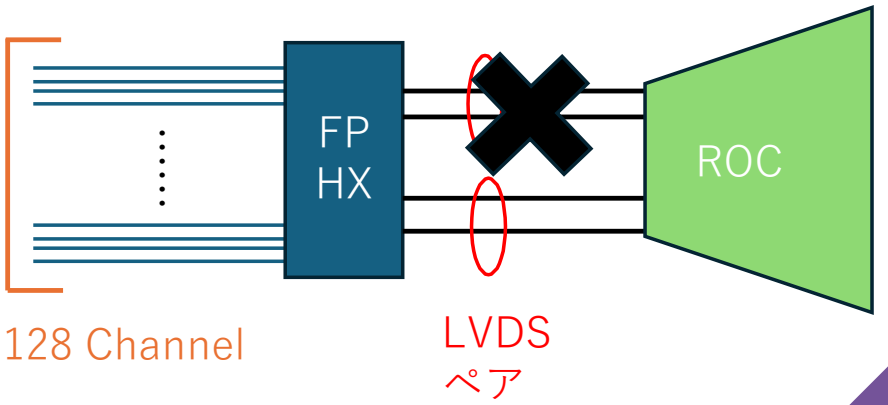
Verification of the cause of half entry ①

In the calibration test, a chip was found to detect a lower amount of signals. The detected amount was half of the expected value.



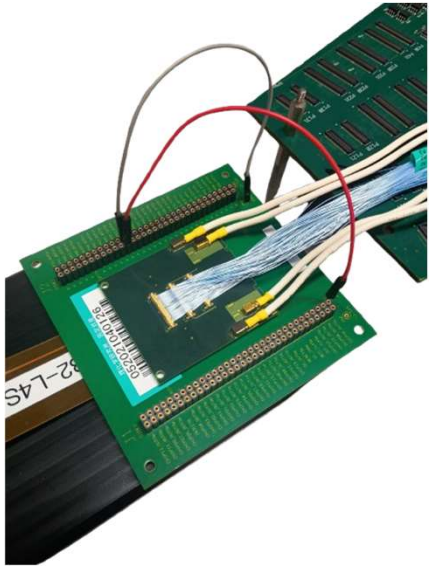
This phenomenon is called half entry.

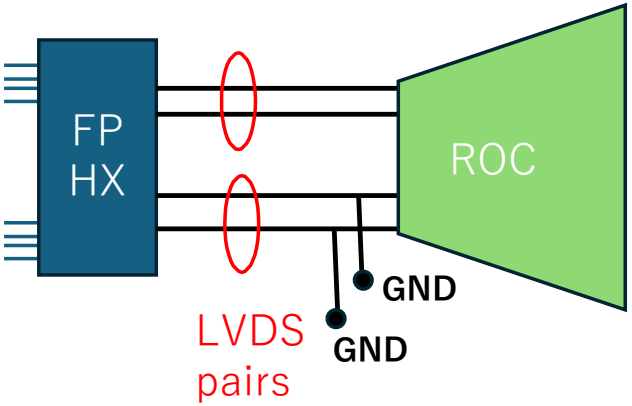
If one of the two output lines is intercepted,
it can be expected that the amount of data will be half entry.



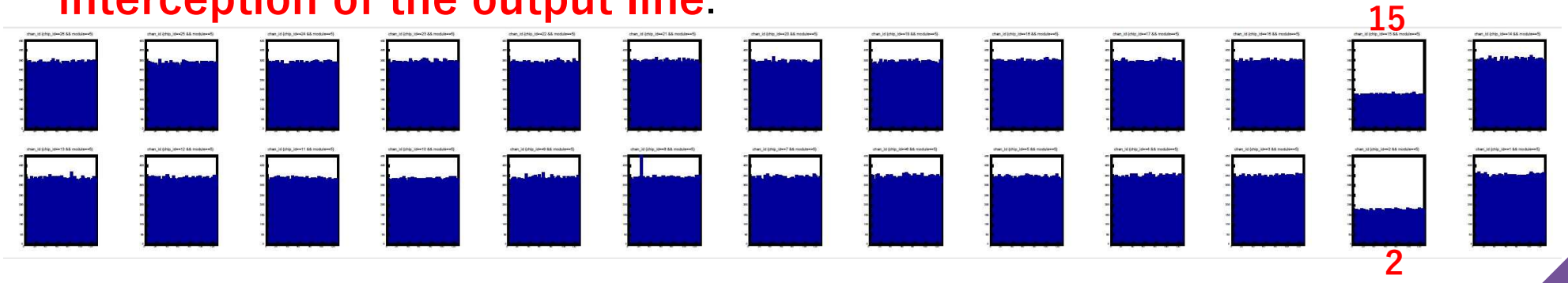
Verification of the cause of half entry ②

The cause of the half entry was examined using the interception board.
The figure below shows the results of the calibration test when the output lines of Chip 2 and Chip 15 were intercepted.。





The half entry was reproduced!
⇒ The cause of the half-entry is the **interception of the output line**.



How to solve the half entry ①

One of the Slow Control functions built into the FPHX chip is Digital Control (DC).
DC is a 4-bit parameter, and the function of each bit isTable.

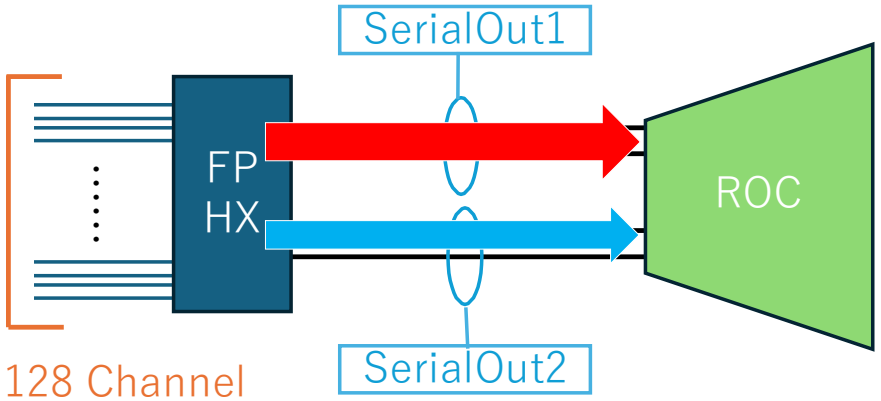
DC Bit	function	ON	OFF
Bit0	Active Serial Lines	0	1
Bit1	Accept	1	0
Bit2	Global Inject Enable	1	0
Bit3	Serial Output Order	/	/

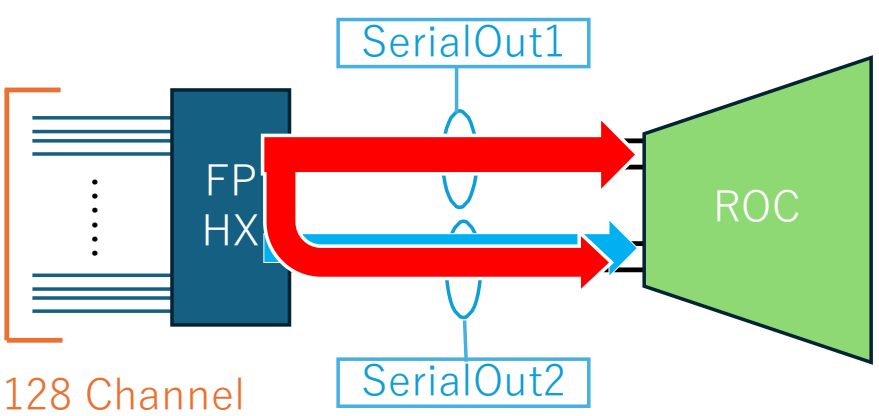
- Bit 0 controls whether to generate a duplicate of the signal.
- Bit 1 controls whether to receive signals from the silicon strip sensor.
- Bit 2 controls whether to receive test pulse.
- Bit 3, when Bit 0 is 0(duplicated), controls which output line the duplicated signal is sent to.

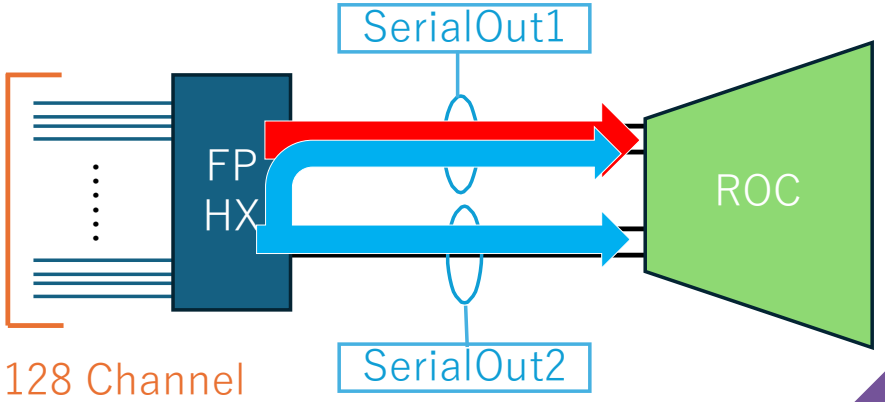
How to solve the half entry ②

The two output lines are called SerialOut1,2.

When duplicating signals using Digital Control (DC), the setting will be either
DC = **0110 (6)** or **1110 (14).**
The figure below provides
a simplified diagram of this configuration.





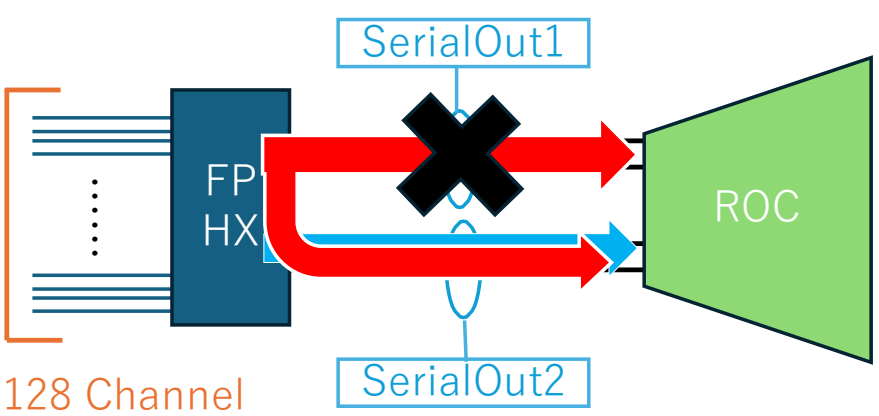


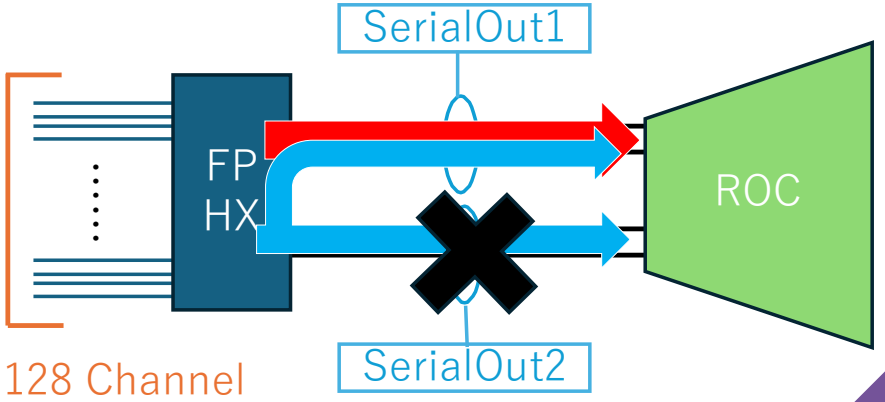
How to solve the half entry ③

If SerialOut1 is intercepted, the DC parameters should be set as shown in the **left diagram.**
If SerialOut2 is intercepted, the DC parameters should be set as shown in the **right diagram.**

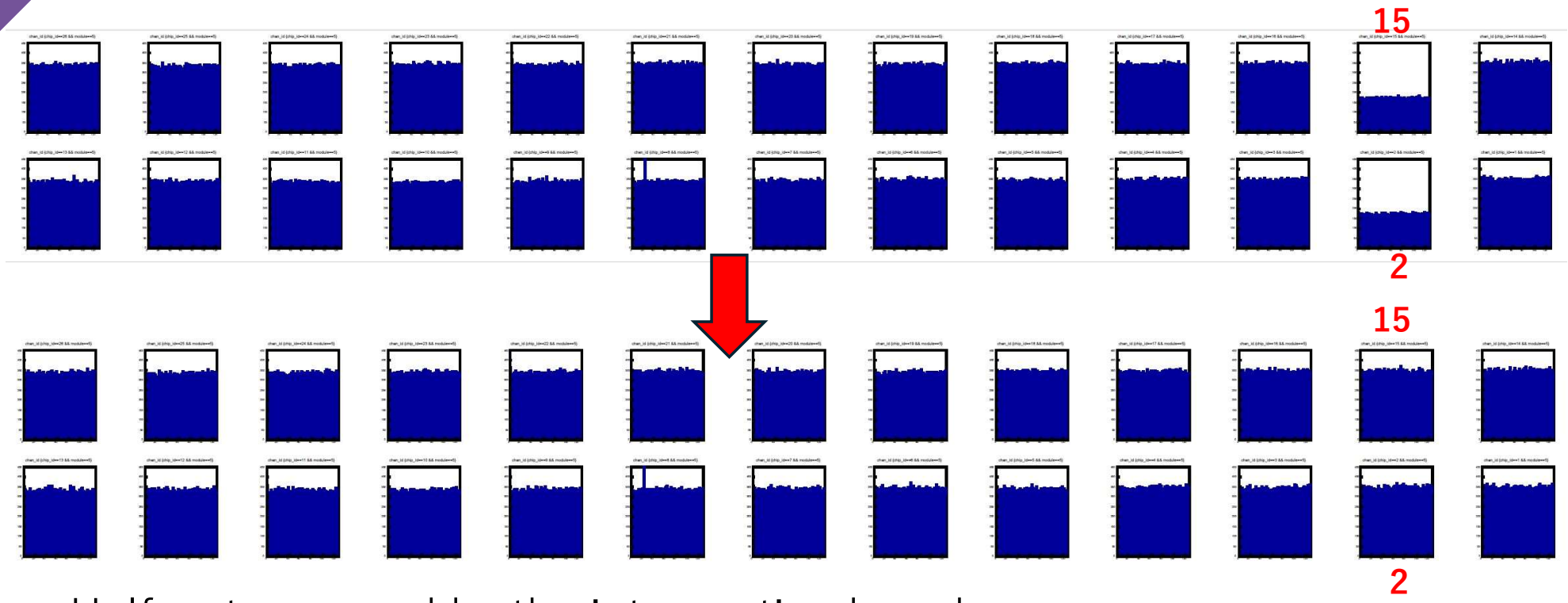
By using **Digital Control**, we aim to resolve **half entry.**

However, to determine which output line is intercepted,
it is necessary to test both DC patterns.





Solving the half entry



- Half-entry caused by the interception board
- Half-entry actually observed on the test bench

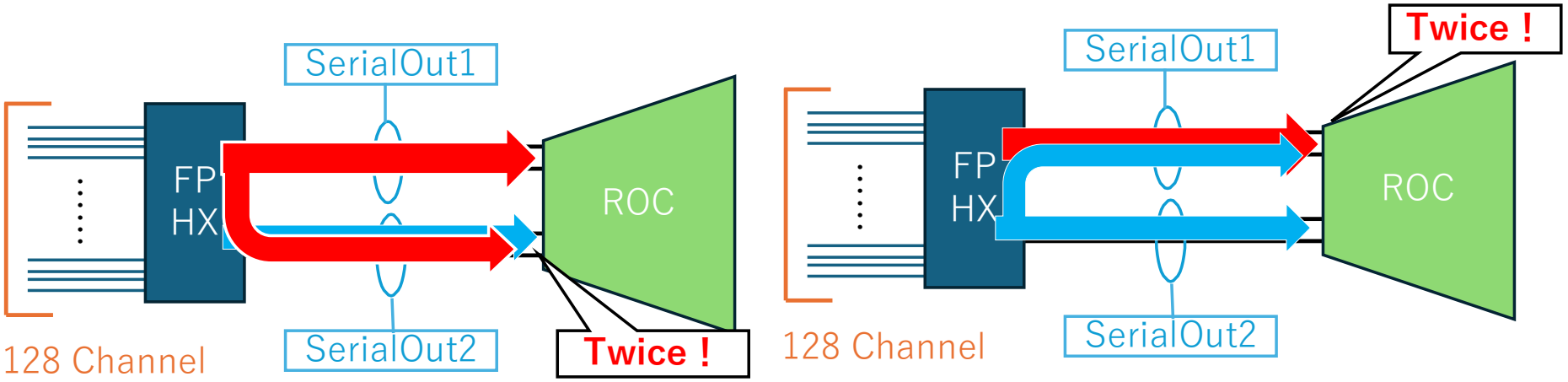
⇒ In both cases, testing the two DC patterns successfully **recovered half entry** to full entry using just a single output line.

Data rate validation

Rate dependence of half entry resolution

By using the DC function,
the data that is originally transmitted through two output lines
is instead sent and received through a single output line at twice the data rate.

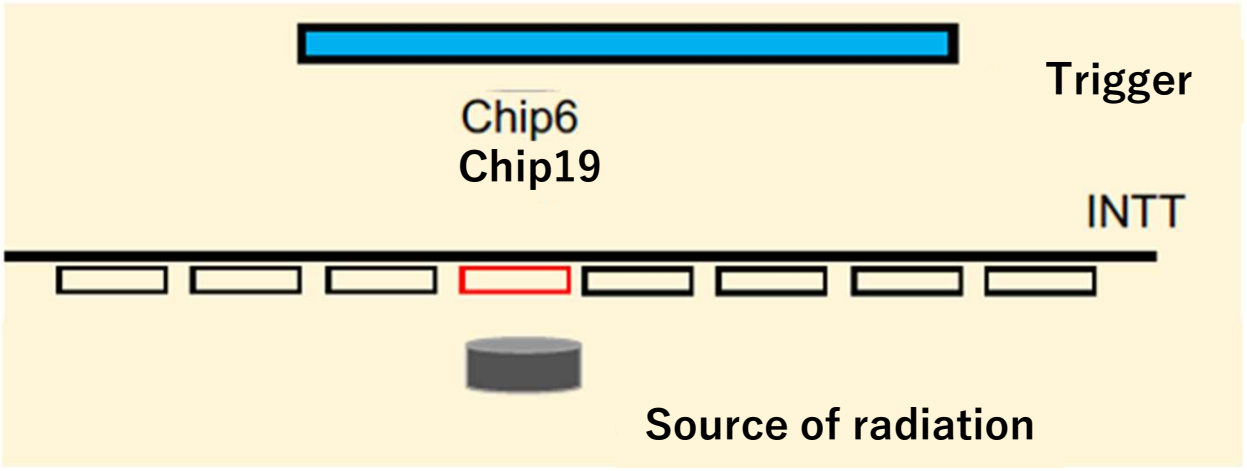
We will verify whether there is a limit to the data rate that can be handled
by a single output line.



Verification of rate dependence using a radiation source

To increase the data rate, the calibration test will not be used.
Instead, a trigger and a radiation source will be used to examine rate dependence.

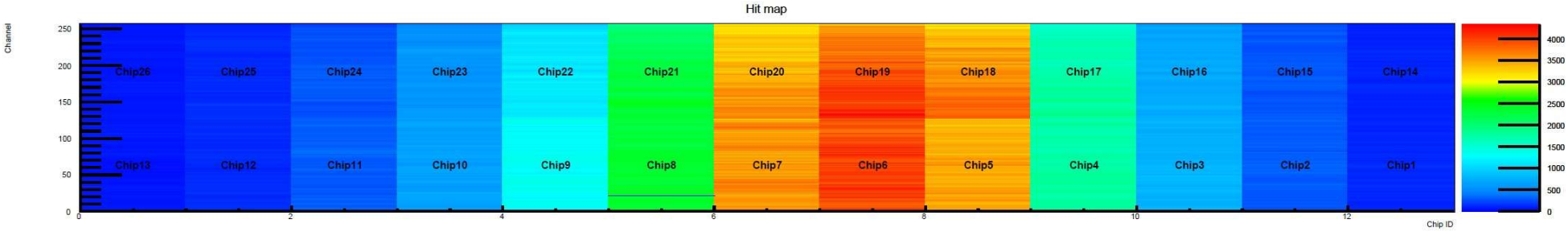
The setup involves placing an aluminum foil sheet between the radiation source and the INTT ladder, with the trigger positioned on top of the INTT ladder.
(The radiation source is placed between Chip 6 and Chip 19.)



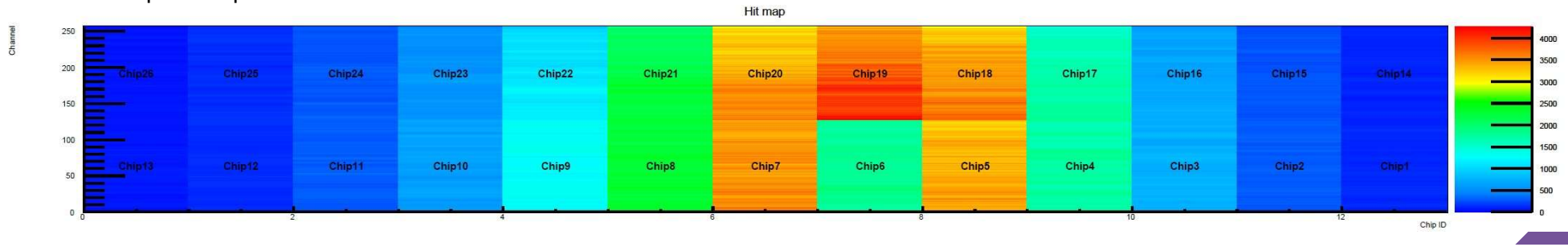
Verification of rate dependence using a radiation source

The interception board is used to cause a half-entry state in Chip 6.
In this condition, Chip 6 should be able to recover to full entry with
DC = 1110 (14).
By varying the number of aluminum foil sheets, we examined the rate dependence.

Not intercept



Intercept chip6

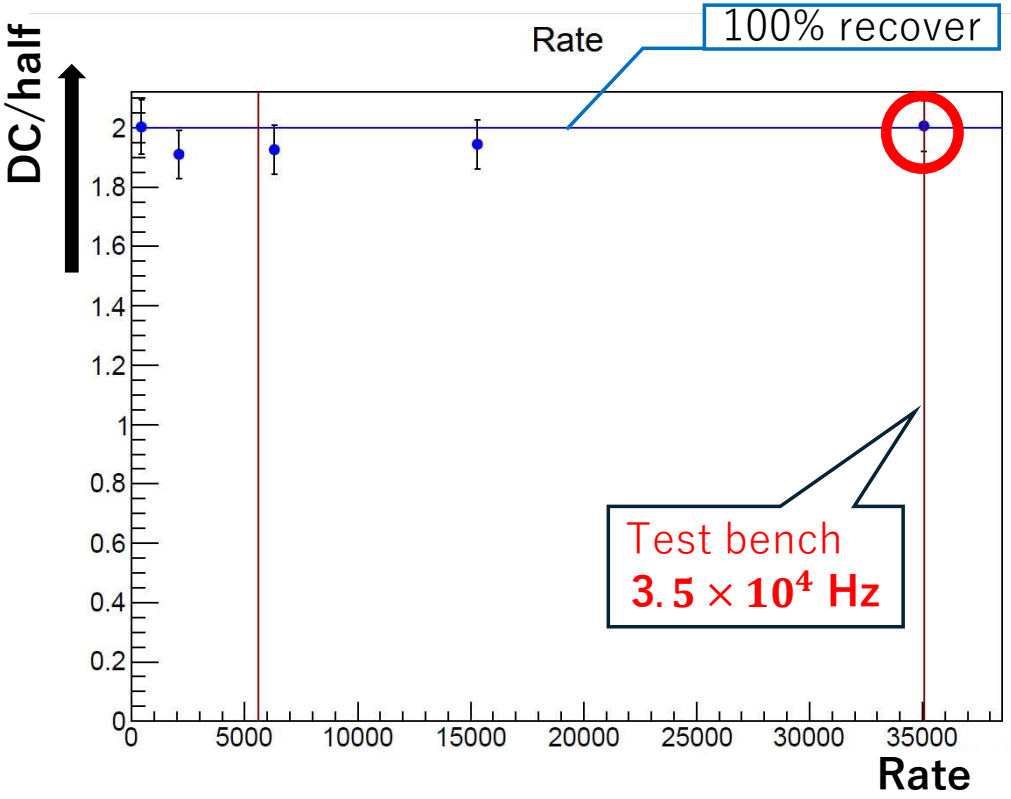


Verification of rate dependence using a radiation source

The right figure shows a graph for Chip 6:
Data rate vs.
Entry recovered by DC=14 /
Half-entry by interception board.

No rate dependence was observed.
The **highest data rate** achieved in this test bench was

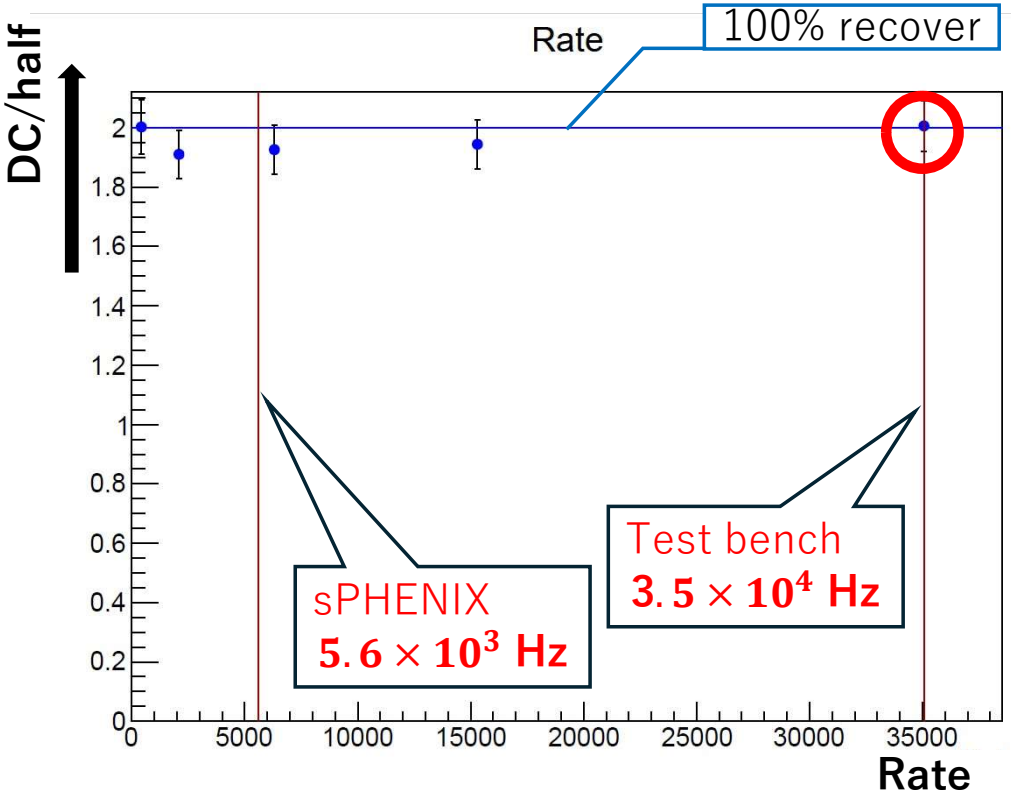
$$\mathbf{3.5 \times 10^4\ Hz}$$



Verification of rate dependence using a radiation source

We examine the data rate in sPHENIX. Since the beam intensity decreases over time, we identify the chip with the highest data rate within the initial run (**Run 54948**) and measure its rate.

The highest data rate in **Run 54948** was $\mathbf{5.6 \times 10^3}$ **Hz** ($< \mathbf{3.5 \times 10^4}$ **Hz**).



The same solution is expected to be effective in sPHENIX.

Summary

Summary

- The cause of the half entry is the **interception** of one of the two output lines.
- The **Digital Control** function built into the FPHX chip enables a solution to the half entry!
- A similar solution is expected to be effective for the half entry in the **sPHENIX** as well.

Outlook for the future of research

Half entry recovery was observed with **DC = 14**.

- we will examine whether the same recovery with **DC = 6**.

DC Bit	function	ON	OFF
Bit0	Active Serial Lines	0	1
Bit1	Accept	1	0
Bit2	Global Inject Enable	1	0
Bit3	Serial Output Order	/	/

Bit 2 controls whether to receive test pulses,
the recovery should also be possible with **Bit 2 = 0**.

- we will also test
  DC = 0010 (2) or 1010 (10)
  to verify half entry recovery.

参考文献

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[3] 杉山由佳.RHIC-sPHENIX 実験の初年度のデータを用いた中間飛跡検出器INTの動作検証
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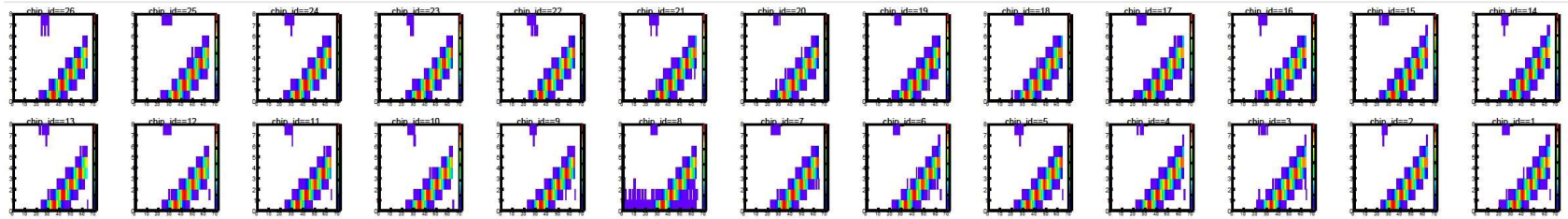
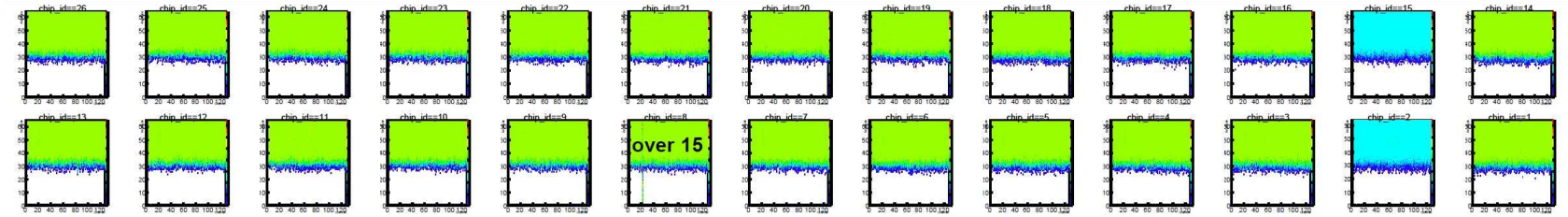
intercept chip2,15

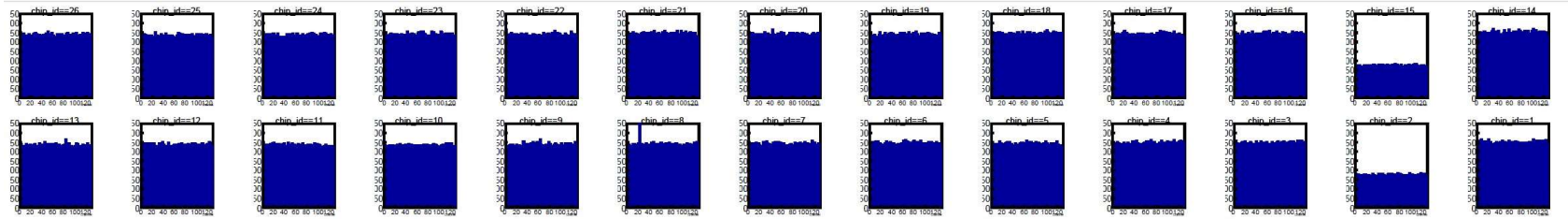
Adc vs ampl



ampl vs channel

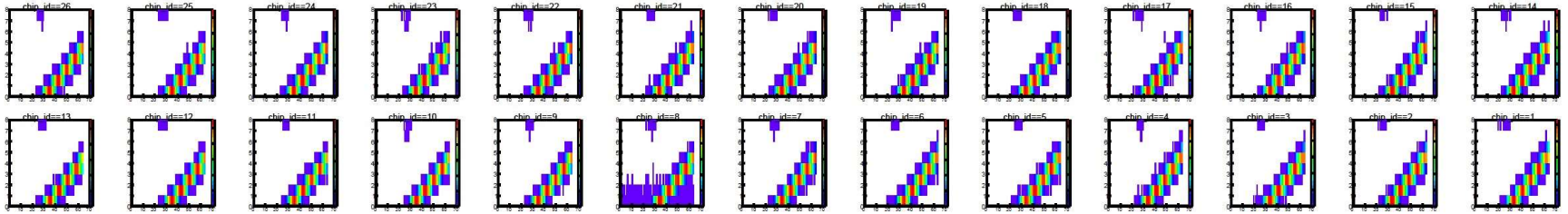


entry vs channel

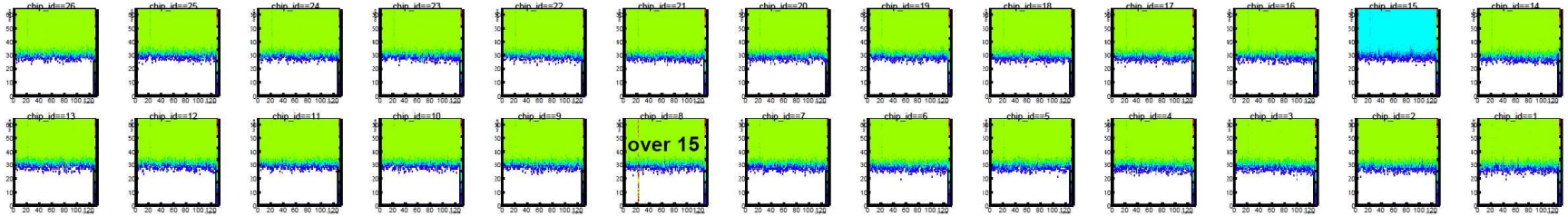


intercept chip2,15 & recover chip2 by Digital Control

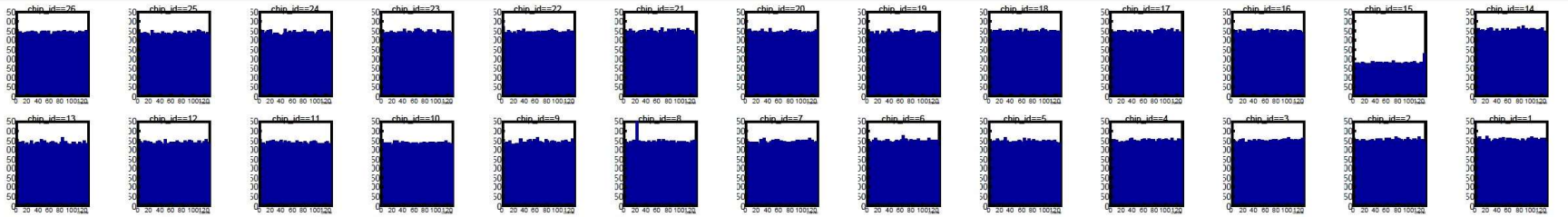
Adc vs ampl



ampl vs channel

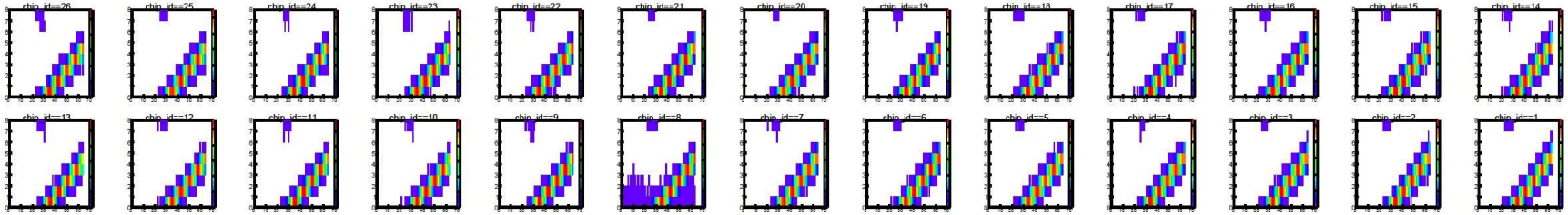


entry vs channel

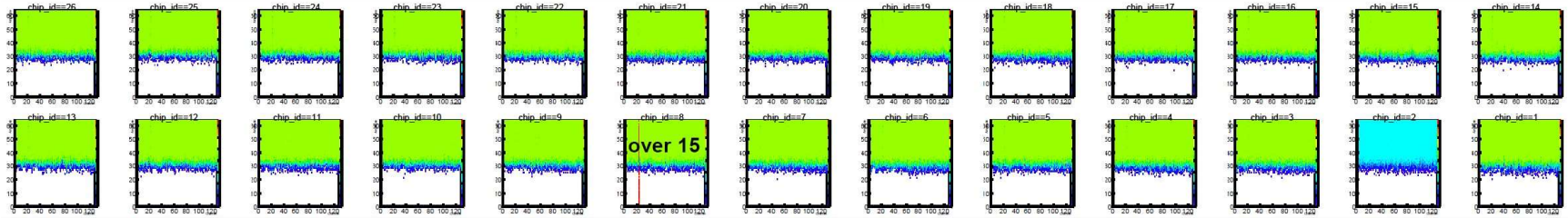


intercept chip2,15 & recover chip15 by Digital Control

Adc vs ampl



ampl vs channel



entry vs channel