The Ladder and Readout Cables of Intermediate Silicon Strip Detector for sPHENIX[★]

Y. Akiba[a,b], H. Aso[g,a], J. T. Bertaux[i,b], D. Cacace[c], K. Y. Chen[d], K. Y. Cheng[d,b], A. Enokizono[a], H. Enyo[a,b], K. Fujiki[g,a], Y. Fujino[g,a], M. Fujiiwara[e,a], T. Hachiya[e,b], T. Harada[g,a], S. Hasegawa[f], M. Hata[e,b], B. Hong[k], J. Hwang[k,b], T. Ichino[g,a], M. Ikemoto[e,a], H. Imagawa[g,a], H. Imai[g,a,b], Y. Ishigaki[e,a], M. Isshiki[e], K. Iwatsuki[e,a], R. Kan[e], M. Kano[e,a], T. Kato[g,a], Y. Kawashima[g,a], T. Kikuchi[g,a], T. Kondo[h], C. M. Kuo[d], C. Kureha[e], T. Kumaoka[a], H. S. Li[i], R. S. Lu[j], E. Mannel[c], H. Masuda[g,a], G. Mitsuka[b], N. Morimoto[e,a], M. Morita[e,b], I. Nakagawa[a,b,*], Y. Nakamura[g,a], G. Nakano[g,a], Y. Namimoto[e,b], D. Nemoto[g,a], S. Nishimori[e], R. Nouicer[c], G. Nukazuka[a], I. Omae[e,a], R. Pisani[c], Y. Sekiguchi[a], M. Shibata[e,b], C. W. Shih[d,b], K. Shiina[g,a], M. Shimomura[e], R. Shishikura[g,a], M. Stojanovic[i,b], K. Sugino[e], Y. Sugiyama[e], A. Suzuki[e,b], R. Takahama[e,b], W. C. Tang[d,b], Y. Terasaka[e], T. Todoroki[b], H. Tsujibata[e,a], T. Tsuruta[g,a], Y. Yamaguchi[b], H. Yanagawa[g,a], M. Watanabe[e,b], R. Xiao[i] and W. Xie[i]

[a]Nishina Center for Accelerator-Based Science, RIKEN, 2-1 Hirosawa, Wako, 351-0198, Saitama, Japan

[b]RIKEN BNL Research Center, 20 Pennsylvania Avenue, Upton, 11973, NY, U.S.A.

[c]Brookhaven National Laboratory, 20 Pennsylvania Avenue, Upton, 11973, NY, U.S.A.

[d]Department of Physics and Center for High Energy and High Field Physics, National Central University, No.300, Zhongda Rd., Zhongli Dist., Taoyuan City, 32001, Taiwan

[e]Department of Mathematical and Physical Sciences, Nara Women's University, Kitauoya-Higashimachi, Nara, 630-8506, Nara, Japan

[f]Advanced Science Research Center, Japan Atomic Energy Agency, 2-4 Shirakata Shirane, Tokai-mura, Naka-gun, 319-1195, Ibaraki, Japan

[g]Rikkyo University, Department of Physics, 3-34-1 Nishi-Ikebukuro, Toshima, Tokyo, 171-8501, Tokyo, Japan

[h]Tokyo Metropolitan Industrial Technology Research Institute, 2-4-10, Aomi, Koto, Tokyo, 135-0064, Tokyo, Japan

[i]Department of Physics and Astronomy, Purdue University, 525 Northwestern Ave., West Lafayette, 47907, IN, U.S.A.

[j]Department of Physics, National Taiwan University, No.1 Sec.4 Roosevelt Road, Taipei, 10617, Taiwan

[k]Korea University, Department of Physics, Anam-dong 5, Seongbuk-gu, Seoul, 02841, Korea

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ABSTRACT

A new silicon-strip-type detector was developed for precise charged-particle tracking in the central rapidity region of heavy ion collisions. A new detector and collaboration at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory is sPHENIX, which is a major upgrade of the PHENIX detector. The intermediate tracker (INTT) is part of the advanced tracking system of the sPHENIX detector complex together with a CMOS monolithic-active-pixel-sensor (MAPS) based silicon-pixel vertex detector (MVTX), a time-projection chamber (TPC), and a micromegas-based detector. The INTT detector is barrel shaped and comprises 56 silicon ladders. Two different types of strip sensors of 78 μm pitch and 320 μm thick are mounted on each half of a silicon ladder. Each strip sensor is segmented into 8×2 and 5×2 blocks with lengths of 16 and 20 mm. Strips are read out with a silicon strip-readout (FPHX) chip. In order to transmit massive data from the FPHX to the down stream readout electronics card (ROC), a series of long and high speed readout cables were developed. This document focuses on the silicon ladder, the readout cables, and the ROC of the INTT. The radiation hardness is studied for some parts of the INTT devices in the last part of this document, since the INTT employed some materials from the technology frontier of the industry whose radiation hardness is not necessarily well known.

1. Introduction

The sPHENIX detector [1, 2] at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory, USA, is a major upgrade of the PHENIX detector [3], which was decommissioned in 2017. The sPHENIX experiment collects high-statistics proton-proton, proton-nucleus, and nucleus-nucleus data, enabling state-of-the-art studies of jet modification, upsilon suppression, and open heavy-flavor production to probe the microscopic nature of the strongly-coupled quark-gluon plasma. Such measurements are complementary to those of experiments at the Large Hadron Collider (LHC) at CERN, and will also allow a broad range of cold quantum chromodynamic studies [4].

The sPHENIX detector provides precision vertexing, tracking, and electromagnetic and hadronic calorimetry in the central pseudorapidity region $|\eta|<1.1$ with full azimuthal coverage at the full RHIC collision rate of 15 kHz in Au+Au at $\sqrt{s} = 200$ GeV. A comprehensive assessment of these requirements led to the development of the reference

Table 1

Number of the INTT silicon ladders of the inner and outer layers of the INTT barrel detector

	Inner	Outer
Number of ladders	24	32

Table 2

The components and total number of channels of the INTT module and ladder. The details of silicon strip sensor type-A and B are discussed in the section 3.1.

	Component	Quantity
Silicon module	Silicon strip sensor	2 (Type-A & B)
	FPHX Chips	26
	HDI	1
	Total number of channels	3,328
Silicon ladder	Silicon module	2
	Stave	1
	Total number of channels	6,656

design shown in Fig. 1. In its overall layout, sPHENIX follows the typical geometry of modern collider detectors. The tracking system comprises a CMOS monolithic-active-pixel-sensor (MAPS) microvertex detector (MVTX), a silicon-strip intermediate tracker (INTT), and a time-projection chamber (TPC). For calibration, a micromegas based detector (TPOT) [5] partially covers the outside of the TPC acceptance. The calorimeter stack includes a tungsten/scintillating fiber electromagnetic calorimeter (EM-CAL) and aluminum/scintillator and steel/scintillator tile hadronic calorimeter (HCAL), divided into inner and outer parts. The inner HCAL sits inside the 1.4 T superconducting solenoid, which was refurbished from the decommissioned BaBar detector [6].

Figure 1: The mechanical drawing of the sPHENIX detector.

This document describes the details of the INTT silicon ladder, its readout cables, and the readout electronics card.

2. Detector Overview

The barrel-type INTT detector comprises inner and outer layers of INTT silicon ladders. Adjacent ladders are staggered to prevent dead space in azimuthal acceptance. The inner and outer barrels have 24 and 32 ladders, respectively, as summarized in Table 1. Details of the INTT barrel are beyond the scope of this document, and a separate paper is under preparation.

The designs of the INTT ladder and its readout are constrained by the specification of of the FPHX readout chip and the readout card (ROC) of the Forward Vertex (FVTX) detector[7] in PHENIX. Since the INTT reuses the FPHX design and ROCs, the rest of INTT detector was designed to be compatible with these readout chip and electronics. Thus, new copies of FPHX chips were produced for the

INTT detector, while the ROCs were recycled. The major difference between the FVTX and the INTT detectors is in the mechanical concept. The INTT is a barrel type with 2 layers, while the FVTX was a disk type with 4 layers.

Two silicon sensors and 26 FPHX readout chips [7] are mounted on a high-density interconnect (HDI) flexible print cable to form an INTT silicon module. The schematics of the silicon module are shown in Fig. 2. The layout of the silicon sensors and the FPHX chips with respect to the HDI cable is defined in the figure.

Figure 2: Schematics of the INTT module and the dimensions of each components, i.e. the silicon sensors, FPHX chips, and the HDI cable. Dimensions are given in inches, while numbers in brackets are in millimeters.

These components of the INTT silicon module and the ladder are summarized in Table 2. Two INTT modules are aligned longitudinally and glued to a carbon fiber composite (CFC) support stave to form an INTT silicon ladder, as shown in Fig. 3. To show the structures of the INTT ladder, the stackup of the components of the ladder is illustrated in Fig. 4.

Both glue and carbon fiber have high thermal conductivity to diffuse heat generated by the FPHX chips. A water cooling system removes heat from the barrel through a carbon tube integrated within the body of the stave. Figure 4 also shows the tube attached to the edge of the CFC stave, which is an inlet for cooling water.

The data of a given ladder are read out from both longitudinal ends for each silicon module. Thus, each HDI cable transmits data from half of a ladder. The data are further transmitted downstream from the HDI by a bus extender (BEX) cable [19] and a conversion cable (CC). The BEX is a 1.11 meter long flexible print cable (FPC) employing liquid-crystal polymer as a dielectric material to suppress losses in transmission lines. In both ends, the conversion
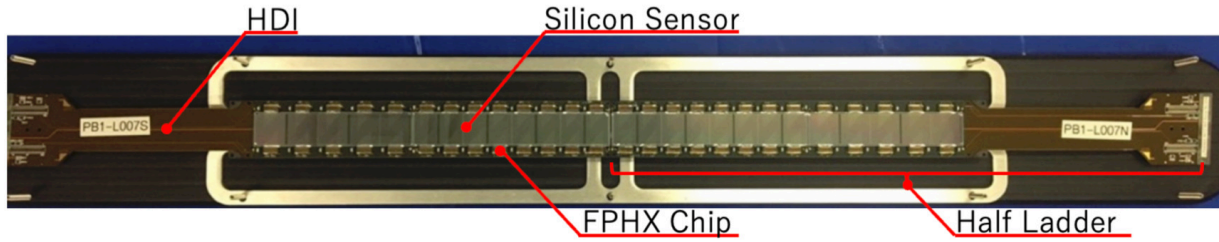
Figure 3: Photo of the INTT ladder with sensors facing up. Note the center line dividing the two halves of the sensor and the rows of FPHX chips along the sensor edges.
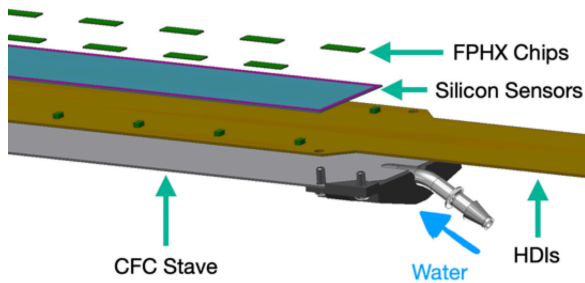

Figure 4: The stackup of the components of the INTT ladder.

cable comprises three components; 1) μ-coaxial harness, 2) power and ground cables, and 3) connector print boards. The downstream end of the conversion cable is connected to the read-out card (ROC) which collects data from up to seven half-ladders, and then transmits reformatted data to further downstream electronics via an optical fiber connection. The downstream electronics beyond the ROC and data acquisition system are beyond the scope of this document.

3. INTT Ladder

This section describes the electrical components and support systems used to read out and power the INTT. The silicon-strip sensors and the FPHX readout chips are introduced in subsections 3.1 and 3.2, respectively. The HDI that provides power, bias voltage, and slow-control signals to the sensor is discussed in subsection 3.3. The stave support structure is discussed in subection 3.4. The material budget of the ladder in the radial direction is discussed in subsection 3.5. Lastly, the dead space of the silicon ladder is evaluated in subsection 3.6.

3.1. Silicon Sensors

The silicon-strip sensor [8] is single-sided and AC-coupled. The design is based on and modified from the PHENIX FVTX silicon mini-strip sensors [7]. The sensors (model S14629-01), as well as the FVTX sensors, were fabricated by Hamamatsu Photonics K.K. There are two types of sensors (type-A and type-B), which are distinguished by the length of strips and number of blocks. The type-A sensor has an active area of 128×19.968 mm that is segmented into

8 rows and 2 columns of blocks, each of which consisted of 128 strips with 78 μm pitch and 16 mm long. Each strip oriented in the longitudinal direction. Similarly, the type-B sensor has an active area of 100×19.968 mm that is segmented into 5 rows and 2 columns of blocks, each of which comprises 128 strips in 78 μm pitch and 20 mm long that are also oriented in the longitudinal direction. Table 3 summarizes these dimensions.

The small gap between adjacent blocks where the DC pads are laid out on the surface is completely active. The sensors were fabricated with p-implants on a 320 μm thick n-type substrate. The strips are AC-coupled and biased through individual 15 MΩ poly-silicon resistors to a typical operating voltage of 100 V. The aluminum metallization width of the strips is 20 μm, which is wider than the implant width of 10 μm. This provides field-plate protection against micro discharges, which are known to grow with radiation-induced increases in the leakage current. These specifications of the silicon sensor are summarized in Table 4. The strips are also protected by two p-implant guard rings and an n+ region between the guard rings and the sensor edge. These designs follow from the silicon-strip sensors of the FVTX [7]. Figure 5 shows details of the sensor layout, including guard rings, bond-pad locations, and mechanical fiducial marks.

In Fig. 6, the strip runs horizontally (longitudinal direction). The readout lines of each strip are wired perpendicular to the strips orientation using double-metal technology. The other end of the readout lines are connected to readout pads, which transmit data to the FPHX chips using a wire bonding. The strips channel 0 to 127 are wired to the readout pads laid out on the bottom of the figure, while the strips from 128 to 255 are wired to the pads on top of the figure.

3.2. FPHX chip

A custom 128-channel front-end ASIC, the FPHX[10], was developed at Fermilab for use in the PHENIX FVTX Detector [7]. The size of the chip is 9×2 mm. The chip is operated at 2.5 V and consumes power as low as 64 mW per chip. The FPHX is a mixed-mode chip with two major and distinct sections: the analog front-end, and the digital back-end.

The analog section consists of an integration/shaping stage, followed by a 3-bit ADC stage. The FPHX chip integrates and shapes signals from 128 channels of strips,

Table 3
The dimensions of type-A and type-B silicon strip sensors. [8]

Item	Type-A	Type-B	Type-A+B Total
Physical dimensions	130.0 mm × 22.5 mm	102.0 mm × 22.5 mm	232.0 mm × 22.5 mm
Active area dimensions	128 mm × 19.968 mm	100 mm × 19.968 mm	228 mm × 19.968 mm
Active area fraction	87.4%	87.0%	
Active cell dimensions	16 mm × 19.968 mm	20 mm × 19.968 mm	N/A
# of cells	8	5	13
Active block dimensions	16 mm × 9.984 mm	20 mm × 9.984 mm	N/A
# of blocks	16	10	26
Number of blocks per cell		2	
Number of strips per block		128	
Strip pitch		78 μm	
Number of strip channels	2,048	1,280	3,328
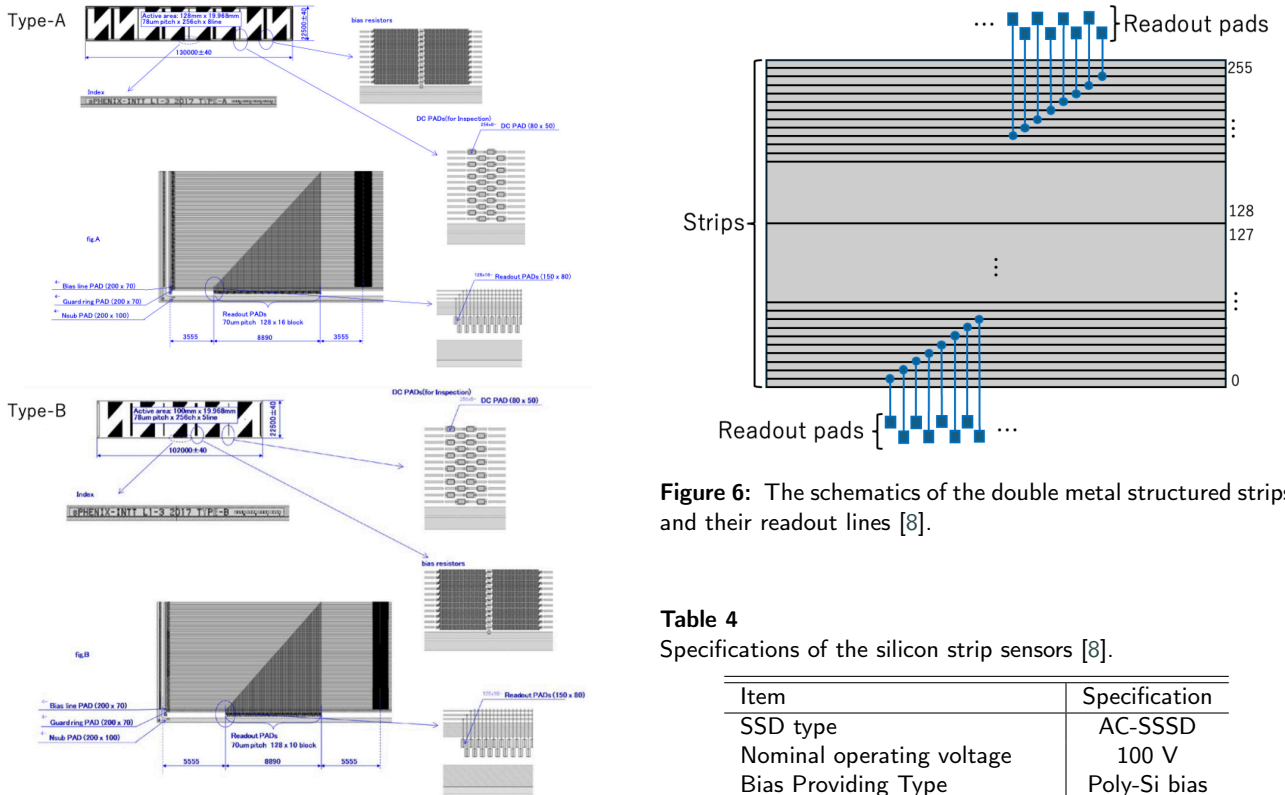
Figure 5: The layout design of the type-A (top) and type-B (bottom) silicon sensors [8].

Figure 6: The schematics of the double metal structured strips and their readout lines [8].

Table 4
Specifications of the silicon strip sensors [8].

Item	Specification
SSD type	AC-SSSD
Nominal operating voltage	100 V
Bias Providing Type	Poly-Si bias
Poly-Si resistance	15 MΩ
Silicon thickness	320 μm
Strip implant width	10 μm
Strip readout aluminum width	20 μm

digitizes and sparsifies the hit channels for each beam crossing, and serially reads out the digitized data.

The back-end is a novel, triggerless, data-push architecture that permits operation without deadtime and high-speed readout with very low latency. It has been designed to process up to four hits within four RHIC beam crossings. Although it takes longer, it can process more than 4 hits from a given crossing.

A fully processed hit pattern is zero suppressed, contains a 7-bit time stamp in the unit of RHIC repetition frequency 9.4MHz (1/106 ns), a 7-bit channel ID, and a 3-bit ADC value. The data word is output over two LVDS serial lines in alternating order at a rate of up to 200 MHz. A summary of FPHX specifications [9][10] is given in Table 5.

In addition, to be as self-sufficient as possible, the FPHX chip provides its own internal bias voltages and currents with minimal external support circuitry. For the user to be able to control the internal parameters and biases, a digital slow-control interface is provided on each chip to enable

Table 5
Specifications of the FPHX readout chip [9].

Item	Specification
Dimensions	9 mm × 2 mm
Operation voltage	2.5 V
Power consumption	64 mW
Number of Channels	128
ADC channels	3 bits
Data Transmission	200 MHz

Figure 7: Seven layer structure of HDI.

172 programming. Adjustable parameters include gain, thresh-
173 old, rise time, fall time, input transistor bias current, channel
174 masking, and several additional fine-tuning parameters [9].

3.3. High-density interconnects

176 The HDI is a flexible print circuit board used to read out
177 a half ladder, which comprises two silicon sensors with 26
178 FPHX chips. The basic layer design of the HDI structure
179 follows from the FVTX [7]. The geometric constraint for the
180 silicon ladder is somewhat less stringent for the INTT than
181 for the FVTX. Thus, the circuit design parameters such as
182 line and space are relaxed from the FVTX, which results in
183 an improved yield rate in the fabricating process.

184 The HDI was designed by HAYASHI-REPIC Co., Ltd.
185 and fabricated by YAMASHITA MATERIALS CORPORA-
186 TION in Japan. The width of the HDI is 38 mm in the
187 sensor area and 43 mm at the connector end. The length is
188 398 mm, which is the longest limit of industry fabrication for
189 the multilayer FPC in an automated manner using dedicated
190 fabrication machines.

191 The HDI is seven-layered, with each layer comprising
192 9 μm thick electrolytic copper foil, 12.5 to 50 μm thick
193 polymide, and 15 to 25 μm thick resin glue. The total
194 thickness is 418 μm in the sensor area. As discussed in
195 subsection 3.5, the total thickness of copper layers is 68 μm,
196 and is the greatest contribution to the material budget of the
197 INTT ladder. The top and bottom copper foil layers were
198 plated with 15 μm of copper[1]. The cross section of the seven-
199 layer structure of the HDI is shown in Fig. 7.

200 The schematic of each layer is shown in Fig. 8. From
201 top to bottom, each layer is for: transmitting bias for the
202 type-B silicon sensor (L1), analog ground (L2), signals (L3),
203 DC power for the analog and digital parts of FPHX (L4),
204 signal (L5), digital ground (L6), and for the type-A sensor
205 and signals (L7). There are two thermostats implemented on
206 the L7 to monitor the cooling status of heat generated during
207 operation from the FPHX chips.

208 There are 122 signal lines per HDI cable: 52 pairs of
209 output data lines, 8 pairs of slow-control & clock LVDS
210 lines, and two dedicated lines to inject calibration pulses to
211 the FPHX. Signal transmission lines are mainly placed in
212 layers 3 and 5 to be shielded from external electromagnetic

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[1]The copper plate was 15 μm thick for the 1st and 2nd batches of the
HDI production. The thickness increased to 25 μm for the 3rd batch in HDI
production. The total radiation length of the silicon ladder was increased by
3%.
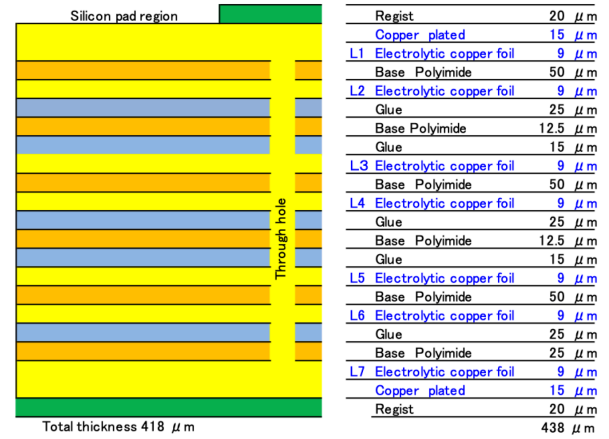
Table 6
Specifications of the HDI cable. The characteristic impedance
is for the LVDS pair.

Item	Specification
Dimensions	398 mm × 38 mm
Width of connector ends	43 mm
Total thickness (sensor pad region)	418 μm
Conductive material	Copper
Dielectric material	Polymide
Number of layers	7
Number of signal lines	122
Line and space	60 μm & 60 μm
Characteristic impedance	100 Ω

213 (EM) fields by keeping these layers between solid-copper
214 layers which are assigned for either analog or digital grounds
215 or the DC power. The line and space are both 60 μm. The
216 characteristic impedance is designed to provide a 100 Ω
217 differential for these LVDS pair lines to ensure matching
218 with the rest of the readout cable chain.

219 Some signal lines in the sensor region L7 are not of
220 the same design as in the FVTX. These signal lines were
221 changed to keep the HDI width as narrow as possible and
222 would not have otherwise fit within the signal layers. This
223 narrow width enables the barrel detector to be as round as
224 possible by minimizing physical interference between adja-
225 cent ladders. Because the back plane of L7 is not shielded
226 by the solid foil ground nor the power layers, the signal lines
227 are exposed to external EM fields. Thus, the length of the
228 lines were kept as short as possible (centimeter lengthscale).
229 Figure 9 shows a photo of the HDI cables with L1 and L7
230 face up. Table 6 summarizes the major specifications of the
231 HDI cable.

232 Pairs of connectors for data, LV power for the FPHX, and
233 grounds are implemented in the end of the HDI. The model
234 of data connector is the Hirose Co. DF18C-100DP-0.4V(51)
235 plug, which consists of 100 channels with a 400 μm pitch
236 between conducting pins. Also, there are two bias connectors
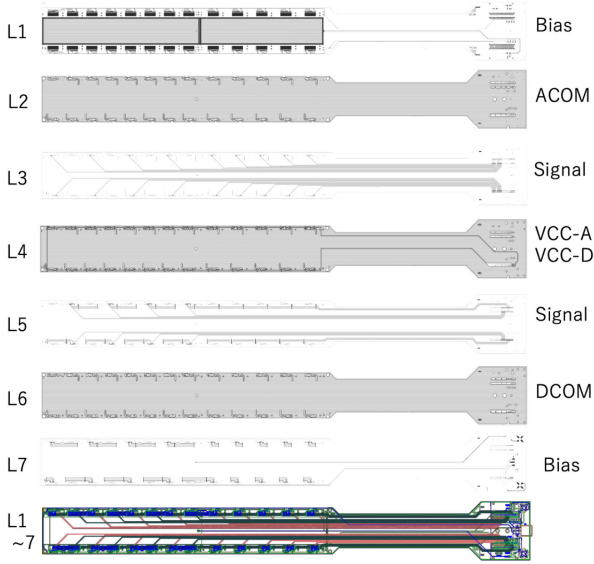
Figure 8: The schematic of each layer of the HDI. The ACOM and DCOM layers provide analog and digital grounds to FPHX chips, respectively. The 2.5 V power lines for the analog and digital parts of the FPHX chip are electrically isolated from each other within L4. The bottom schematic figure shows (in different colors) the overlay of line patterns for all seven layers.
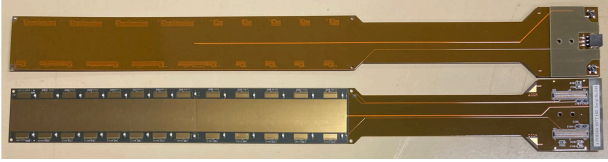

Figure 9: Photo of the HDI cables with L1 face up (bottom) and L7 face up (top).

and a 3-pin thermostat connectors implemented in the end of the HDI.

3.4. Stave

The stave is a mechanical support made mainly of carbon fiber composite (CFC) skins. The stave itself, plus an extension for mechanical attachment, spans 497 mm long and 38 mm wide. This matches the HDI width around the sensor area and accommodates two silicon modules per stave, forming the INTT silicon ladder. The heat load expected from each half ladder is 64 mW × 26 FPHX chips, or approximately 1.7 W. The total heat load over the entire INTT is about 186 W for 112 half ladders.

The stave is required not only for the rigidity of the support structure, but also for high thermal conductivity to dissipate local heat generated by the FPHX chips. The main component of the stave is made of a carbon fiber reinforced plastic prepreg (CFRP). The GRANOC prepreg sheet model NT91500-520S of Nippon Graphite Fiber Co. was used, which comprises 25R epoxy and XN-90 carbon fiber with a high thermal conductivity of 500 W/mK, with

Table 7
Specifications of the CFRP prepreg.

Item	Specification
CFRP prepreg	NT91500-520S [12]
Carbon fiber	XN-90
Resin	25R epoxy
Resin weight fraction	20 %
Density	2.19 g/cm^3
Thermal conductivity	500 W/mK
Tensile module	860 GPa
Tensilie strength	3430 MPa
Thickness	100 μm

resin weight fractions of 20% [12]. The thickness of 0.10 mm with density of 2.19 g/cm^3 prepreg provides satisfactory mechanical strength with tensile module and strength of 860 GPa and 3430 MPa, respectively. Table 7 summarizes the specifications of the CFRP prepreg.

Figure 10 shows the stack up of the stave and the mechanical attachments of its edge. The shells of the stave are CFC plates at the top and bottom are flat and formed, respsectively. The formed plate is U-shaped to accommodate the 3 mm diameter cooling tube between two CFC plates with 3 mm thick ROHACELL 110 RIST form [13] that tapers down near the edge forming a structural core. The cooling tube is made of Toreyca T700C carbon fiber prepreg [11] fabricated by Kimuraya Co., Japan. The NT91500-520S sheet is unidirectional with high thermal conductivity. To provide omnidirectional rigidity, each CFC plate has three unidirectional sheet layers with high thermal conductivity oriented in longitudinal, transverse, and longitudinal directions. The thickness of the CFC plate is 0.33 mm and the total thickness of the stave is 3.76 mm.
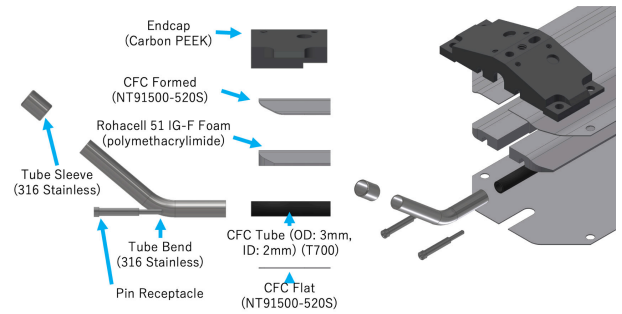
Figure 10: The mechanical design of the edge of the stave. The HDI is assembled on the bottom flat CFC plate.

The mechanical attachment of both edges of the stave comprise the end caps, SUS316 cooling-tube extensions, and pairs of pin receptacles manufactured by Mill-Max MFG Co. for grounding. The endcap is made of Ketron CA30 PEEK [14] manufactured by Mitsubishi Chemical Co. The stainless tubes and the cooling tubes were glued using Henkel LOCTITE EA 9396 adhesive [15]. The rest of the stave pieces are assembled using the graphite conductive

Table 8
The material list of stave components and specifications. The total thickness is at the sensor region.

Item	Model/Specification
Dimensions	497 mm × 38 mm
Total thickness	3.76 mm
Adhesive for stave assembly	MasterBond EP75-1 [16]
Structure core	ROHACELL 110 RIST [13]
End cap	Ketron CA3 PEEK [14]
CFC cooling tube	Toreyca T700C [11]
Cooling tube extension	SUS316
Cooling tube adhesive	Henkel LOCTITE 9396 [15]

Table 9
The material budget of the silicon ladder. TC-2810 is the thermally conductive glue. The radiation thickness of the HDI listed in the table is for production batches 1 and 2.

Item	Thickness mm	Radiation Length X/X_0 %
Silicon Sensor	0.32	0.34
Silver epoxy	0.01	0.02
HDI	0.42	0.43
TC-2810	0.05	0.02
Stave	3.76	0.33
Total	4.56	1.14

EP75-1 epoxy adhesive (MasterBond Co.) [16]. Figure 11 shows the engineering drawing of the INTT stave. Table 8 summarizes the material list of stave components and specifications.
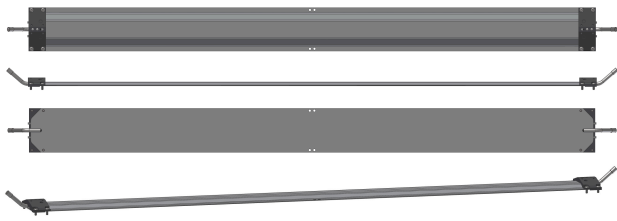
Figure 11: The INTT stave drawings from four different view angles. The HDI is assembled on the bottom flat CFC plate.

The staves were fully fabricated by Asuka Co., Japan including the baking process of the CFC plates. To ensure meeting the requirements, the following four tests were applied to staves and to every cooling tube (after the stainless extensions were glued). Only components that passed examination were used.

1. Burst test : Tube does not burst for 1 hour at 60 ± 2 psi
2. Leak test : less than 0.2 ml-mbar/min
3. Heat-cycle test : $40 \leftrightarrow 0°C$ (one cycle)
4. Flatness < 100 μm of the flat side of the stave and alignment positions are within specified tolerance

The staves were assembled with only those cooling tubes that passed the 1 and 2 examinations to keep the yield rate of the stave production reasonably high. The assembled staves were then examined for the above items 3 and 4.

3.5. Material Budget

Table 9 summarizes the material budget of the silicon ladder. The total thickness of the silicon pad area of the ladder is 4.57 mm and its effective radiation length X/X_0 is 1.14%. The largest contributions to the budget is the HDI (with radiation length is $X/X_0 = 0.43$%), and the silicon and staves with radiation lengths $X/X_0 = 0.34$% and $X/X_0 = 0.33$%, respectively.

The material budget of the HDI is largely governed by the copper layers. As shown in Fig. 7, there are 7 layers of

Table 10
The effective thickness of the HDI's copper layers.

Layer	Function	Residual copper fraction %	Effective thickness μm
1	Bias + AGND	71.3	17.1
2	AGND	93.5	8.42
3	Signal	6.5	0.59
4	Power	94.0	8.64
5	Signal	7.2	0.65
6	DGND	93.2	8.38
7	Bias+Signal	4.7	1.12
Total			44.7

9 μm thick copper which total 63 μm. Furthermore, both top and bottom surface layers are plated with 15 μm thick copper[2]. While the simple stack up of these copper sheets results in 93 μm, the effective amount of copper in the signal layers is much less than solid ground layers.

Table 10 summarizes the effective copper thickness of each layer, which was estimated based on the residual copper fraction after the etching process of the HDI fabrication. The effective total thickness is estimated to be 44.7 μm, approximately 48% of the 93 μm total stack-up thickness, with corresponding radiation length X/X_0 is 0.31%. The total thickness of polymide and glue layers is 325 μm with X/X_0 of 0.11. The total radiation length of the HDI in the silicon pad area is thus 0.43%.

The silicon sensors were glued on the bias pads of the top layer of the HDI using electrically conductive silver epoxy, i.e. Henkel LOCTITE ABLESTIC 2902 adhesive. The average thickness of the epoxy was designed to be 9 μm based on the 50 μm thick glue mask, which has total of 295 glue potting holes with 2 mm diameter each. The radiation length of the silver epoxy was then calculated to be $X/X_0 = 0.02$% based on the mixing ratio of the silver powder and the epoxy of 0.21:0.79 [17]. Due to the short radiation length $X_0 = 8.54$ mm of the silver material, the contribution of

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[2]The thickness of the copper plate was 20 μm only for the last production batch, which increases the radiation length of the third batch HDIs by $X/X_0 = 0.02$%.

Table 11
The dimensions of the dead space and region in the longitudinal direction of the half ladder.

Longitudinal	Physical	Active
Dead space I	0.5 mm	0 mm
Type-A	130 mm	128 mm
Dead space II	0.2 mm	0 mm
Type-B	102 mm	100 mm
Total	132.7 mm	228.0 mm
The fraction of longitudinal active length		98.0%

Table 12
The physical and active area of the half ladder.

Transverse	Physical	Active
Type-A & B	22.5 mm	19.968 mm
The fraction of transverse active length		88.7%

Table 13
The physical and active region of the half ladder.

	Physical	Active
Area	5235.75 mm^2	4552.70 mm^2
The fraction of active area		87.0%

the silver epoxy to the total material budget can be non-negligible. Without the glue mask, the contribution of the 50 μm thick silver epoxy is as significant as 12% of the total material budget.

To diffuse the heat generated by the FPHX chips, highly thermally conductive epoxy adhesive glue, 3M^{TM} TC-2810 [18], was used to assemble the HDI and the stave. The radiation length for the 50 μm thick the epoxy makes a very small contribution to the total material budget of the silicon ladder, unlike the silver compound one.

3.6. Dead Space

Due to the precision limit of the silicon sensor alignment during the assembly process of the silicon sensors on the sensor pads of the HDI, there are small dead spaces between the edge of the type-A sensor and the tip of the HDI (dead space I), and also the type-A and type-B sensors (dead space II). They are 0.5 and 0.2 mm, respectively, as shown in Figure 12.
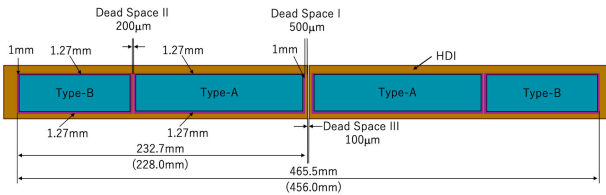
Figure 12: Dead spaces of the INTT ladder. The number in parentheses is the longitudinal length of the active region of the type-A and B sensors altogether.

As the result of the dead spaces in the silicon alignment, the total distance from the boundary of the two half ladders to the large rapidity end of the type-B sensor is 232.7 mm, while the length of the active region of type-A and type-B sensors is 228.0 mm as tabulated in Table 3. This results in 98% coverage of the active region in the longitudinal direction as summarized in Table 11. On the contrary, there is no additional dead space originating from the alignment in the transverse direction. The fraction of the active region in the transverse direction is thus 88.7% as tabulated in Table 12. The resulting fraction of the active area of the half ladder is 87.0% as tabulated in Table 13.

Lastly, there is another 0.1 mm of dead space between two half silicon ladders (Dead Space III in Figure 12) originating from the alignment precision of the two half silicon modules on the stave. The resulting physical length between the large rapidity end of the type-B sensors of two half ladders is 465.5 mm, while the total longitudinal length of the active regions of 4 silicon sensors is 456.0 mm. This dead space is relatively minor enough, the fraction of active area still stays as 98.0% in the longitudinal direction for the full ladder.

4. INTT Readout Cables and Front End Circuit Board

Because the entire INTT barrel must fit within the inner diameter of the TPC detector [1, 2], the signal from the barrel must be transmitted all the way to the outside of the TPC volume. The ROCs from the FVTX detector, which are downstream electronics for signal processing, cannot fit within the inner diameter of the TPC.

Massive raw data generated from the INTT must be transmitted at high-speed to the ROC through a curved cable path for longer than 1 m. Because no commercial cable satisfies the requirements, a novel bus-extender cable was developed based on the FPC. This technology simultaneously satisfies the requirements of high-density signal lines, flexibility, and long cable length. In contrast, the specification of line and space of the bus extender prevented its connector-end design to be compatible with the input connector ports of the existing ROC. Therefore, another 15 to 25 cm conversion cable was developed to interconnect between the bus extender and the ROC. Flexibility in three-dimensions for the conversion cable is required to guide the connection smoothly without introducing any stress at the ROC input connector. This is needed to absorb the geometrical mismatch of the downstream end of the bus extender and the corresponding input connector location of the ROC.

The schematics of the INTT silicon ladder and full readout cable chain up to the ROC is depicted in Fig. 13. The data of each half ladder is readout from opposite side of the full ladder and processed by different ROCs.
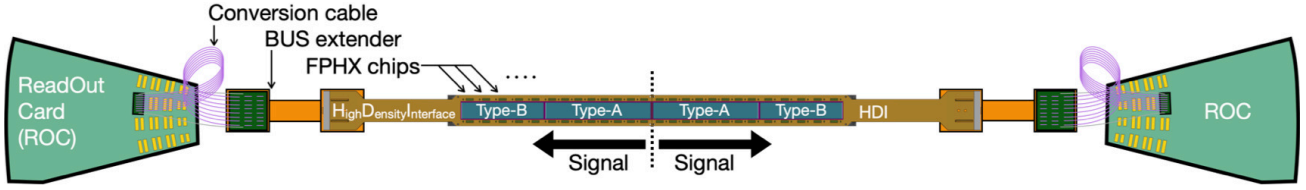
Figure 13: The schematics of the INTT silicon ladder and full readout cable chain up to the ROC.

4.1. Bus Extender Cable

Only key features of the bus extender (BEX) are described here, because details of the BEX cable are discussed elsewhere [19]. This FPC cable comprises four layers of three flexible-copper-clad laminate (FCCL) as shown in Fig. 14. The top and third layers are for the digital and analog grounds, respectively. The second layer is used for signal lines. The bottom layer has the power supply lines for the FPHX chips. The choice of the four-layer structure, instead of the seven-layer structure of the HDI, is primarily driven by fabrication constraints. The yield rate is a big concern for the BEX. The main driver is the signal layer due to its required microfabrication accuracy over the extraordinary length of 1.11 meters. Reducing the number of signal layers was chosen to minimize the risk in the fabrication process. All of the BEX signal lines were thus integrated into a single layer.

Table 14
Specifications of the BEX cable.

Item	Specification
Dimension	1.11 m × 34 mm
Width (connector region)	43 mm
Total thickness	398 μm
Dielectric material	LCP
Dielectric model	Panasonic FELIOS [20]
Dielectric layer thickness	100 μm
Bonding sheet thickness	25 μm
Number of layers	4
Number of signal lines	122
Line and space	130 & 130 μm
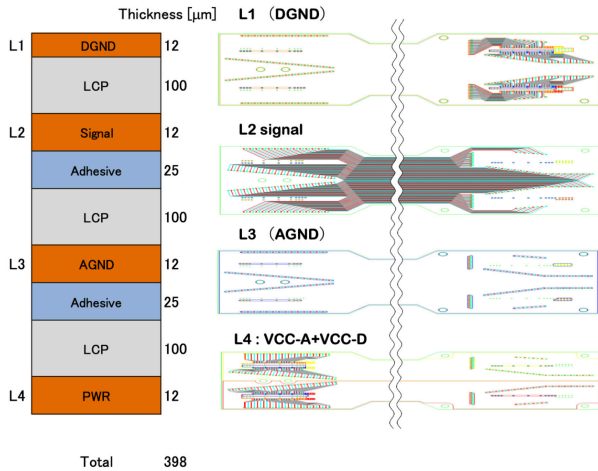
Figure 14: Four layer structure of the BEX (left), and schematics of each conductive layer (right) from L1 to L4.

Polymide is the most popular market choice of a dielectric material for the FPCs and its fabrication technology is well established in industry. For the BEX case, liquid crystal polymer (LCP) was chosen as the dielectric material due to its lower transmission loss of signal amplitude and the availability of thicker FCCLs in the industrial market compared to polymide. These features are advantageous for the bus extender, whose design is strictly constrained by the

precision and yield limit in the fabrication process due to its extraordinarily long length.

The realistic limit of the line and space for the BEX were both found to be 130 μm. To achieve a reasonable yield rate in the fabrication factory, which was Printed Denshi Kenkyusho Co., Ltd. Given the line and space, the thickness of the dielectric material is required to be as thick as 100 μm to match the differential characteristic impedance of 100 Ω. While such a thick polymide is not available in the industrial market, the 100 μm thickness is available in the FELIOS model LCP from Panasonic Industry Co., Ltd. [20]. The key specifications of the LCP to make the low transmission loss possible are the dielectric constant $\epsilon_r = 3.3$ and the dissipation factor $\tan \delta = 0.002$.

For the bonding sheet, a specially optimized model for LCP was employed with thickness of 25 μm chosen for having a low dielectric constant. As a consequence of R&D, this was also a crucial choice to achieve decent yield rate in the through-holes plating process [19] by Taiyo Manufacturing Co., Ltd. because the fabrication technology for the LCP is not as well established as for the polymide. Table 14 summarizes the specifications of the BEX cable.

Pairs of DF18C-100DS-0.4V(81) receptacle connectors manufactured by Hirose Electric Co. Ltd. are implemented at both ends of the bus extender as shown in Fig. 15. The space between a pair of DF18 plugs is 26 mm which is incompatible with the 10 mm spacing of the input connector pair of the ROC. This extra spacing between the connector pairs of the BEX is caused by the difficulty to wire 122 signal lines of 130 μm line & space into the short connector spacing. Due to the incompatibility of the connector layout

Table 15
The performance of the BEX cable. The insertion loss and return losses are the performance at 200 MHz. The characteristic impedance is the differential of the LVDS pair.

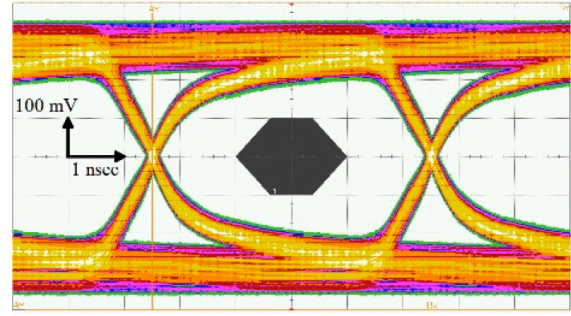| Item	Performance
Insertion Loss	-2.7 dB
Return Loss	-23 dB
Characteristic impedance	90 Ω

Figure 16: The measured eye-diagram of the BEX as a result of transmitting 200 MHz signals for 1 million times [19].

between the BEX and the ROC, a conversion cable was introduced which converts the connector spacing from the BEX to the ROC spacing.

Figure 15: A photograph of the 1.11 meter long BEX cable.

The bus extender successfully moderated the signal attenuation. However, the signal level is still questionable due to the extraordinarily long cable length as a multilayered FPC. The performance of signal transmission was evaluating with measurements using each of the following methods: 1) S-parameters, 2) eye-diagram, and 3) time-domain reflectometry (TDR). From the S-parameter measurement, the insertion and reflection losses are -2.7 and -23 dB, respectively at 200 MHz. The measured eye diagram is shown in Fig. 16. The waveform is confirmed to exhibit a sufficient margin to a defined mask[3] by observing 1 million waveforms of the 200 MHz signal (see the solid hexagon in the middle of Fig. 16). The measured characteristic impedance was 90 Ω differential in the TDR measurement. This is 10% smaller than the default 100 Ω, it is confirmed to be permissible by the return loss measurement of the daisy chain with the conversion cable as discussed in subsection 4.2. Table 15 summarizes the performance of the BEX cable.

4.2. Conversion Cable

As discussed in previous sections, the FPC is the first choice of technology to satisfy the high-performance requirements of signal transmission, high signal-line density, and flexibility. However, it is difficult for the FPC to satisfy

[3]Private communication with the FPHX chip developers.

an additional and unique requirement as the last stage of the readout cable series. The requirement is flexibility in three dimensions to connect the downstream end of the BEX and the input connector ports of the ROC board without introducing any stress at the connection. Due to the geometrical mismatch between the INTT barrel ladders and the input connector layout of the ROC, flexibility in three dimensions is crucial for the conversion cable. If the FPC cable has directivity, then stress is induced at the connector end, which would bend the cable to the transverse direction of the cable plane.

A μ-coax technology was chosen. Although the signal line density cannot be as high as the FPC, the three dimensional flexibility offers a good trade-off in the INTT readout design. According to an engineering study, due to its lack of flexibility the FPC solution would require as many as 14 different designs in curving and length to interconnect mismatching connector geometries between the BEX and input connectors of the ROC. Furthermore, spare cables of all designs would be needed for risk management, which leads to high cost inefficiency. The μ-coax solution reduces the number of designs to be only two in different lengths.

The CABLINE-UX II model manufactured by I-PEX Inc. [21] was employed as the last stage of the signal transmission cable chain for the INTT ladder. The AWG#44 harness is made of silver-plated copper alloy with a center conductor insulated by $30\mu m$ thick perfluoroalkoxy alkane (PFA) dielectric material from tinned copper alloy with wire wrapping in the outer spiral shield. The shield is covered by the outermost jacket made of the PFA, as well forming a four-layered coaxial cable with total thickness of 0.24 $\pm$ 0.01 mm. The characteristic impedance of the harness is 45 Ω (90 differential for a LVDS pair). A slim plug and small connectors are assembled for both ends of the harnesses to bundle 50 harnesses in the wire spacing with 0.25 mm pitch. Finally, the harness bundle is wrapped by an acetate cloth adhesive tape.

The conversion cable interconnecting between the BEX and ROC comprises three μ-coax bundles, two power and two ground cables, and the PC boards in both ends. The AWG#24 power and ground cables in both ends are assembled with HJ-3 male pins manufactured by MAC EIGHT
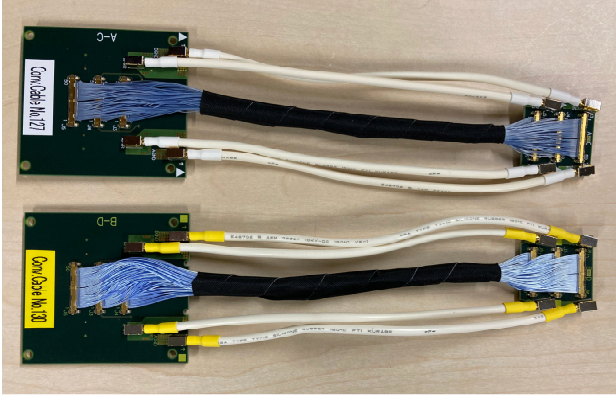
Figure 17: Conversion cable type-AC (top) type-BD (bottom). The bundles in the middle of the cable are 15 cm length μ-coax harnesses with four white jacket cables for the power and ground cables. The larger PC board is the connector for the BEX side and the smaller board is for the ROC side.

Co. Ltd.. The male pin and the receptacle connection are secured by the HH-3-R lock. The wire gauge is optimized to be AWG#24 to drop the voltage properly and to provide the FPHX chip power from the slightly higher regulator voltage output at the ROC. Details of the voltage drop is discussed in Section 4.3.

Three UX II receptacles and four HH-3-G sockets (manufactured by MAC EIGHT Co. Ltd.) are implemented on the top side of the PC board and two DF18C-100DS-0.4V(81) receptacle connectors are implemented on the bottom side of the board. The PC board is fabricated by Hayashi-REPIC Co. Ltd. and eight layered with dedicated layers for the digital and the analog-power and ground. The dimensions are 48 mm wide × 52 mm long for the BEX end to match the size of the connector end, while the ROC side is rather compact with dimensions 25 mm wide × 25 mm long. There are two types of conversion cables namely "type-AC" and "type-BC" and the difference is so the channel mapping is compatible with the channel map, which are differently designed for the columns A&C and B&D of the input ports on the ROC. There are two different lengths of harnesses for the power and ground cables, which are 15 and 25 cm, respectively.

4.3. ROC

The readout card (ROC) is a multilayered circuit board implemented outside of the TPC volume. The ROCs were refurbished after the FVTX operation in the PHENIX experiment and reused for the INTT. ROC details are described elsewhere [7]. Any aspects of ROC usage that are different from the FVTX or customized for sPHENIX are discussed below.

Twelve pairs of DF18C-100DP-0.4V(51) plug connectors and four pairs of DF18C-60DP-0.4V(51) are implemented in the ROC as input ports for a half ladder. The DF18C-60DP-0.4V(51) plug connector has 60 pins and is not used for the INTT.

Table 16
Specifications of the conversion cable. The characteristic impedance is given in differential of the LVDS pair.

Item	Specification
μ-coax make	I-PEX Inc.
μ-coax model	CABLINE-UX II [21]
Harness AWG	44
Characteristic impedance	90 Ω
Number of harness per bundle	50
Number of bundle	3
Power/ground cable AWG	24
Number of power cable	2
Number of ground cable	2
Length	15 & 25 cm

The ROC boards are originally implemented with 2.5 V regulators to provide analog and digital power for the FPHX chips with an operating voltage of 2.5 V for both analog and digital [9]. The voltage drop in the power-transfer line was minor in the FVTX owing to the short readout-cable length and low power consumption of the FPHX chip. On the contrary, as has been discussed in the previous sections, the INTT operates in the higher-power consumption mode due to its extraordinarily long readout cable chain. The FPHX operates with higher LVDS current for output data transmission than do the FVTX chips so that the signal amplitude is kept well above the receiver driver threshold.

The maximum drawing current per half ladder (26 FPHX chips) for the analog and digital power of the FPHX chips is measured to be 0.21 and 0.42 amps, respectively. Although the ROC are designed to allocate reasonably large physical cross sections or american wire gauge (AWG) for the power transmission lines, the resistances of these cables is a few hundred mΩ. The resulting voltage drop of the daisy chain of the readout cables amounts to as much as 0.2 to 0.4 V which is sizable enough for the FPHX chips to possibly malfunction due to insufficient voltage supply.

To compensate for the voltage drop, the surface mounted regulators for the FPHX power are upgraded to supply larger output voltages. The pin layouts of the upgraded regulators match the pad pattern of the ROC. Newly implemented regulators are MCP1700-2802E/TT and MCP1726-3002E/MF (Microchip Technology Inc.) with outputs of 2.8 and 3.0 V for analog and digital power, respectively. With drawing currents increased for higher voltage outputs, the supplied voltages at the FPHX location are calculated to be ≈ 2.5 to 2.6 V for both analog and digital.

5. Radiation Hardness

In the INTT readout system (see Section 4), there are a few materials for which radiation hardness is either not known or known to be not durable. In this section, the radiation hardness is evaluated for these items. Also discussed is the study of the potential radiation damage of the ROC boards during the preceding PHENIX operation.

5.1. Bus Extender

The FPC with standard polymide is widely used in radiation environments and its radiation hardness is well established. However, because LCP is a relatively new material being used for the dielectric layer of the FPC, the radiation hardness of the FPC with LCP has not been established as well as that of the polymide. The radiation hardness of the LCP material itself is proven to be as durable as polymide [23] although, the radiation hardness of the bonding sheet employed for the BEX was not known. The overall mechanical characteristics of the BEX after assembly was measured before and after a radiation exposure rather than investigating the radiation hardness of the bonding sheet itself. The primary concerns are the degradation in the flexibility of the BEX and the peel strength of the bonding sheet due to radiation damage.

A few samples of the BEX cable were exposed to ^{60}Co source for 7.2 kGy, 685 kGy, 1.45 MGy at National Institutes for Quantum Science and Technology, Japan. The expected radiation dose at the location where the BEX is installed in sPHENIX is approximately 5 kGy for five years operation[4]. The mechanical performances were evaluated by the following two tests: 1) stress test to evaluate the flexibility, and 2) peel strength test between the copper and the LCP layers [19]. As the test item 1), the Young's modulus was measured for the samples before and after the radiation exposure. Figure 18 shows the Young's modulus of these samples based on natural frequency measurements. No degradation of flexibility was observed within the accuracy of the measurements (7%) in any samples. The error was estimated by the standard deviation of multiple samples within the same radiation dose group.
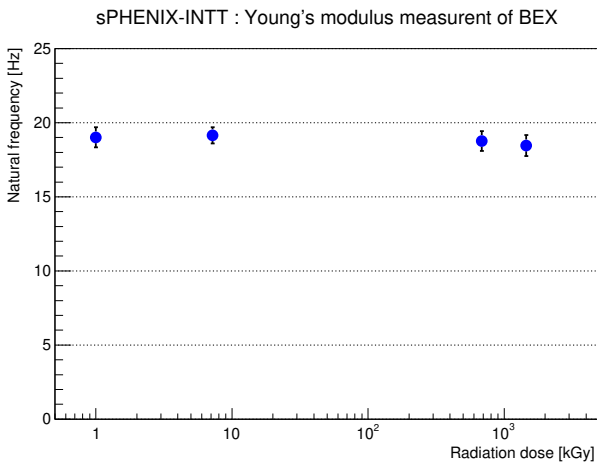

Figure 18: The Young's modulus measurement results of samples exposed to various radiation dose. The vertical axis is the natural frequency in the unit of Hz, while the horizontal axis is the radiation dose in the unit of kGy. The measurement of the sample with no radiation exposure is plotted purposely at 1 kGy.

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[4]Including an extra two years of operation beyond the officially approved three years.

For test item 2), approximately 50% and 70% degradations were observed in the peel strength for 685 kGy and 1.45 MGy samples, respectively as shown in Fig. 19. However, the measured peel strength of 18 N/cm for the 7.2 kGy sample proved to be sufficiently strong and is similar to the typical level of polymide-based FPC. Although the safety margin to keep this peel strength for possible unexpected extra radiation dose may be marginal, it is unlikely that FCCL layers would fall apart by gravity even if the peel strength were weakened by 50%. It was thus concluded that the radiation hardness of the BEX is expected to be durable for the duration of sPHENIX operation.
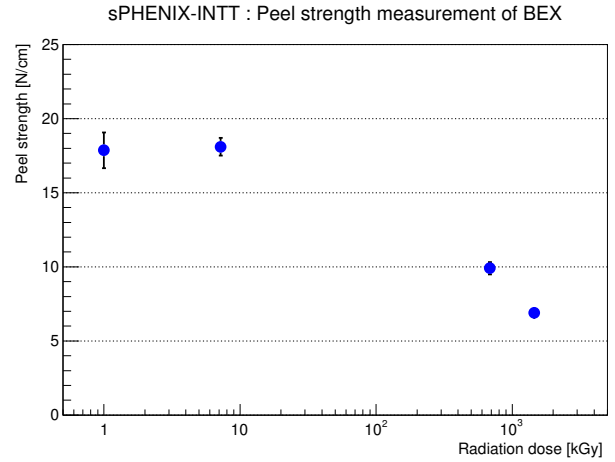

Figure 19: The peel strength measurement results of samples exposed to various radiation doses. The vertical axis is the peel strength in units of N/cm, while the horizontal axis is radiation dose in units of kGy. The measurement of the sample with no radiation exposure is plotted at 1 kGy on purpose.

5.2. Conversion Cable

The material "fluorinated resin", which is used as a dielectric insulator for the μ-coax cable [21], is reported to be weak against radiation [23] compared to popular dielectric insulator materials like polyimide or LCP. The estimated equivalent neutrons at the location of conversion cables to be installed is 0.15×10^{12} for three years of sPHENIX operation.

In order to address the radiation hardness of the μ-coax harness for three years of sPHENIX operation, the effect of radiation was studied at the RIKEN Accelerator-driven compact neutron systems facility (RANS), Japan. Three samples of harness bundle were exposed to the RANS neutron beam at energies up to 5 MeV. Each sample was exposed to 1.3, 2.6, and 4.0×10^{12} equivalent neutrons. These are factors of 9, 17, and 27, respectively, more than the estimated radiation dose for the INTT operation in sPHENIX. The signal transmission performances were compared before and after the irradiation to evaluate the radiation effect. The comparisons were made for the S-parameters, the eye diagrams, and the TDR. No degradation was observed for all samples in any of these measurements, regardless of the exposed radiation dose. Thus, it is reasonable to conclude that the radiation

hardness of the conversion cable is durable for the INTT operation as well.

5.3. ROC

The radiation dose of the ROC boards throughout five years of operation of the FVTX detector in PHENIX is estimated to have been approximately 300 Gy, while the corresponding radiation dosage for three years of the INTT operation in sPHENIX is estimated to be approximately 50 Gy. The dose for the INTT is moderate owing to the relatively farther distance of the ROC position from the collision point compared to that of the FVTX in PHENIX. Here the radiation hardness of the ROC board with respect to the total dose of 350 Gy is evaluated.

The ROC board is designed to be radiation hard and in fact it utilizes the FLASH-based ACTEL ProASIC3E FPGAs [7] which is known to be radiation hard. The optical data transmission system of the ROC board comprises the model TLK2711 (Texas Instruments) as the serializer/deserializer of data. There is a study of the radiation tolerance of the TLK2711 [24]. In this study, the increase of leakage current and the bit-error rate was monitored as a function of radiation dose. The first bit error appeared ≈280–420 Gy and the TLK2711 encountered functional failure as low as 700 Gy depending on the beam condition of the radiation exposure, e.g., high (low) intensity and short (long) duration. While the leakage current stays the same up to 400 Gy, a rather rapid increase of current was observed beyond that point.

According to the above study, the condition of the TLK2711 are already in the range that some bit error symptom may start after the FVTX use. Altough it was preferable to replace them all before the reuse for the INTT, the model was discontinued. Unfortunately, insufficient quantities were available in the market place to replace them all. Hence, the replacement candidates are prioritized and limited to only those which already have bit-error symptoms. The only ROCs installed are those which passed the various function tests including no bit-error symptoms.

6. Summary

A new silicon-strip detector was developed for the sPHENIX experiment at RHIC. The silicon ladder consisted of silicon-strip sensors, FPHX chips, HDIs, and a high thermally conductive carbon-fiber stave. The ladder was designed to be as thin as $X/X_0 = 1.19\%$. The bus extender and the conversion cables were developed to transmit signals from the ladder to the ROC board. The 1.11 m long bus extender cable employs the novel low attenuation LCP as the dielectric material of the FPC. The conversion cable employs μ-coaxial harnesses to secure flexibility in three dimensions in order to connect the bus extender end to the input/output ports of the ROC board without introducing any stress at the connection.

The result of the study indicated that both the bus extender and the conversion cables are sufficiently radiation hard against estimated radiation dose for three years of the INTT operation in the sPHENIX experiment. In contrast, the exposed dose for TLK2711 chips of the ROC board throughout five years of the FVTX operation in the PHENIX experiment caused some bit errors to start to appear. Any chips showing these symptoms were replaced with new chips. The ROCs are installed relatively far away from the collision point for INTT operation in sPHENIX as opposed to FVTX in PHENIX. Thus, the radiation dose for the ROC boards in three years of INTT operation in sPHENIX is estimated to be relatively moderate, i.e. 1/6 of that of the FVTX in PHENIX.

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