News

- Tim Camarda is leaving the Group
  - this creates problems for our Power Board prototype, for BTOF power board discussions, for EICROC0 BNL testing and for general power distribution topics in EPIC
  - he will remain at BNL and is available for (very) light support in the short term only
- "AC-LGAD Readout" PED to Fernando.
  - Responded on 10-Mar
    - *I shared your proposal, which I support, with Elke and Rolf for their feedback. I expect to have some feedback soon.*
  - Responded on 11-Mar
    - *We have concurrence from Rolf to proceed but with modifications as the availability of funds is uncertain at this time.*
    - *we need to split the funding/effort into two parts: now (FY25) and after Oct 1st (FY26)*
      - proponents need to meet to decide how to do it
- Electronics@DAQ Meeting last week, from Christophe regarding ASICs
  - *EICROC0/A ready (B in progress)*
  - *EICROC1/1A*
    - *– 1A (4x32) : ready*
    - *– 1 (32x32) : issues to be fixed* ⇐ *we'd like to use this for our electronics prototyping with full sensor*
  - *EICROCs ~55% or reticle area*
  - *CALOROC1A/B complete (see talk by Frédéric Dulucq)* ⇐ *we might want to use this for our electronics backend prototyping*
    - *– In verification*
  - *Other (non EIC) chips ready*
  - *Submission delayed till EICROC1 fixed*
    - Expectation is end of March (said Christophe)

Ongoing Efforts

- Power Board
  - Tim is leaving but the PB sub-project is in an advanced shape so we are trying to see if our v1 can be completed at BNL under Steve Boose (another engineer, at 25% of his time) with Tim's limited guidance ⇒ "Project" agreed but TBD ⇒ more discussions needed
- EICROC0 testing (@BNL)
  - stalled, waiting for people (NOTE: RHIC is just starting up its physics run which will likely cause further delays)
  - this needs more discussion (Prithwish, Prashanth, TL, other?)
- lpGBT interfacing (Zhengwei@LBNL)
  - moving on… will discuss this next Monday (also with Zhenyu & TL)
- "FELIX-lite" (or "DAM-lite")
  - decided to use the Alinx AXAU15 PCIe card as a "FELIX-lite" candidate
    - people from the "Electronics & DAQ Group" seem to also agree
  - **NEW:** an effort is underway (JLab) to design & produce a FMC daughtercard under William Gu's (JLab) guidance:
    - 4 fibers going to RDOs
    - 1 data fiber going to the future GTU (so-called "Fast Command" stuff)
    - 1 clock dedicated fiber going to the future GTU (for a pristine clock!)
    - **this would give us full FELIX functionality in a small & cheap board for testing ideas as well as lab readout of various detectors**
  - Working on the PCIe interface FW (TL) to be able to stream data into a DAQ PC
    - will do a (simple) emulation of the lpGBT+ASIC in the AXAU15 card to look at various issues arising due to the streaming nature ⇒ interest from the DAQ Group
    - I hope we can integrate Zhengwei's lpGBT FW later on…
  - We are aiming at the full *streaming* readout chain: ASICs⇔lpGBT⇔DAM(w GTU iface)⇔DAQ PC⇔data/configuration files & GUIs

More ongoing efforts

- BTOF SH and Power Board
  - we started on this: we should get it into some pre-preliminary shape (at least an educated guess for dimensions and power!) and send it off to Sushrut to start the iterative cycle to figure out where to place and how to cool the SH
    - Wei, Mike, Zhenyu, TL…
- FTOF ASIC Module and ASIC package
  - Mathieu expressed a worry that direct connector-to-connector links between the ASIC package and the RB might apply too much pressure on the ASIC package
  - we wanted to take a more detailed look on how this is done for CMS ETL (?)
  - any new items to discuss here?

Comments?