ePIC Silicon Vertex Tracker R&D

eRD104: Services Reduction
eRD111: Modules, Mechanics, Cooling and Integration
eRD113: Sensor Development and Characterization

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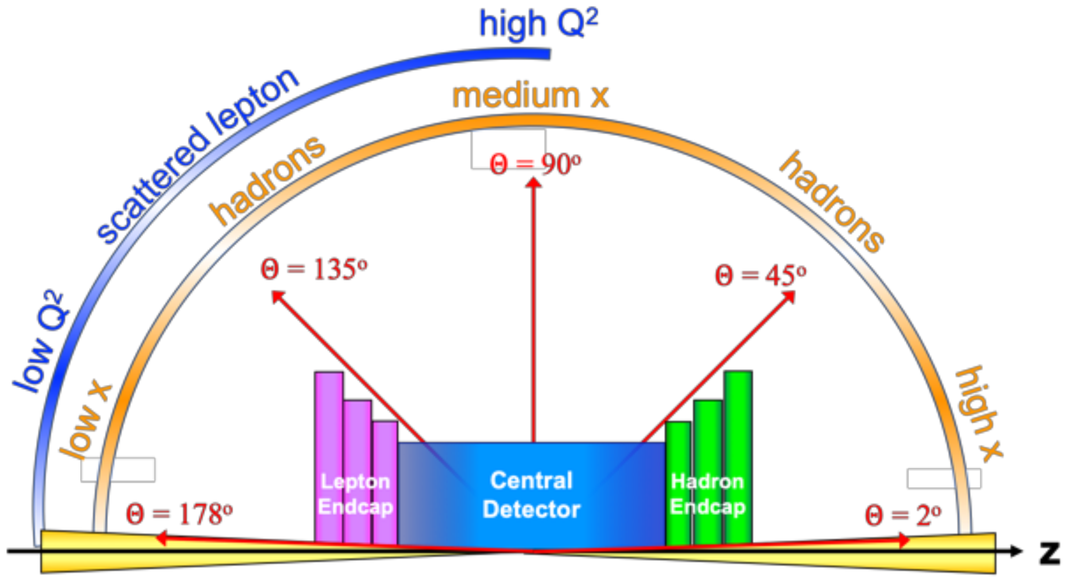
ePIC / EIC Project R&D Day, 16 – 17 April 2025
https://indico.bnl.gov/event/27200/

Outline

- Introduction
- Sensor Development and Characterization
- Services Reduction
- Modules, Mechanics, Cooling and Integration
- Remaining R&D Milestones

ePIC Tracking Resolution Requirements



	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	~0.10%×p⊕2.0%	~ 30/p_T μm ⊕ 40 μm
Backward (-2.5 to -1.0)	~ 0.05%×p⊕1.0%	~ 30/p_T μm ⊕ 20 μm
Barrel (-1.0 to 1.0)	~0.05%×p⊕0.5%	~ 20/p_T μm ⊕ 5 μm
Forward (1.0 to 2.5)	~0.05%×p⊕1.0%	~ 30/p_T μm ⊕ 20 μm
Forward (2.5 to 3.5)	~0.10%×p⊕2.0%	~ 30/p_T μm ⊕ 40 μm

ePIC SVT Detector Subsystem Collaboration

- The overarching goal is the development and construction of a well-integrated full tracking and vertexing detector subsystem for the ePIC project detector based on 65nm MAPS sensors

- This talk presents R&D updates with respect to last year's meeting — https://indico.bnl.gov/event/22388/

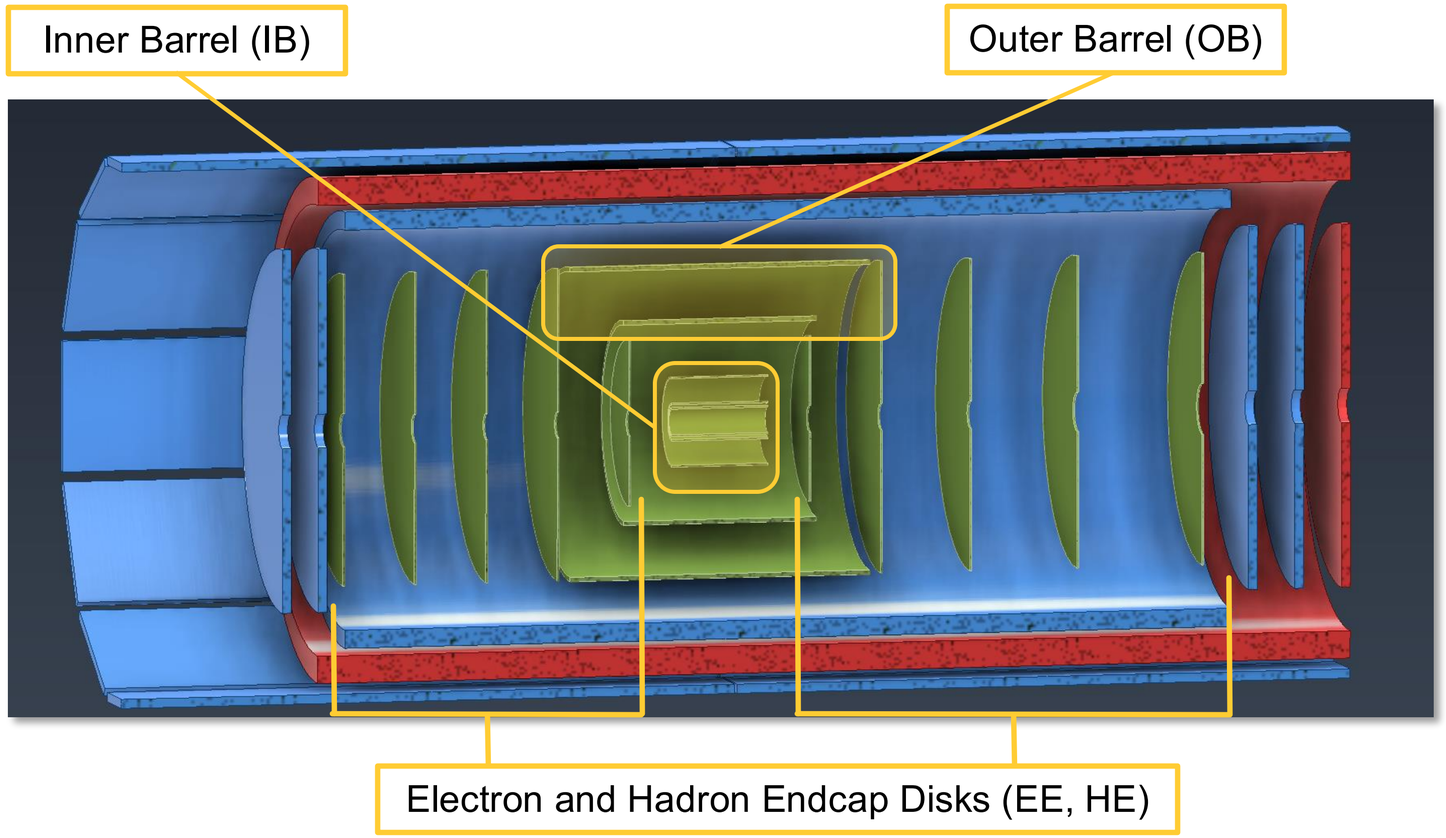
- The SVT workfest at the January 2025 collaboration meeting provides a good overview of the many ongoing R&D activities — https://agenda.infn.it/event/43344/

SVT Concept

- **Inner Barrel (IB)**
  - Three layers, L0, L1, L2
  - Radii of 36, 41, 120 mm
  - Length of 27 cm
  - X/X_0 ~ 0.05% per layer
  - Curved, thinned, wafer-scale sensor
  - Approx. 20μm pixel pitch

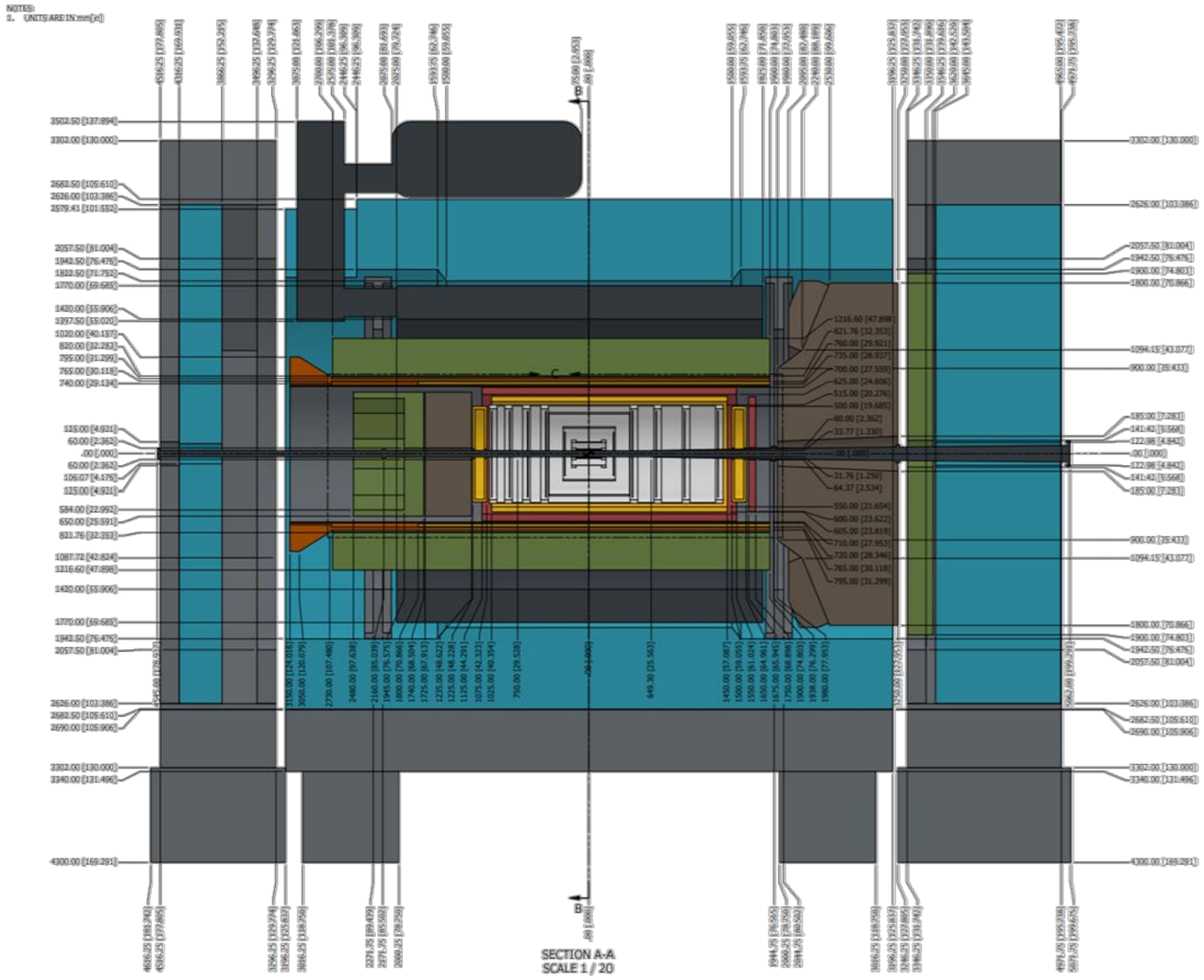
- **Outer Barrel (OB)**
  - Two layers, L3, L4
  - Radii of 27 and 42 cm
  - X/X_0 ~0.25% and ~0.55%
  - More conventional structure w. staves
  - Sensor derived from IB sensor

- **Electron/Hadron Endcaps (EE, HE)**
  - Two arrays with five disks
  - X/X_0 ~0.25% per disk
  - More conventional structure
  - Sensor derived from IB sensor; common with OB



- **Lengths for L2 – L4 increase so as to project back to z = 0; disk radii adjust accordingly**

SVT outer dimensions and integration in ePIC



Spatial extent along the beam axis:

$-106.25 < z_{SVT} < 136.25$ cm

Radially:

$r_{out} < 43.00$ cm

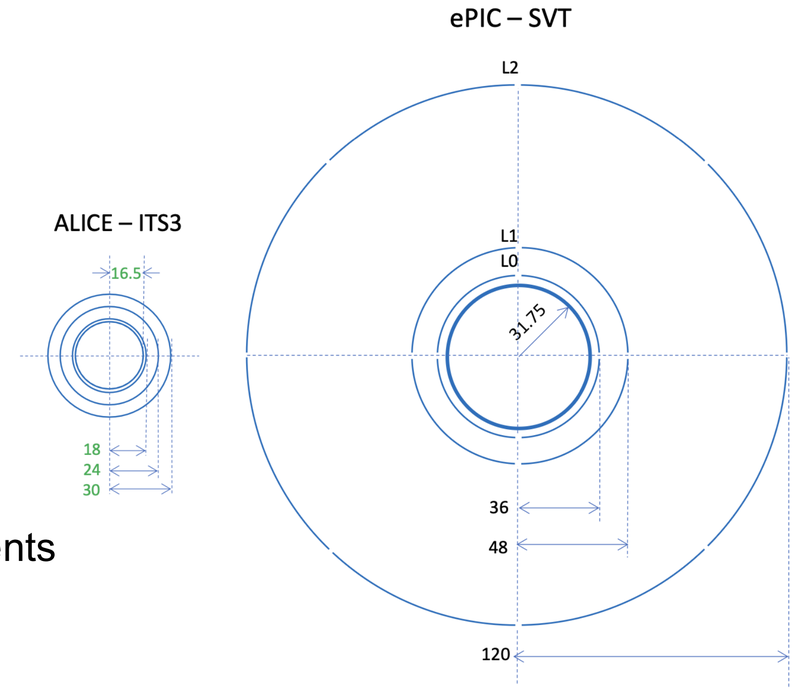
$r_{in}(z)$ determined by beam-pipe + 5mm

Beam-pipe bake-out with SVT installed; clamshell of detector halves

See Rolf Ent's discussion of envelopes at the March 20, 2025 ePIC general meeting, https://indico.bnl.gov/event/25908/

ePIC SVT R&D

At a high level, the ePIC SVT thus requires us to develop:



1. ITS3-like Inner-Barrel layers

- Re-use the **ITS3 sensor** as is
- Adapt the ITS3 detector concept to the EIC:
  - Mechanics of bent layers — sensor and support — for the larger EIC radii
  - Services and cooling design and routing for the EIC acceptance requirements
  - Considerations related to in-situ beam-pipe bake-out at the EIC

2. EIC variant for the staves in the Outer Barrel and the Endcap Disks

- **EIC Large Area Sensor (LAS)**, i.e. ITS3 sensor optimized for large-area coverage, yield, and cost
  - EIC LAS will be stitched, but not to wafer scale; functionality and interfaces stay largely unchanged
  - Size(s) of the EIC LAS defined by requirements for full coverage and yields, cost; currently 5 and/or 6 RSUs
  - Approximately 4,000 EIC-LAS sensors will be used in the OB and Disks,
- More conventional carbon composite mechanical support structures with integrated cooling
- Lightweight electrical interfaces with **Ancillary ASIC** and aluminum flexible printed circuit technology

SVT R&D

R&D for the ePIC SVT historically organized in three Project R&D areas: eRD104, eRD111, eRD113

- **eRD104** — services reduction
  - Investigates methods to significantly reduce the services load;
  - Powering system
  - Readout system
- **eRD111** — modules, mechanics, cooling, and integration
  - Development of a full tracking detector solution composed of next-generation 65 nm MAPS;
  - Forming modules from stitched sensors
  - Barrel and Disks
  - Cooling
  - Mechanics and integration
- **eRD113** — sensor development and characterization (started in FY23)
  - Development of the EIC MAPS;
  - Sensor design
  - Sensor Characterization

Most activities now transitioned to Project Engineering and Design (PED) support

In addition, the SVT relies on significant in-kind contributions

Sensor Development and Characterization

ITS3 Wafer Scale Sensor — Development Path

- **MLR1** - Submitted Q4 2020
  - **Technology exploration** and prototype circuit blocks for future sensors
  - Large number of test structures; including Analogue and Digital Pixel Test Structures (APTS, DPTS)

- **ER1** - Submitted Q4 2022
  - Exploratory designs (MOSS, MOST sensors) for **proof of stitching principles**, learning methodology and yield
  - Also, small prototypes and test chips

- **ER2** – Design almost completed, submission by mid-2025
  - **MOSAIX** sensor aims to satisfy ITS3 requirements
  - Not an evolution of MOSS/MOST; substantial redesign of existing circuits, with new features

- **ER3** – Production version
  - Minimal modifications to MOSAIX

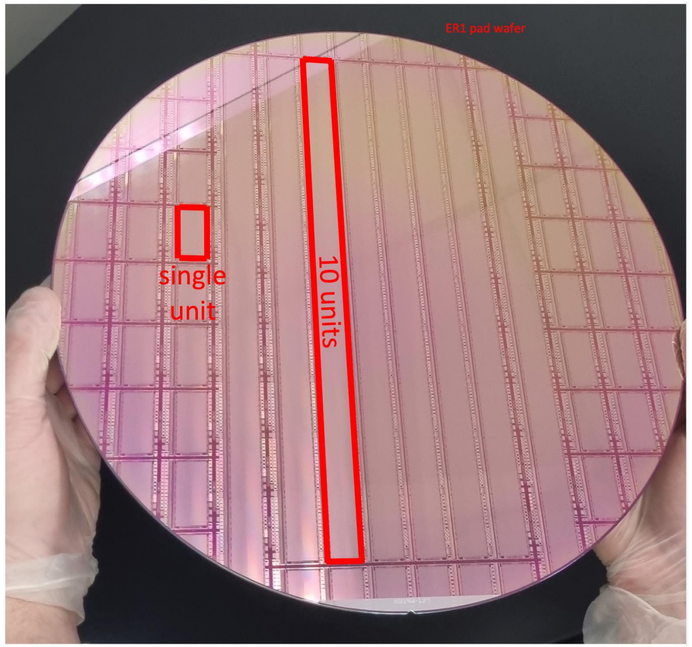
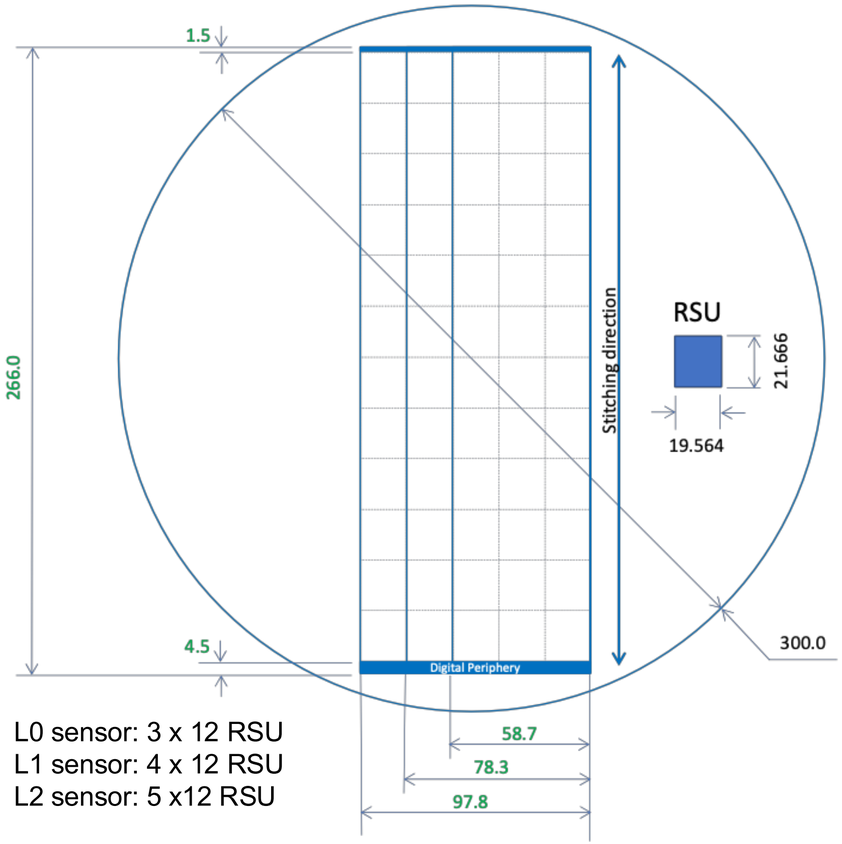


Figure credit: Gianluca Aglieri Rinella, Walter Snoeys — https://indico.cern.ch/event/1280150/

MOSAIX sensor

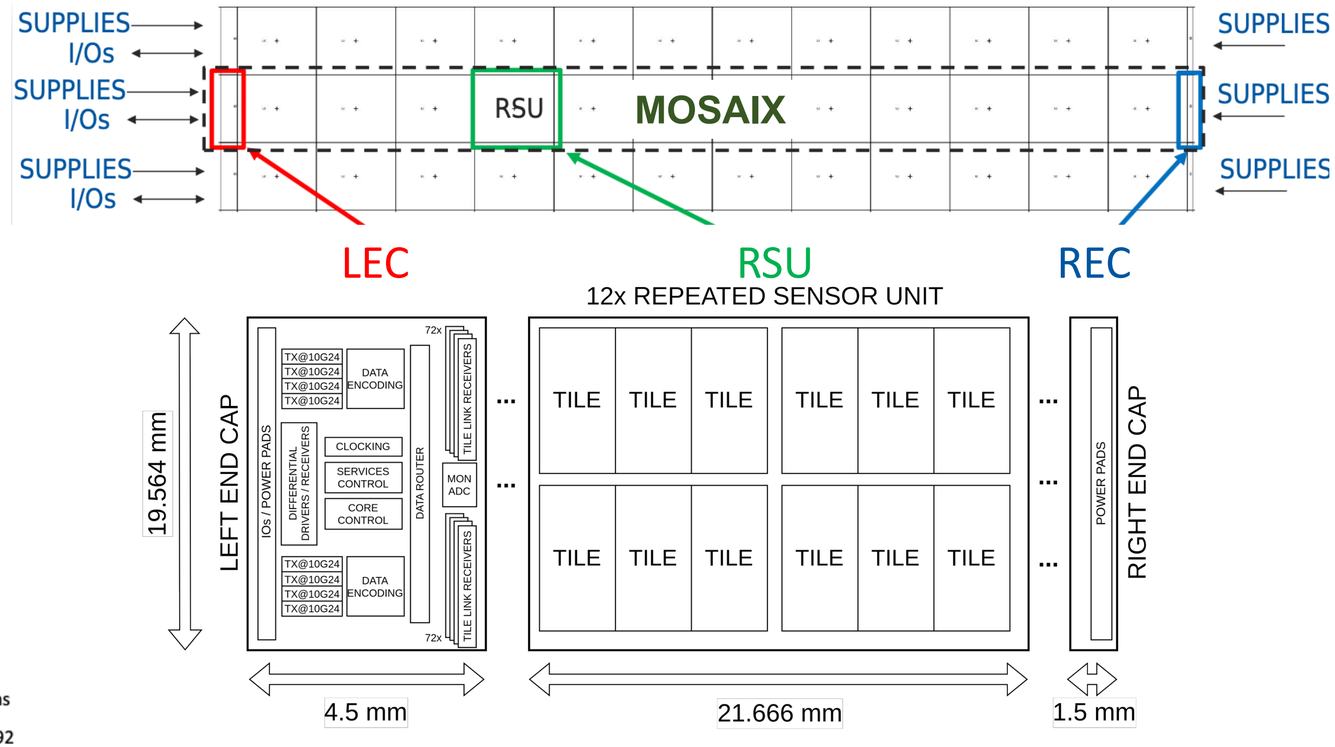
- Full feature prototype of the sensor for ALICE ITS3, to be used in the SVT IB
- Wafer scale sensor design using stitching technique in the TPSCo 65 nm CMOS Imaging Sensors process (customized)
- The design is largely completed and undergoing verification in preparation for submission



L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU

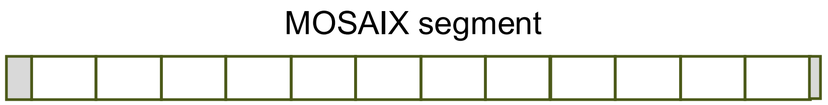
ER2 sensor widths

19.564 x 3 = 58.692
19.564 x 4 = 78.256
19.564 x 5 = 97.820



MOSAIX to EIC-LAS

Inner Barrel



- 12 RSUs
- 8 data links
- 7 slow control links
- Direct powering

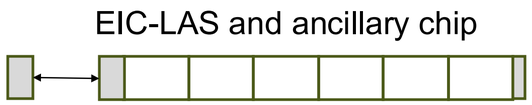
Improve yield and coverage

Lower material budget

Lower material budget, fit integration requirements

Lower material budget, fit integration requirements

Outer Barrel, E/H Endcaps



- **5 or 6 RSUs**
- **Single data link**

EIC-LAS

- Multiplex slow control
- Serial powering

Ancillary ASIC

Ancillary ASIC

The Ancillary ASIC is designed to enable lightweight power distribution and signal transmission to the SVT the OB, EE, HE

Being developed in a 110 nm SOI technology

- No modification of MOSAIX needed
- 4 MPW runs per year, fast and cost-effective prototyping

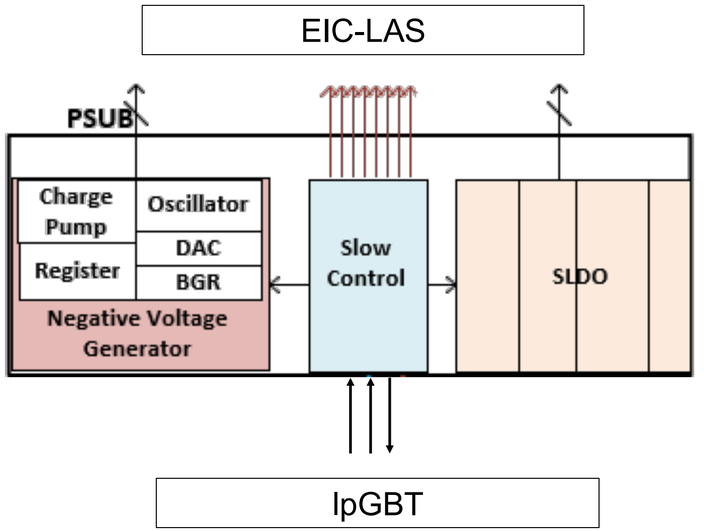
Power

- **Shunt-LDO** (SLDO) regulators for serial powering
- **Negative Voltage Generator** (NVG) to deplete the sensor

Dedicated **Slow Control** (SC) interface between EIC-LAS and lpGBT

- Lowers material budget
- Enables integration within the available FELIX channels

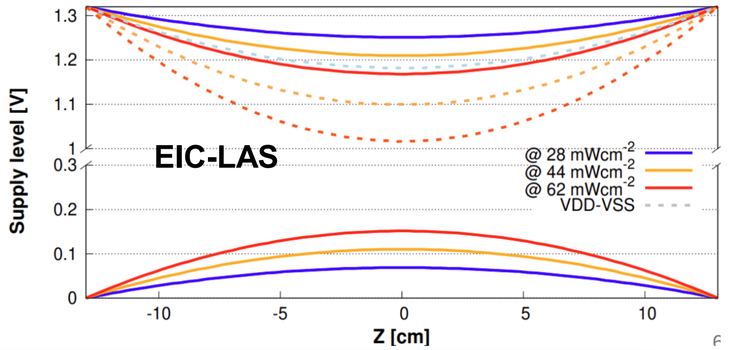
Ancillary ASIC
High level block diagram

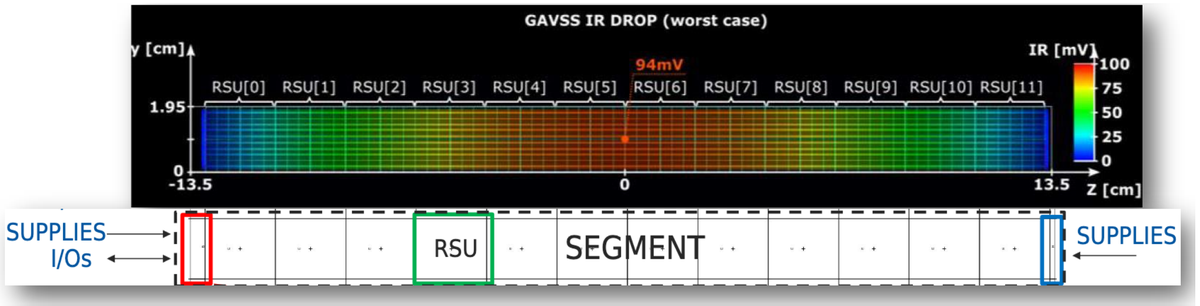


Work on EIC LAS

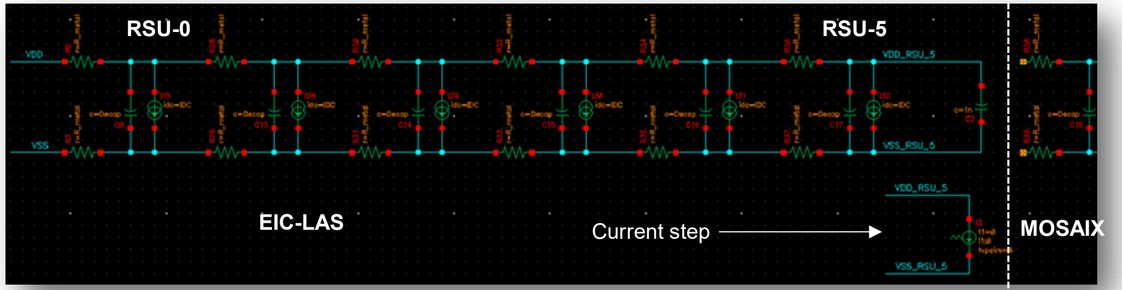
Reducing from 12 to 5 – 6 RSUs

- MOSAIX powered from LEC and REC to compensate for IR drops along the length of the sensor
- Ongoing **simulations to understand IR drop in EIC-LAS** (@ 5/6 RSU)





Simple model including supply resistivity, constant DC current, and local decaps.

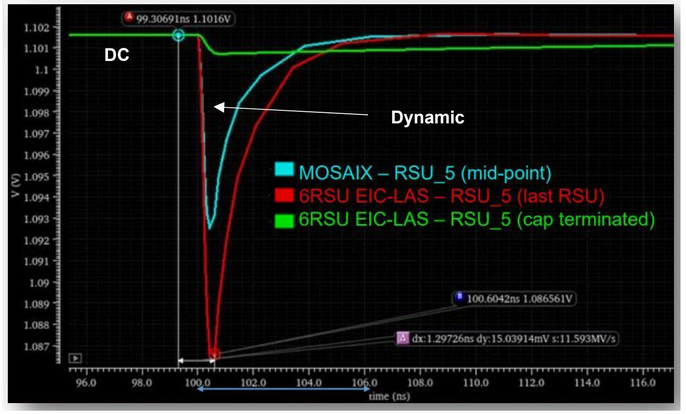


Clock propagation delay of about 2ns (in each RSU)

- Local supply drop/noise are expected to be worse in the EIC-LAS in case of dynamic activity

- Possible improvements:
  - REC internal decaps - limited area in REC for modification
  - REC external decaps – option under discussion
  - Power also from the REC – not really considered

VDD-VSS Local drops @ RSU-5 after a current step



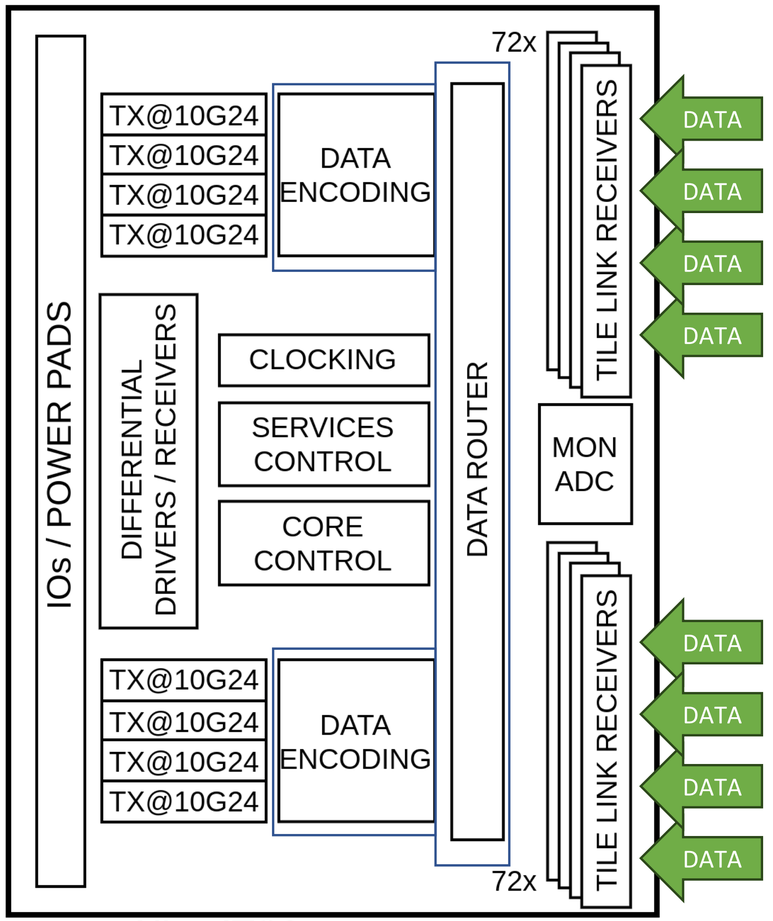
Modifications require access to the design database.

Work on EIC LAS

LEC modifications

- MOSAIX LEC
  - 144 data links @160Mbps from RSU tiles
  - Data Router to reroute data from the 144 tile links to different serializers
  - 8 high speed serializers
  - Data Encoding logic ported from the lpGBT chip to drive the electro-optical transceivers (i.e. VTRX+)

- **EIC-LAS LEC: single high speed serializer**
  - Bypass Serializer LDO
    - Study on the performance before and after removing LDOs
    - Dedicated decap cells, star routing (supply), and functional adjustments (no LDO controls)
  - Data Encoding and Router
    - Serialization of the data to a single channel
    - Challenge to adapt/change
    - Slow control needs to be modified



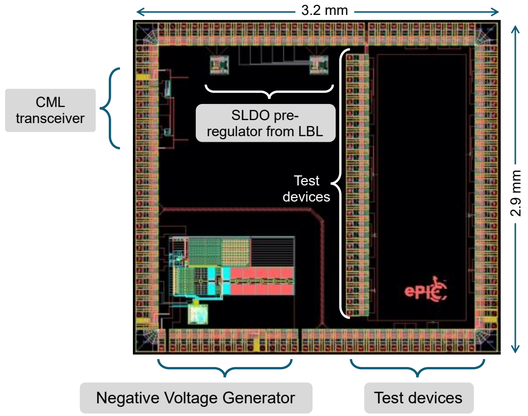
Alice/ITS3 (Gianluca's slides)

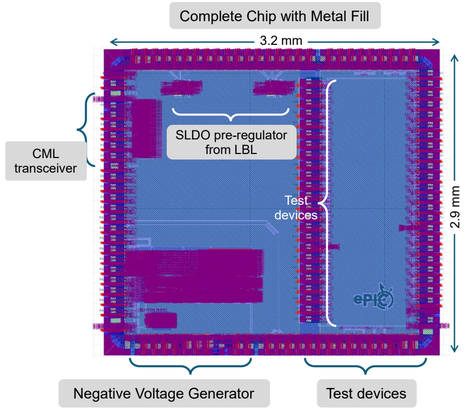
Modifications require access to the design database.

AncASIC prototype submissions

AncASICXT011_P1

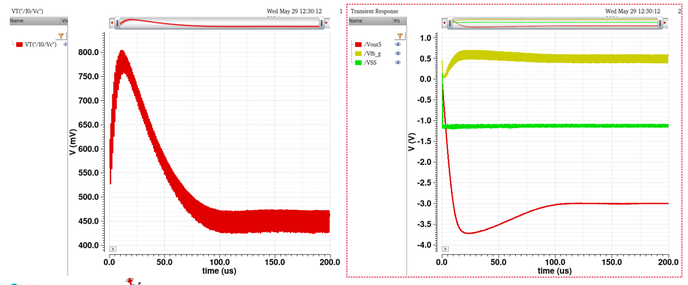
- NVG first prototype
- SLDO pre-regulator stages
- Transistor test structures for radiation hardness study
- TX/RX stages for DC-coupling demonstration





Simulation of the closed-loop regulator

- Drive strength = 2, V_{REF} = 3 x (3/20) V = 0.45 V, should produce -3V, R_L = 25 kΩ



Brookhaven National Laboratory ePIC

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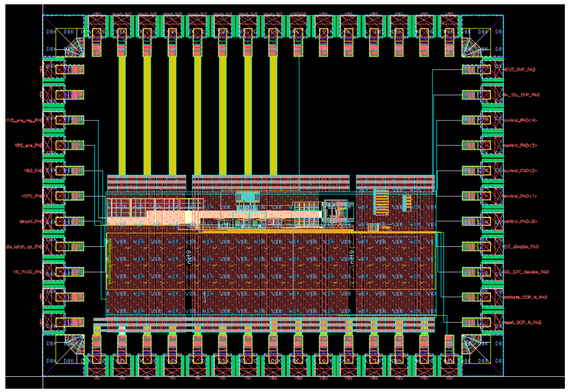
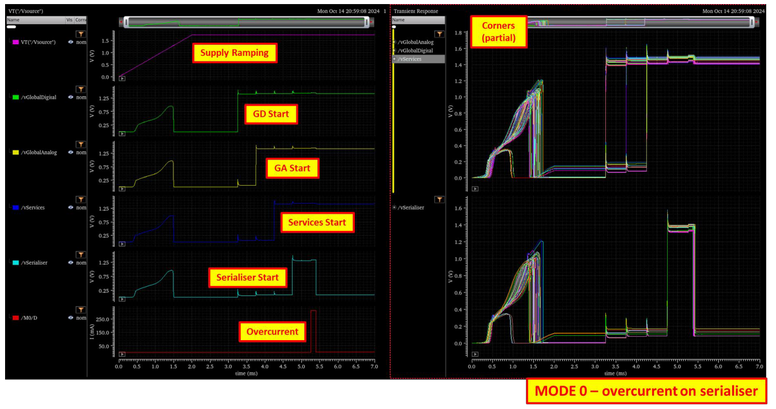
MPW2_SLDO

- Complete SLDO regulator
  - Including pre-regulator, bangap, overcurrent protection
- Independent UK submission, no Design Sharing Agreement (yet)



Start-up and Overcurrent Protection simulation



- Design reviews organised for each block by SVT designers with external expert(s)
- **Both taped out in March, expeted out of fab in September**

AncASIC ongoing work and next steps

AncBrain

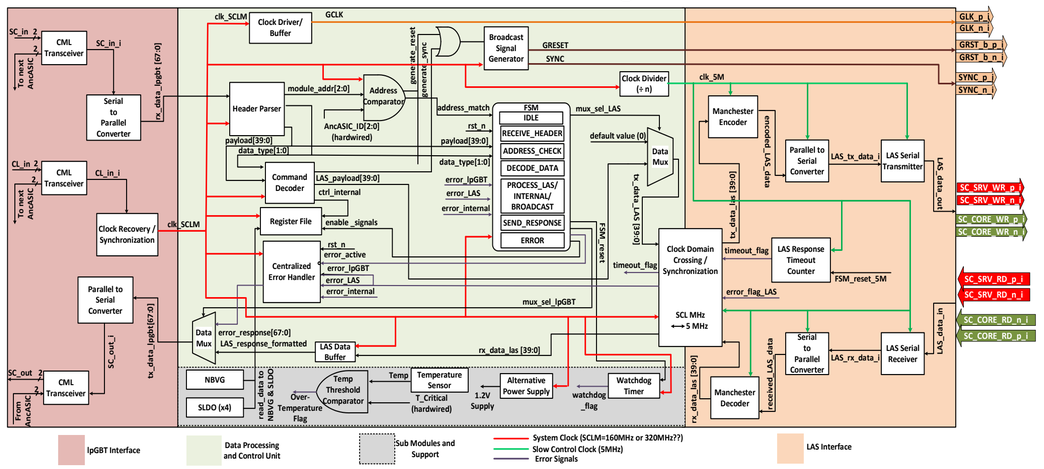
- Functionality
  - SC interface between lpGBT and EIC-LAS
  - Internal Sub-Module (SLDO, NVBG) Control

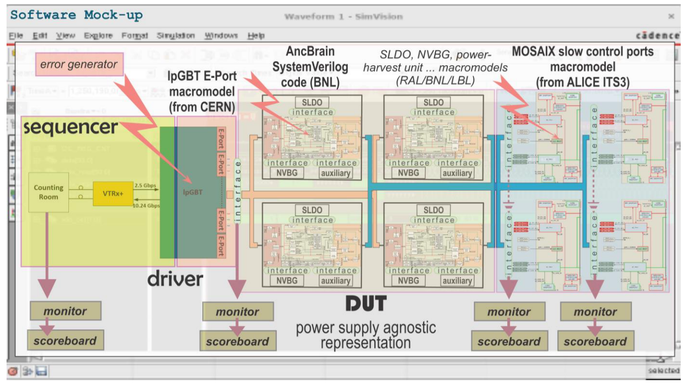
- Ongoing work
  - Specs capture well advanced
  - Design and simulations ongoing
  - SW and HW mockups in development for verification, including full chain from counting room to groups of AncASIC/EIC-LAS

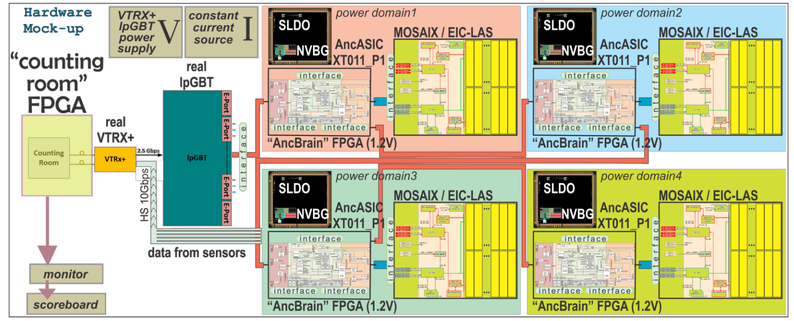
Next steps

- Two more MPW submissions planned before production: AncBrain, complete AncASIC
- Next foundry runs (2025): May, September, November

AncBrain block diagram







Characterization and production testing

- Covers ITS3 sensors, EIC-LAS and AncASIC, including test setups development

- Characterisation of prototypes
  - Tests – characterization, thermal, irradiation – in labs and test beams
  - Development of wafer probing capability for production
  - Irradiations at SVT facilities

- Production testing (i.e. Quality Control)
  - Probing of all ER3, EIC-LAS production, AncASIC production wafers

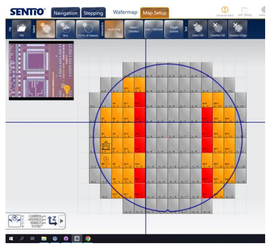
- Ongoing work
  - Preparations of MOSAIX wafer probing
  - Preparation of AncASIC prototypes testing
  - ER1 testing

MOSAIX wafer probing development

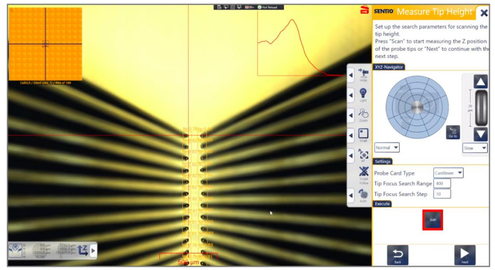
- Wafer probing development for MOSAIX ongoing at CERN with significant SVT contribution
- Goal: automated high speed wafer probing with vertical probe card

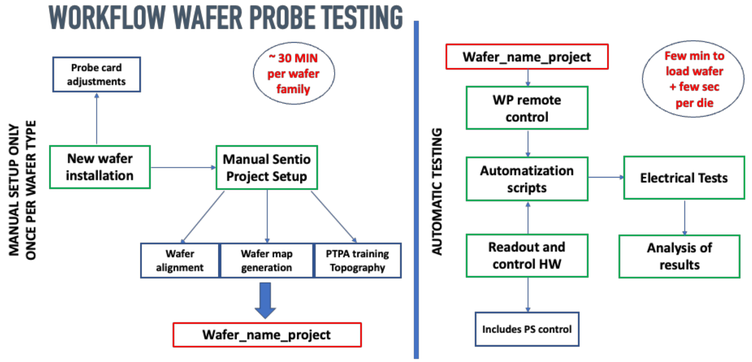
- Commissioning and first tests in **non-automated mode**
- Development of **automatization SW** tools

Wafer map generation



Probe To Pad Alignment training

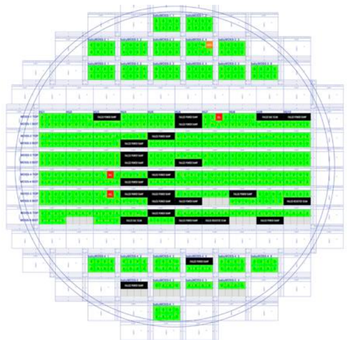




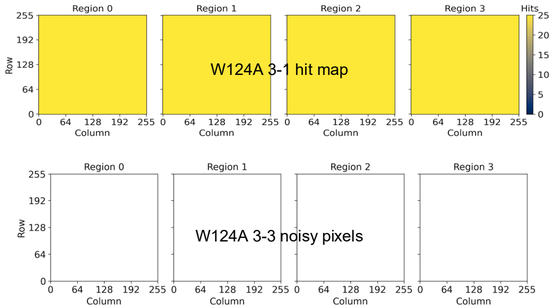
- **Automated probing** of an ER1 wafer with **cantilever probe card**, ER1 DAQ and analysis tools

Tested all 25 babyMOSS top unit in the wafer in 25 minutes with comparable results to ALICE

ITS3 results



SVT results

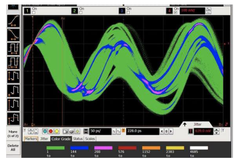


- Tests of NKF7 transmitter chip with **vertical probe card**

10 GBPS FIXED PATTERN WITH DIFFERENT VOLTAGE ACTIVE PROBE

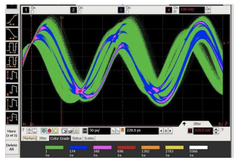
- Fixed pattern set to: 4h'5555

@1.2V



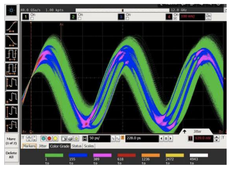
- > 600 mV amplitude
- Eye width of > 50 ps

@1.3V



- > 650 mV amplitude
- Eye width of > 80 ps

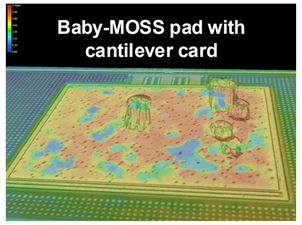
@1.4

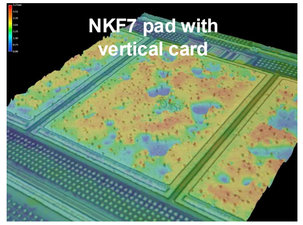


- > 700 mV amplitude
- Eye width of > 80 ps

The results obtained are relatively similar to the results of testing by chip designers

Ongoing study of the penetration of the needles as function of the applied force to optimise electrical contact between needle and pad (Optical Microscopy)



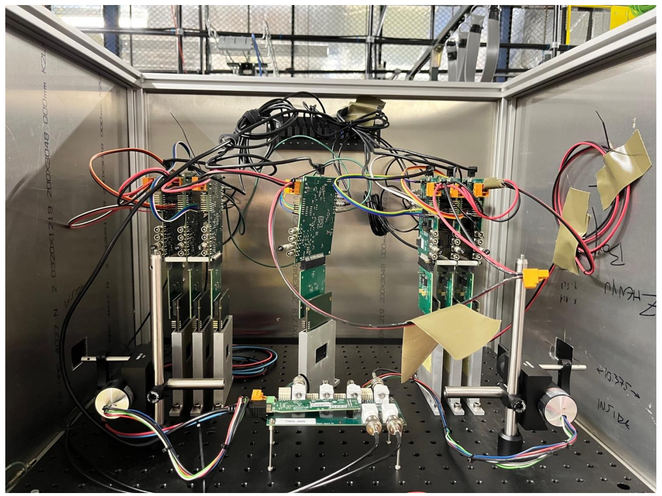


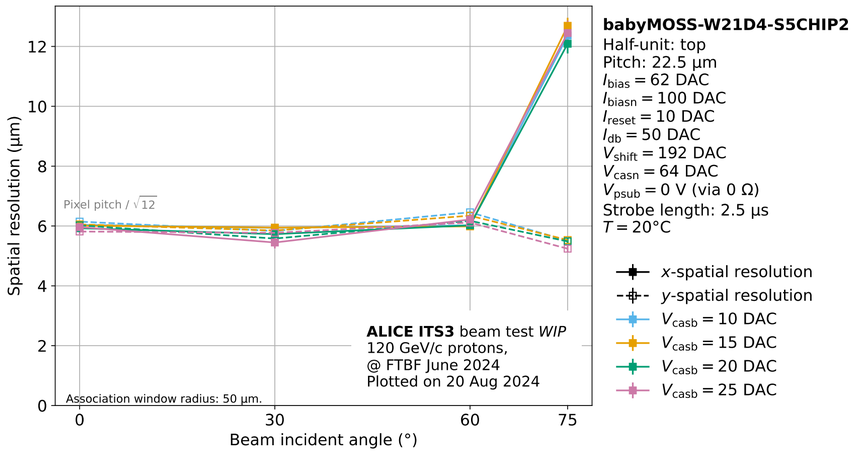
ER1 beam and irradiation tests

- Single RSU ER1 sensor, a.k.a. “babyMOSS”, tests in climate chamber, beams at FNAL and JLab; irradiation campaigns at LBNL and UC Davis

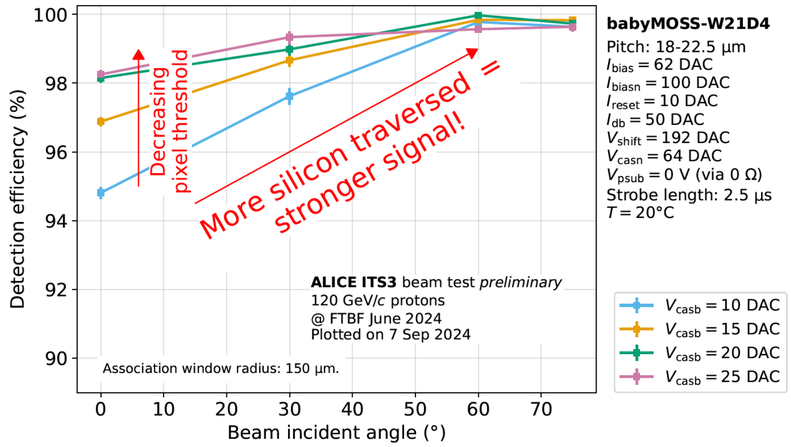
- Goals: quantify point resolution and its angular dependence, fake hit rate and signal efficiency in dependence of temperature and irradiation, handling and assembly tests

Test beam at FNAL - 120 GeV pions- ER1 telescope





Spatial resolution at large angle dominated by multiple scattering in the sensor holding frame



Services Reduction

Services Reduction

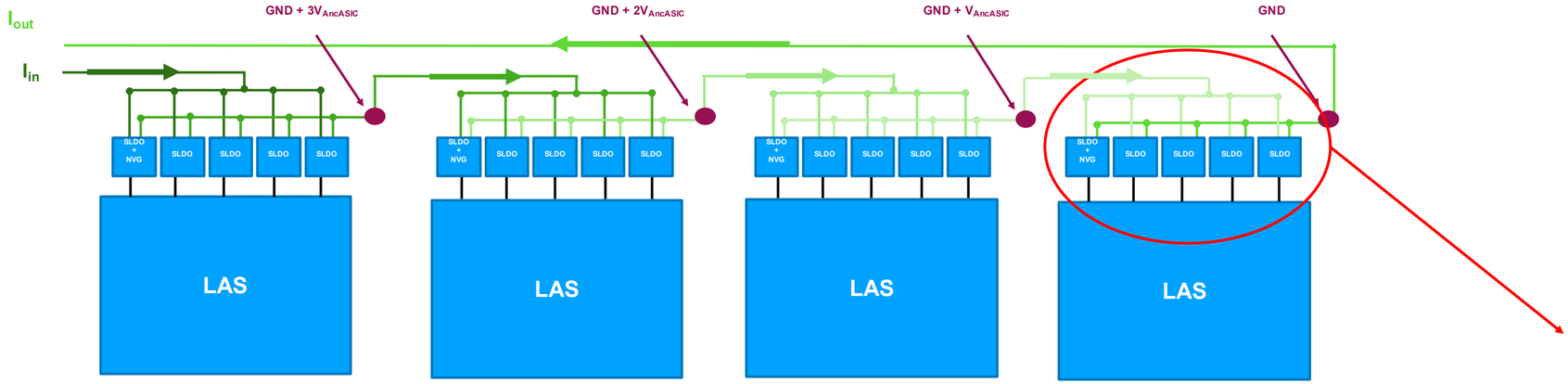
- Services are strongly coupled with sensor
- Traditionally powering forms the leading contribution to the service load; readout and slow-control are key as well

- Reduction of material associated to the services is needed for OB, HE, EE
- Approx. 8m^2 of surface; 4000 EIC-LAS sensors; main impact on service load and integration constraints

- Serial powering, sensor bias voltage generation, and multiplexed slow-control incorporated into the AncASIC
- Readout and powering schemes between sensors and control room designed around powering and slow control features, integration constraints

OB, HE, EE powering

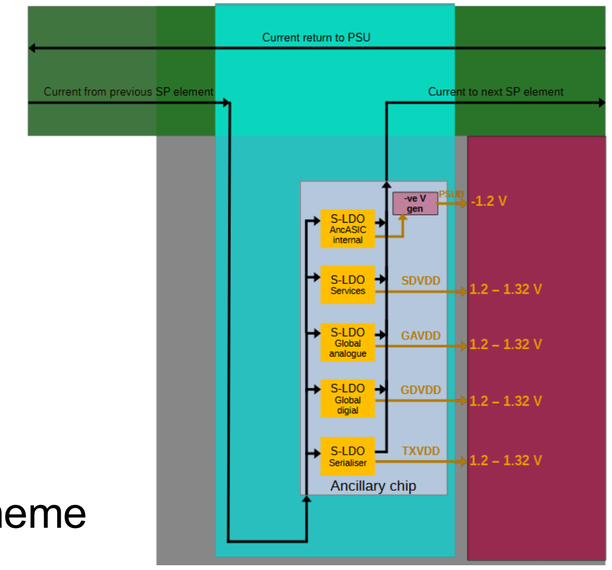
- Powering and readout **organized by groups of up to 4 EIC-LAS**



- **Serial powering**: current flowing between AncASICs on FPC
  - One pair of lines (I_{in}, I_{out}) per group carrying current for one AncASIC/EIC-LAS module

- S-LDO regulators in each EIC-LAS to generate stable voltages for
  - Electronics power domains (services, global analogue, global digital, serializers)
  - Voltage for internal AncASIC modules (e.g. NVG for sensor bias voltage)

- AncASIC/EIC-LAS modules in the SP are on different grounds
  - Needs to be accounted for in data and slow control links, and overall SVT grounding scheme

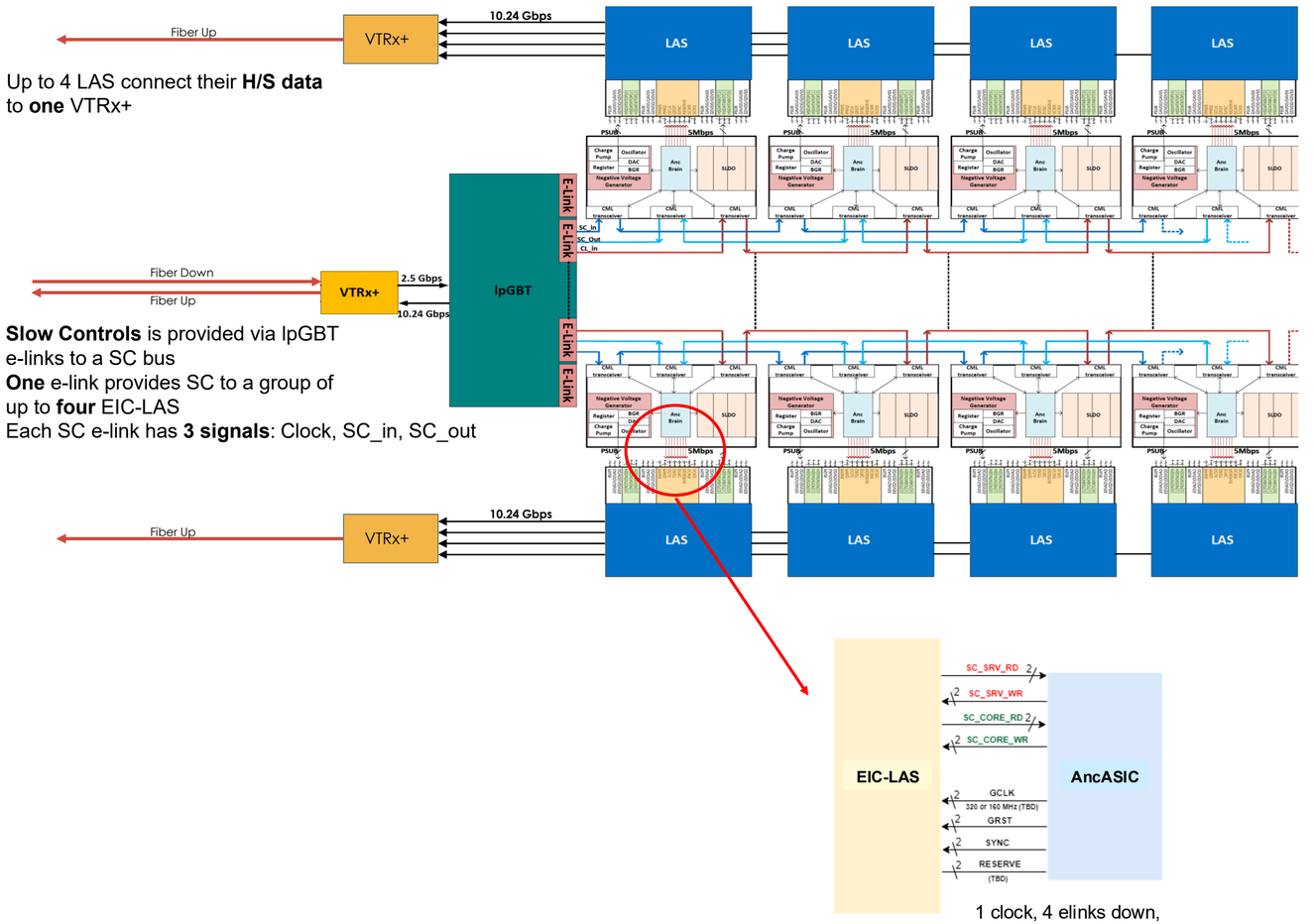


OB, HE, EE readout scheme

- Powering and readout **organized by groups of up to 4 EIC-LAS**

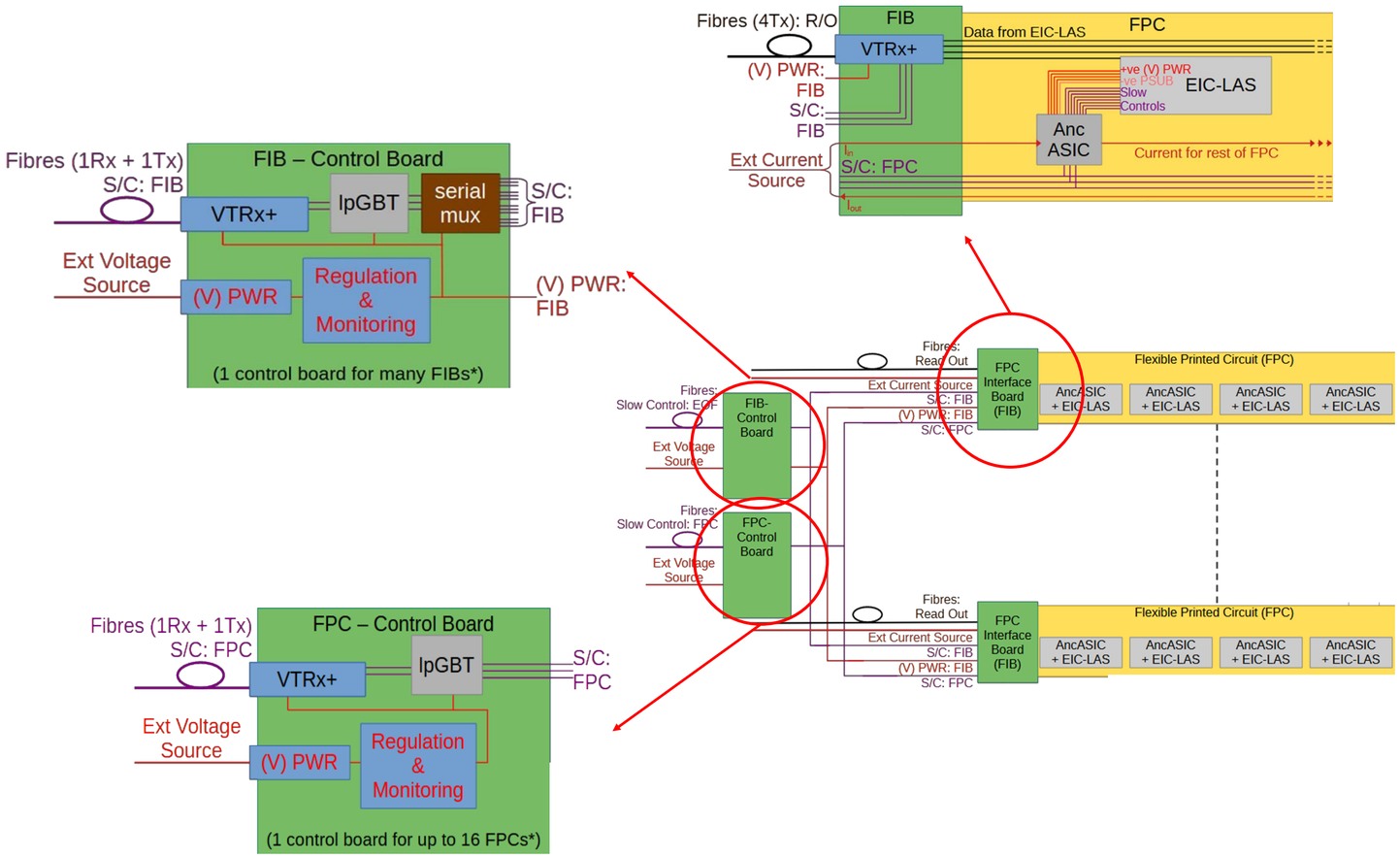
- 1 readout (**data**) link/EIC-LAS
  - AC-coupled directly to the VTRX+; then fibers to FELIX through aggregator board

- 3 **slow control** lines per group
  - Slow control signals provided to AncASIC through lpGBT elinks to a SC bus on the FPC
  - One SC elink has 3 signals: clock, SC_in, SC_out
  - AncBrain translates incoming SC protocol to EIC-LAS slow control interface (same as MOSAIX)
  - Two configurations under discussion for the SC bus: AC-coupled, multidrop (see backup); DC-coupled daisy-chained (shown in the figure)



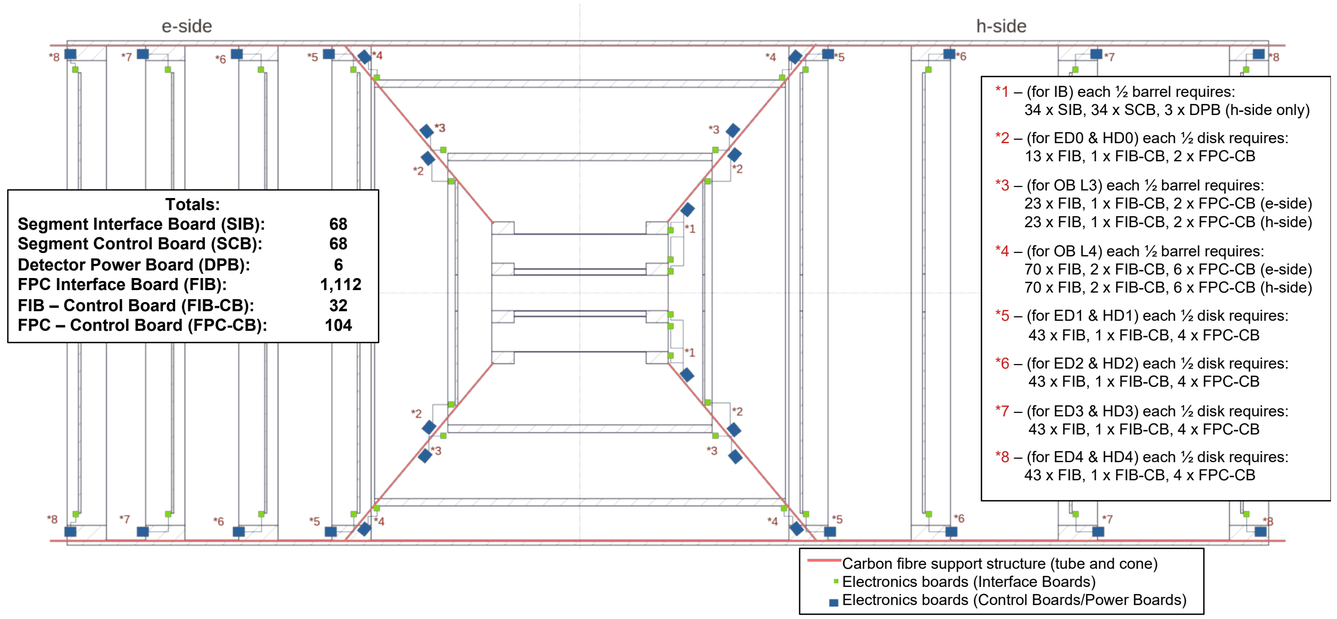
Readout boards

- **FPC Interface Board - FIB**
  - Routing of SP current and slow control signals to FPC
  - AC-coupled data links to VRTX+, electro-optical conversion, connection to fibers
- **FIB Control Board - FIB CB**
  - Provides control signals and power for the VTRX+ on the FIB card
- **FPC Control Board – FPC CB**
  - Provides slow control signals for the AncASIC/EIC-LAS modules on the FPC via the FIB

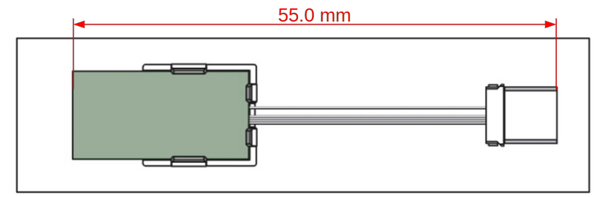


Readout boards: number and size

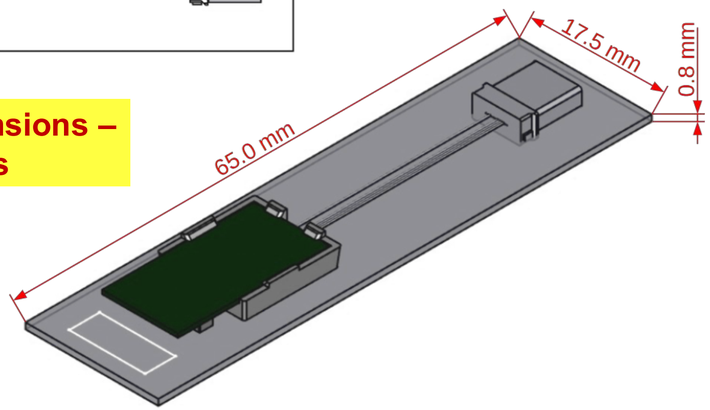
- 1 FIB for up to 4 EIC-LAS sensors
- 1 FPC control board for up to 12 FIB
  - 16 elinks per lpGBT, 4 reserved for internal FPC CB use
- 1 FIB CB for up to 48 FIB
  - 12 lpGBT links used, each connected to a 1:4 MUX



- Length of boards roughly the same driven by VTRX+ (pigtail) size
- Control boards also need space for
  - lpGBT, power regulation, monitoring, serial multiplexers
- Space to bond/solder connections on all boards



Approximate FIB dimensions – work in progress



(FIB, FIB CB, FPC CB power also being estimated, see later slide)

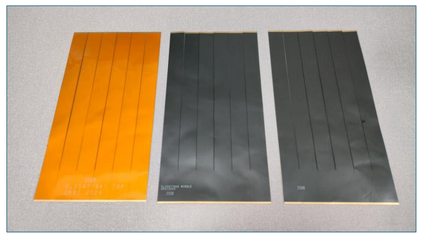
FPC prototyping and vendor selection

- **Mechanical mock-ups of IB L0 and L1** FPC procured in Cu technology to be used for IB mechanical prototypes
  - Based off ITS3 design

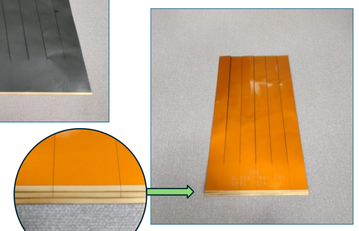
- **OB L4 ½ stave length prototype** delivered
  - Alu technology by **LTU**
  - Test setup incl. adapter boards and FPGA card ready
  - Visual inspection completed; ongoing trials of tab bonding FPC to adapter boards

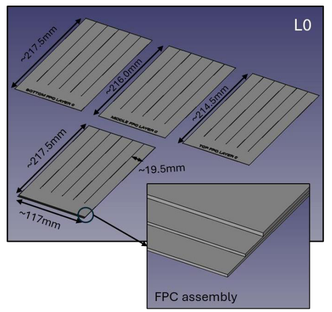
- Copy of bridge FPC ordered from alternative vendor, **QFlex**

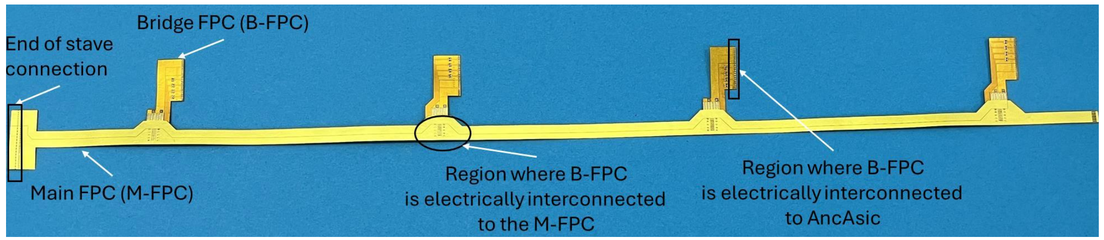
- **Two prototyping iterations completed with Omni Circuit Boards** (CA); third version under development
  - Initial tests on second iteration designed for high-speed data transmission indicate good signal integrity at 10 Gbps

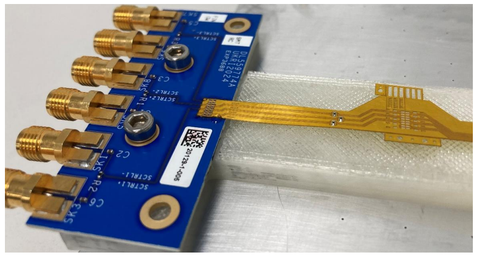


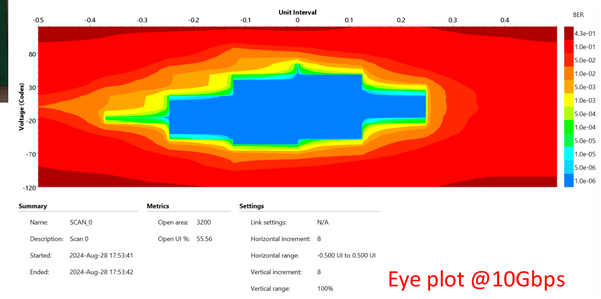
SVT IB L0 FPC
Cu mock-up











Eye plot @10Gbps

SVT readout prototypes

- Full setup with **lpGBT, VTRx+**, and FPGA development boards (stand-ins for FELIX) for evaluation of the various readout components

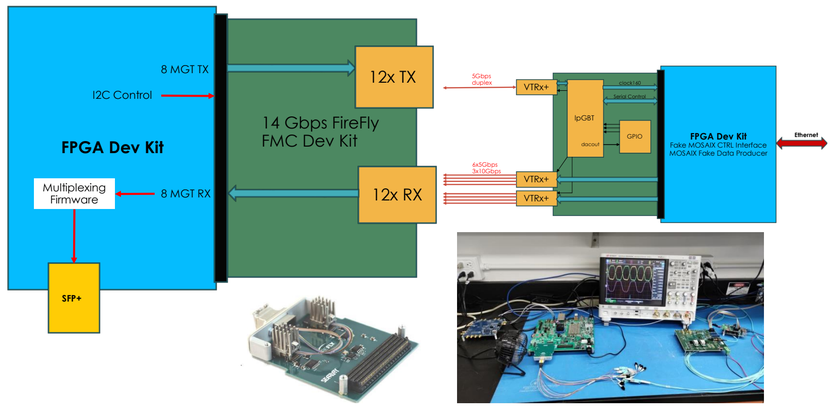
- Alternatives to CERN's lpGBT universe of components using commercial alternatives being investigated
  - Evaluation of the **Samtec Optical FireFly** as an alternative to VTRx+
  - Evaluation of the **Microchip PolarFire FPGA** as a radiation-tolerant FPGA replacement of the lpGBT

- Evaluation of **Aggregator Board** architectures with commercial FPGA development ongoing

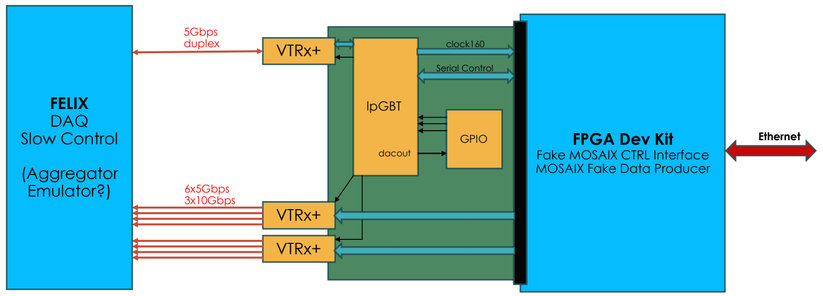
- Development of **MOSAIX hardware mockup** started

- Characterization of the **NKF7 serializer** to be used in MOSAIX and EIC-LAS ongoing

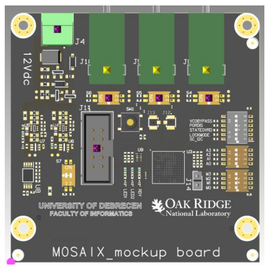
Aggregator Board Prototyping



MOSAIX Hardware Mockup



VTRx+ connected to FMC HPC (8 MGT available), emulate typical packets



Clock measurements

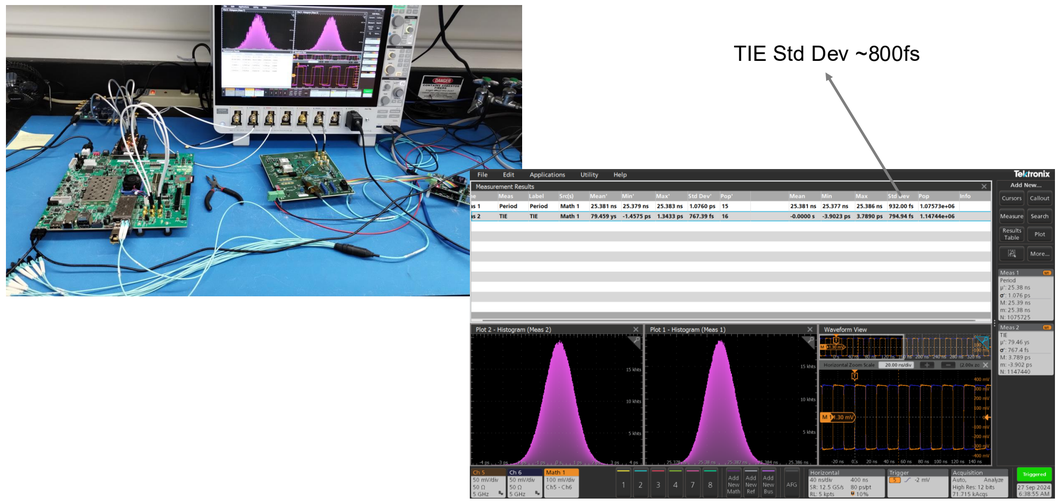
- Measurements of phase and jitter of the clock signal provided through an lpGBT link
  - Clock used by different ePIC subdetectors; test results apply more widely than the SVT
- For SVT, 10's of ps jitter are sufficient to make the PLL on the MOSAIX to lock properly
- This clock is also the means for the bunch crossing counter; needs to be stable in phase over power-cycles, to avoid calibration of clock delays each time an FEE or RDO is power cycled.

Skew and Delay Measurements

Phase Std Dev ~2.2ps

TIE Measurement with ZCU102 and Tektronix Scope

TIE Std Dev ~800fs

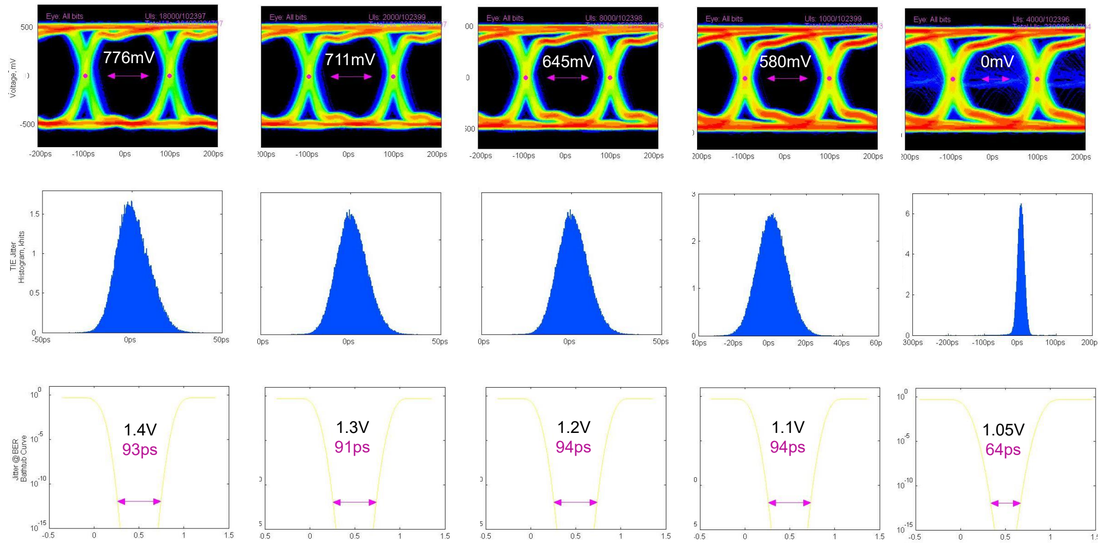


NKF7 serializer chip

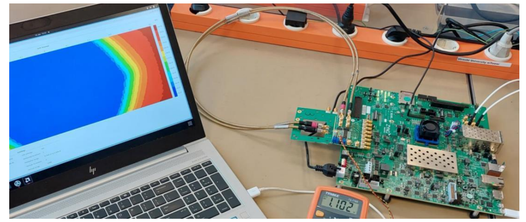
- The NKF7 serializer is going to be used in MOSAIX and EIC-LAS for data transmission off sensor on the FPC

- Characterization of the serializer prototype chip is ongoing
  - Signal integrity tests with fixed and PRBS patterns indicate stable operation at 5.12 Gbps
  - Tests continue at 10.24Gbps, and to include FPC and VTRx+ in the setup

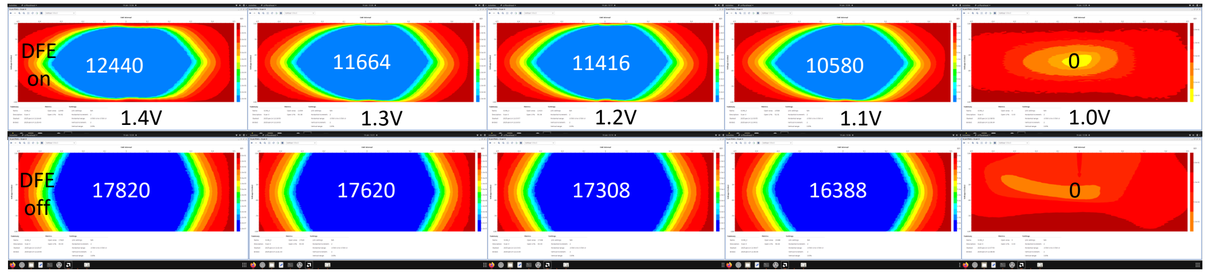
Oscilloscope Eyes with PRBS @ 5Gbps



FPGA Transceiver Statistical Eyes



Conclusion:
At 5.12 Gbps NKF7 operation seems stable
(within certain parameters)



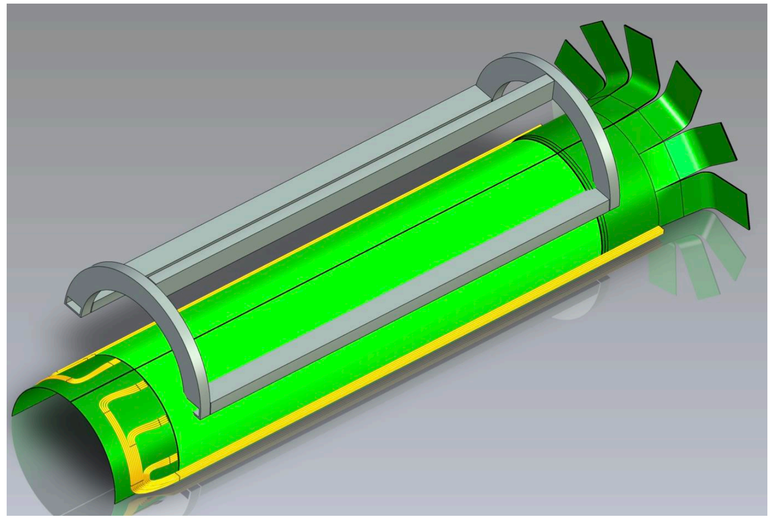
PRBS7, DFE off: 1.35V, 0 error in 20 hrs => BER< $3*10^{-15}$

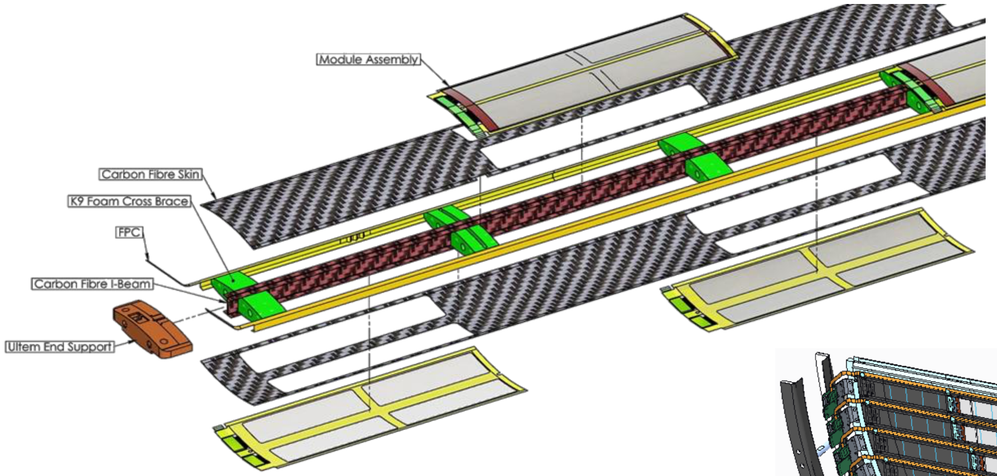
1.1V, 0 err 20 hrs => $3*10^{-15}$ <1.06V BER explodes

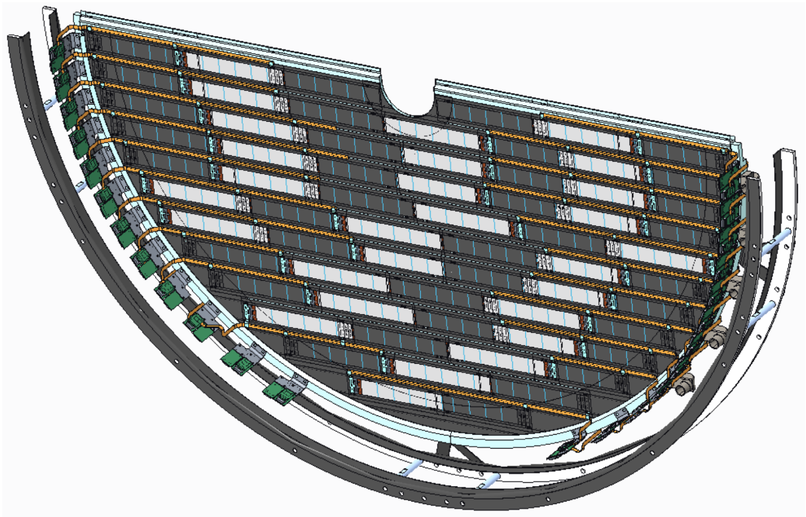
Modules, Mechanics, Cooling and Integration

Mechanical prototypes (test articles) program

- Ongoing effort for prototypes of IB layer, OB stave, disk quadrant aimed at demonstrating
  - Assembly, tooling, and procedures
  - Mechanical performance
  - Thermal performance
  - Feedback into design

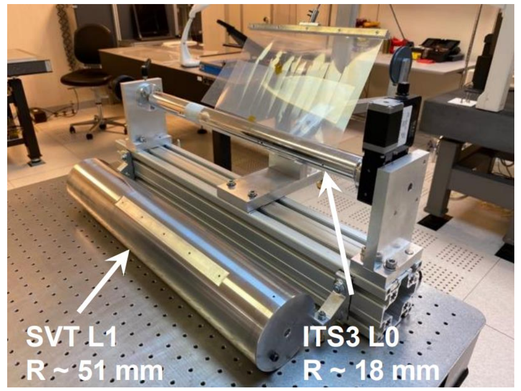


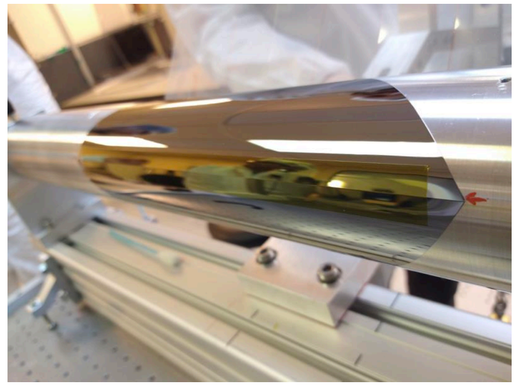




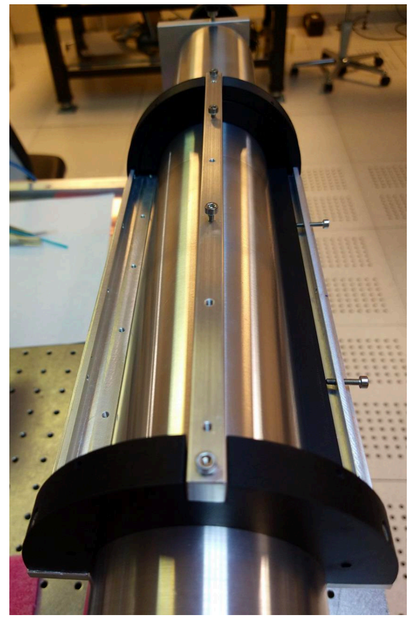
Mechanics — Inner Barrel

- SVT Inner Barrel will be constructed from wafer-scale curved ITS3 sensors
- Larger SVT radii require two or more sensors per half barrel, unlike ITS3 which uses one sensor per half barrel
- Need to precisely align the sensors, join them, handle the joint sensors during the bending, and adhere supports
- Developed and successfully exercised using thinned and diced dummy silicon wafers, 3D printed half-ring, 3D printed/plexiglass longerons
- Next steps: SVT-L1 half-layer; SVT-L0L1 half-barrel; improvements to handling and gluing tools





Attempts #	Conditions	Dates	Success	Notes
1	2 half-moon shaped L0 3D printed longerons and half-rings mandrel produced on our workshop	25/11/2024 - 26/11/2024	NO	Breakage of the second silicon piece during the bending
2	2 half-moon shaped L0 3D printed half-rings and plexiglass longerons mandrel produced on our workshop	13/01/2025 - 31/01/2025	YES	
3	2 half-moon shaped L0 3D printed half-rings and plexiglass longerons mandrel produced on our workshop	24/03/2025 - 28/03/2025	NO	One silicon piece already broken from the transport box
4	2 half-moon shaped L0 3D printed half-rings and plexiglass longerons mandrel produced on our workshop	03/04/2025 - 10/04/2025	YES	



	Prototype	Components	Goal
MAR 2025	IBL01_P1 (half-layer)	• 2 naked silicon L1 sensors • L1 local support structure (3-D printed) • outer support shell (machined in PEEK)	• finalize half-layer assembly procedure
	IBL01_P2 (half-barrel)	• IBL01_P1 + • 2 naked silicon L0 sensors • L0 local support structure (3-D printed)	• finalize half-barrel assembly procedure
JUL 2025	IBL01_P3 (half-layer)	• 2 naked silicon L1 sensors • L1 local support structure (carbon foam) • outer support shell (carbon fiber, to be defined)	• thermal chamber test
	IBL01_P4 (half-barrel)	• IBL01_P3 + • 2 naked silicon L0 sensors • L0 local support structure (carbon foam)	• thermal chamber test
OCT 2025	IBL01_P5 (half-barrel)	• 2+2 silicon L0+L1 **sensors with heaters from CERN** • L0+L1 local support structures (carbon foam) • outer support shell (carbon fiber, to be defined) • **air distribution inlet et outlet** (to be designed) • PT1000 sensors (to be glued on heater surface)	• wind tunnel test

They require dummy silicon sensors from DISCO;
to validate 2-sensor connection and bending, to design local support structure, external shell etc

In addition to DISCO dummies, they require:
- carbon foam local support (procurement and machining TBD)
- carbon fiber outer support shell TBD

(if yes, needs for design&simulation, procurement and machining)

IBL01_P5 requires:
- dummy silicon sensors with heaters
- air-cooling mechanism verification
- Possible preliminary FPC (mechanical) prototype to check volumes, transport etc)
- transport issues to wind tunnel facility

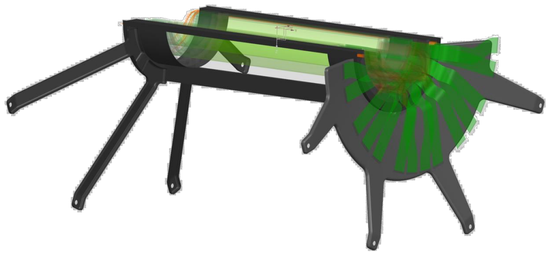
Prototype	Components	Goal	Date
IBL012_P6/7	• 2+2+4 ER2 pad wafer L0+L1+L2 sensors (x 2 HB?) • L0+L1+L2 local support structures • gloabal support mechanics (advanced design) • FPCs (advanced design) • air distribution inlet & outlet (advanced design)	• first complete IB HB prototype w/o sensors • including test of wirebonding to FPCs • final test on HB support mechanics • possibly built 2 complete HBs (to allow HB mechanical support matching test)	2026/07
IBL012_P8	• 2+2+4 ER2 wafer L0+L1+L2 sensors • L0+L1+L2 local support structures • mechanics, FPCs, cooling (~final/advanced design)	• complete IB HB prototype w/ sensors • qualification model w/ bent sensors for cooling + powering/DAQ/DCS finalisation	2026/10

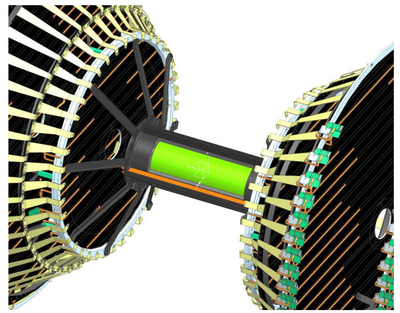
Mechanics — Inner Barrel

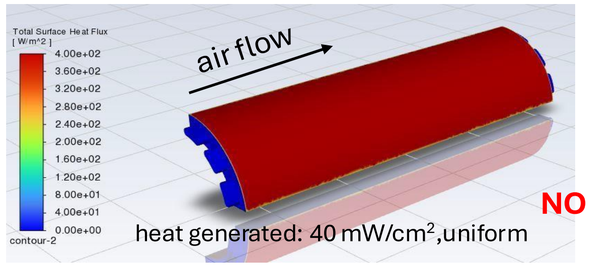
- Mechanical support design and prototypes
  - Updated L0, L1 design with supporting arms with feedback from simulations; update to L2 to follow
  - Planned prototype production by October; company already identified

- Mechanical and thermal load simulation
  - Heat transfer simulation of quarter-barrel L0+L1
    - Heavily dependent on mesh definition
    - Turbolence (critical for proper cooling) not easily set
  - Simulation of structure deformation
    - 300 μm close to the sensors, 600 μm on the edge of longerons
    - Good starting point towards effective production strategy and limited material budget

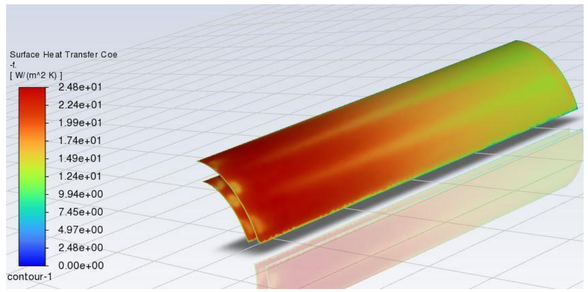
- IB transport boxes design
  - Safe handling/transportation of bent sensors of the SVT inner layers between labs
  - Plexiglass container with polystyrene holder of the sensors; designed for simplicity, robustness and durability

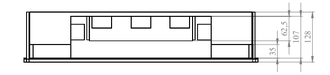


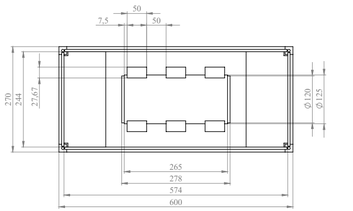


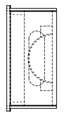


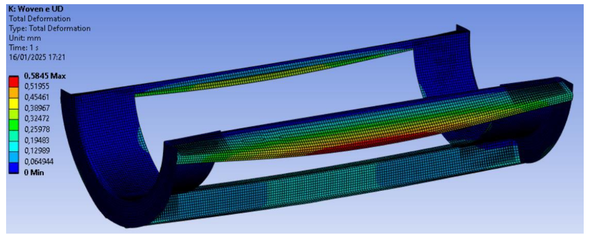
NO LEC!

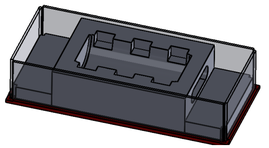






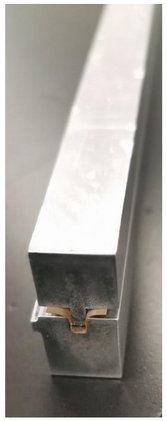




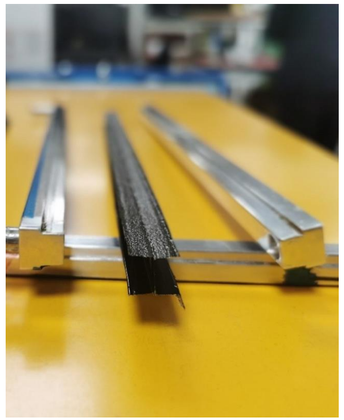


Mechanics — Outer Barrel

- Tooling developed to construct a first quarter-length L4 stave with curved facesheets

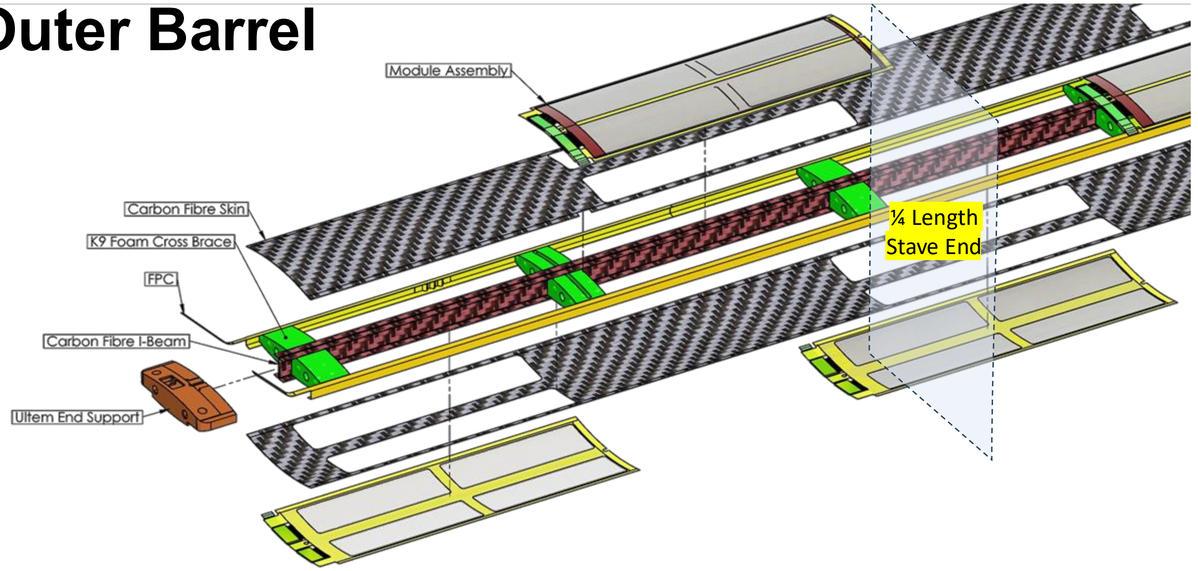


Kapton Former

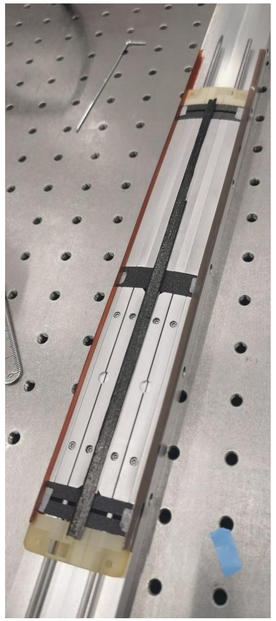


Carbon Fiber I-beam Mould

Internal Formers



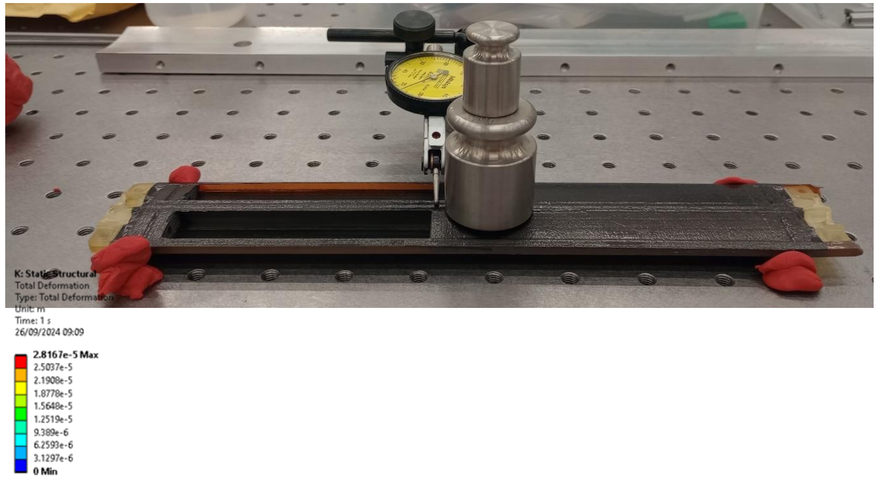
- First quarter-length stave article constructed
  - Hand-cut CF top and bottom skins (2 layers 90/0 of K13C2U/EX1515)
  - Pure Kapton FPC mock-ups
  - SLA 3D printed stave ends
  - Production intent I-beam and K9 foam blocks



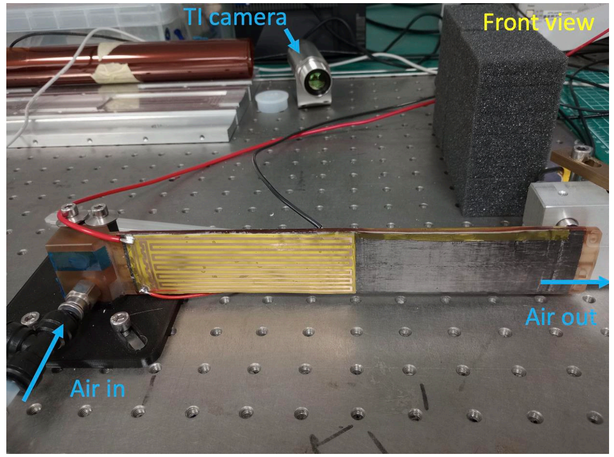
- Take-aways from the first article
  - No noticeable twist in stave
  - Strategically placed threaded holes needed for controlled removal of internal tooling
  - Reinforcement needed for end supports (deformed/failed)

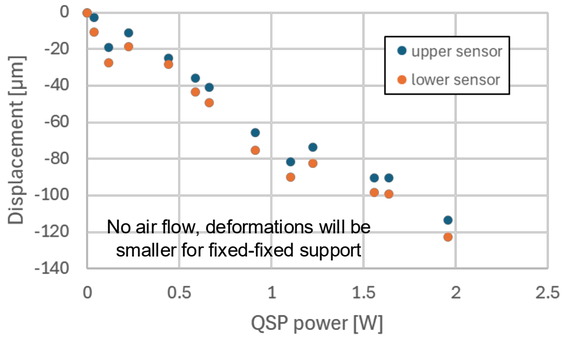
Mechanics — Outer Barrel

- Good agreement between estimated and measured mass, as well as deflections in 3pt bend tests
- ANSYS Modal model for a quarter-length stave without sensors gives a 1st mode frequency of 97Hz
- Studies started on displacements (vibrations, deformations) under dissipative load and airflow using capacitive probes – preliminary results
- Valuable lessons learned in terms of tooling and handling towards full length prototype

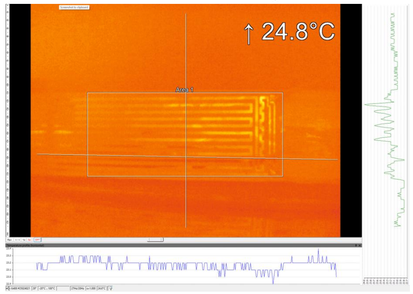


Quarter stave prototype with resistive heaters

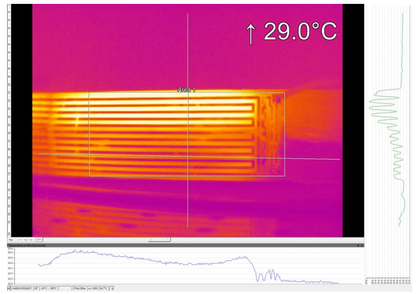


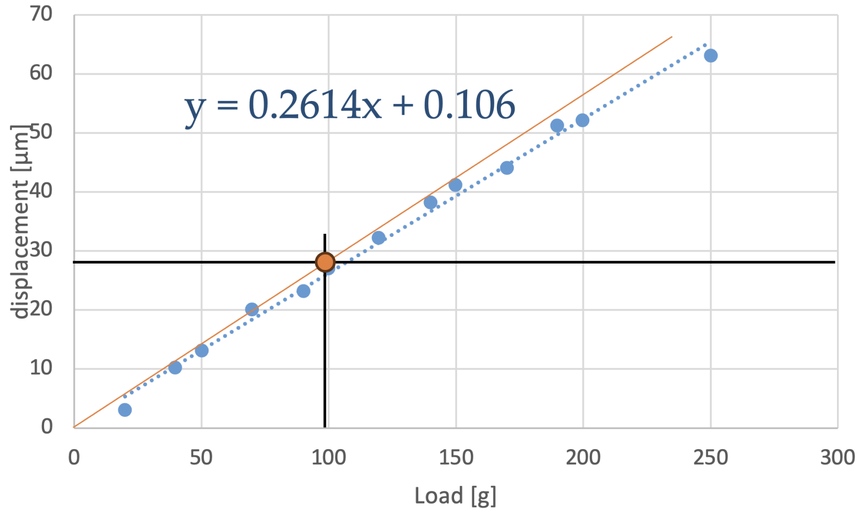


0 W, no cooling



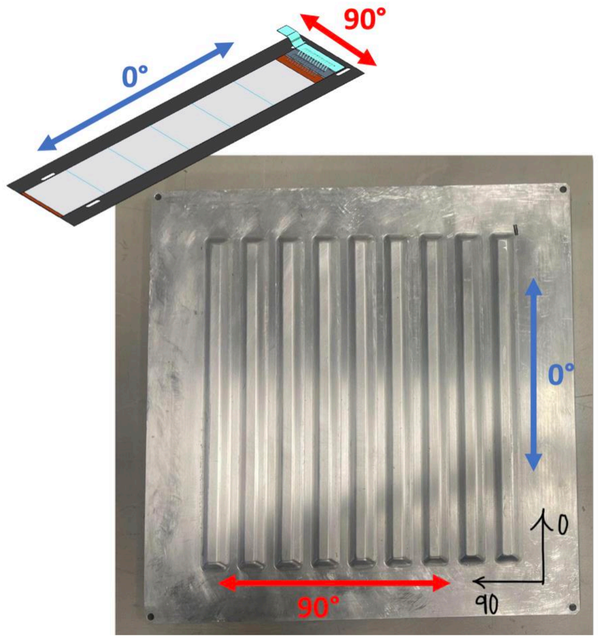
1.8 W/QSP, 30 l/min in lower channel

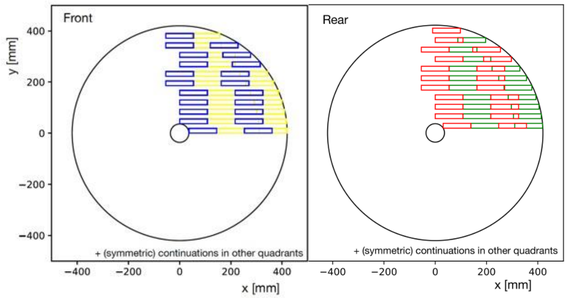


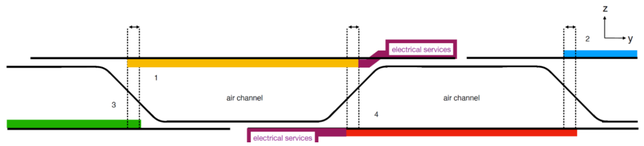


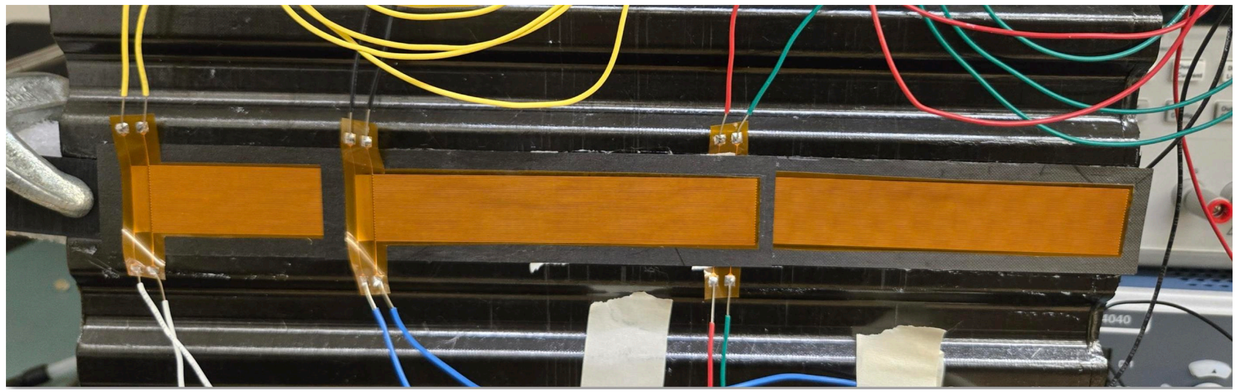
Mechanics — Disks

- Test articles created using K13C2U unidirectional high thermal conductivity CF
- Three-layer CF layups, 90/0/90 and 0/90/0, as the corrugated disk core and as the sensor support
- Thermomechanical models constructed thus far using resistive circuits (FPCs) powered separately so as to correspond to the anticipated dissipations from the EIC-LAS LEC and RSUs



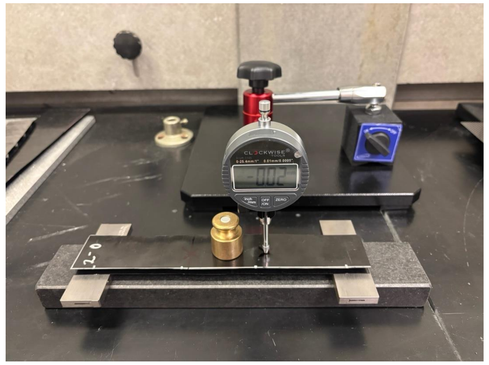


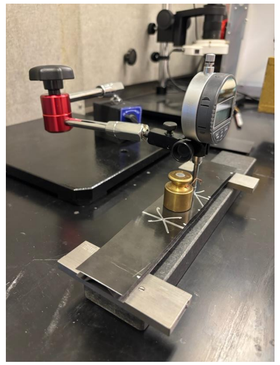


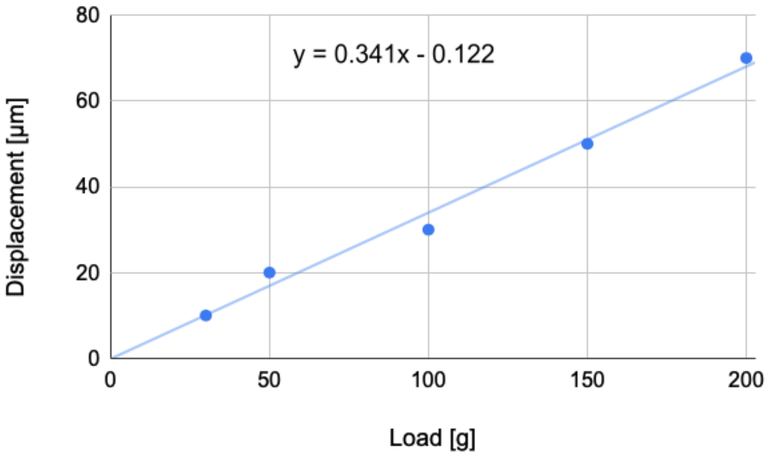


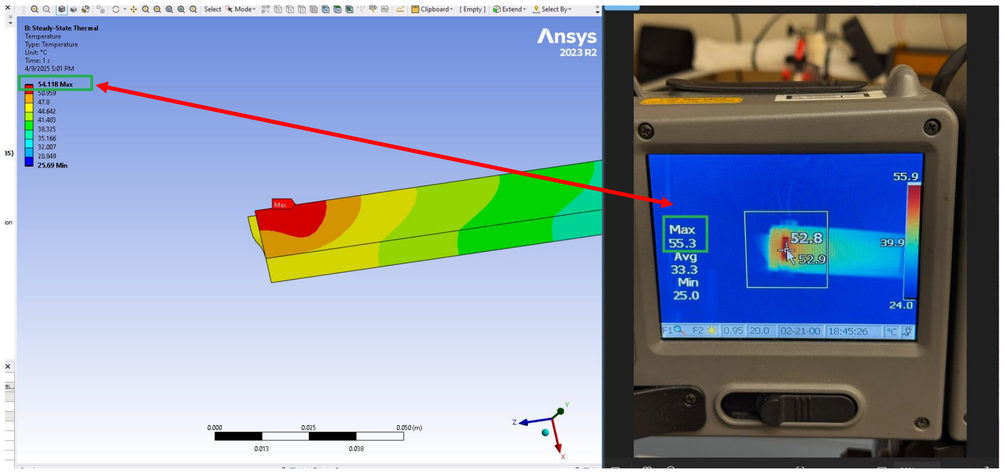
Mechanics — Disks

- 3-point bend tests performed, shown here along the corrugation, simulation to follow
  - One corrugation width, approx. length of small disc radius; load on the hump of corrugation
- Steady state thermal simulations for a single corrugation channel are in good agreement with measurements
- Studies for a range of airflows are ongoing.









SVT Cooling Strategy

- ***Baseline*** cooling design is ***air*** internal to the mechanical structure(s); liquid cooling in strategic places as necessary

- End goal is operation of SVT at/near ***room temperature*** (25 – 30C)
- Measure thermal performance with $\Delta T = T_{sensor} - T_{inlet\ air}$
- “Reasonable” ΔT is one that achieves room temperature operation with sensible air inlet temperature and air volume
- Aiming for $\Delta T < 20^{\circ}C$ (which would require 5-10 °C air)

SVT power to cool

Staves and disks
(incl. sensors, AncASIC, voltage drop on FPC)

	nominal		max	
	Power/stave [W]	Total power/system [W]	Power/stave [W]	Total power/system [W]
L0		30		37
L1		40		50
L2		101		124
L3	15.4	706	22.5	1037
L4	31.4	2199	48.2	3377
Disks		5051		7345
Total power [kW]		8.12		11.97

Readout boards - OB

	Count	Dissipation [W]
Total FIBs	372	75
Total FIB-CBs	8	171
Total FPC-CBs	32	55
Total		**301**

Readout boards - IB

	Count	Dissipation [W]
Total SIBs	68	27
Total SCBs	68	297
Total DPBs	6	88
Total		**385**

Readout boards - Disks

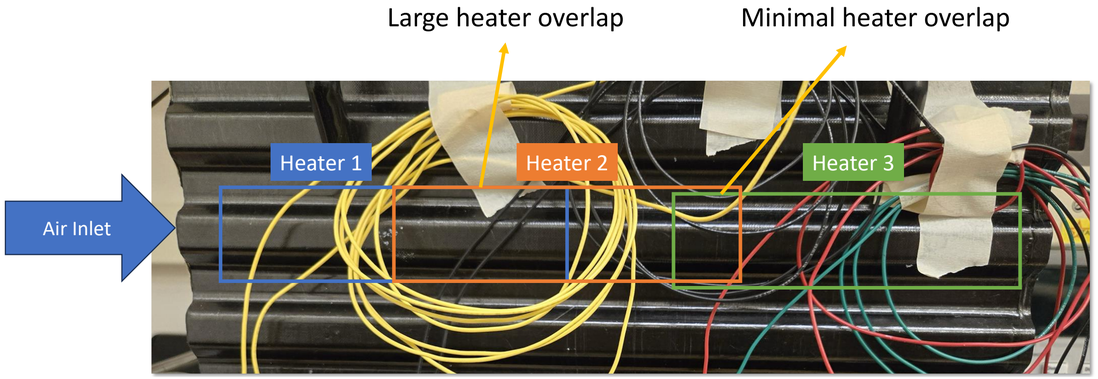
	Count	Dissipation [W]
Total FIBs	740	149
Total FIB-CBs	18	385
Total FPC-CBs	70	121
Total		**655**

- MOSAIX, EIC-LAS power estimates
  - Based on most recent MOSAIX figures; not final numbers
- AncASIC power estimates
  - Only SLDO regulators power consumption; by far the largest contribution, but will need to include NVG and AncBrain
- Readout boards power estimate
  - lpGBT and VTRX+ power consumption figures
  - MUX power consumption (FIB SC only)

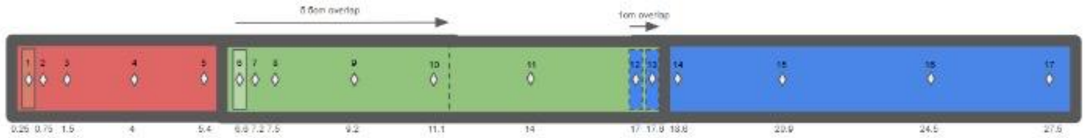
Sensors + AncASIC: ~ 8 – 12 kW
Readout boards: ~1.4 kW

Thermal prototype measurement

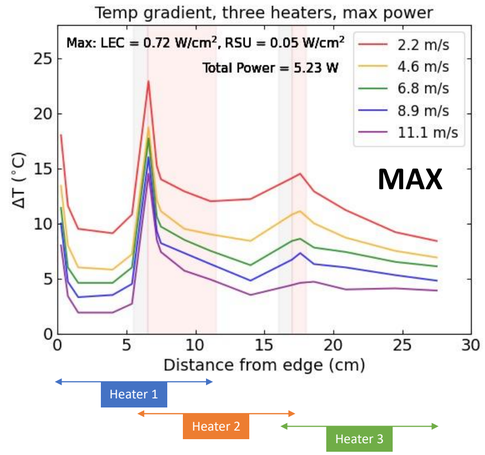
- Three heaters placed on one corrugated channel, with two overlap regions
- Tested at nominal and max power for 6 RSU EIC-LAS, using thermal camera, ~0.5°C fluctuations
- $\Delta T = T_{BrightTemp} - T_{DarkTemp}$
  - Dark temp: air flowing, no power
  - Bright temp: air flowing, power on

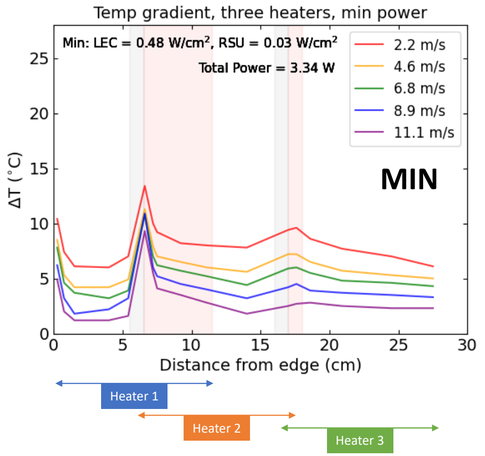


Measurement points

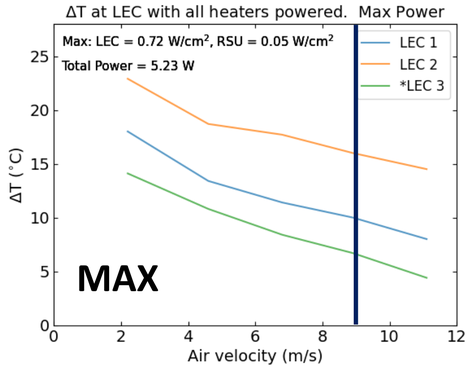


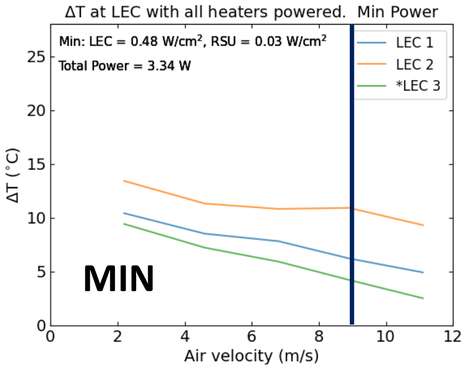
- At 9m/s:
  - RSU: ΔT < 10°C for MAX and < 5°C for MIN
  - LEC: ΔT < 20°C for MAX and < 15°C for MIN
- ΔT dependent on overlap and proximity to air flow/edge of disc





LEC3 cannot be directly measured and is therefore a measurment of the RSU with the LEC behind it





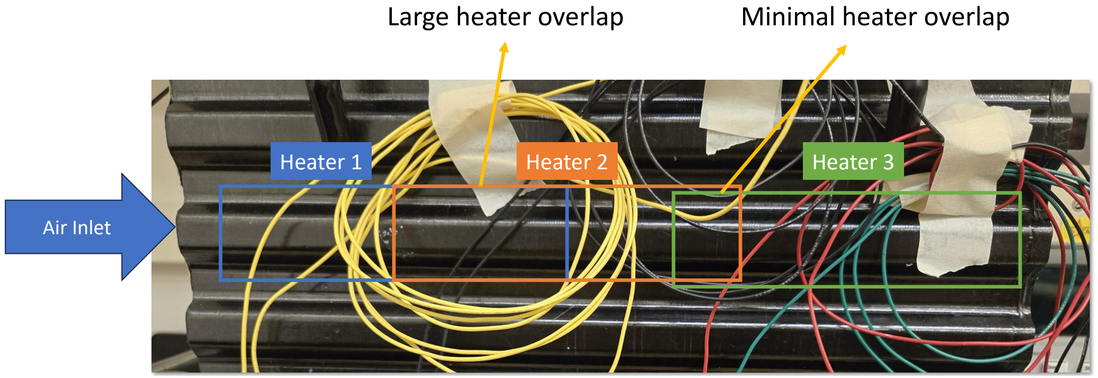
Heat transfer coefficient, h

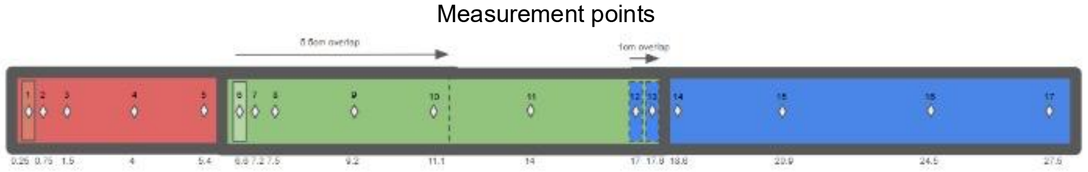
- h is dependent on air properties, changes with velocity and temperature; measured based on q (power density) and ΔT

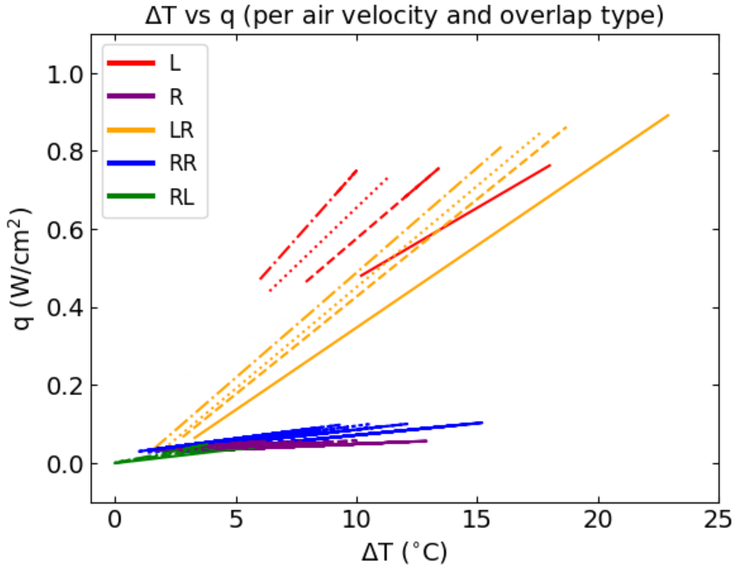
$$h \sim \frac{q}{\Delta T}$$

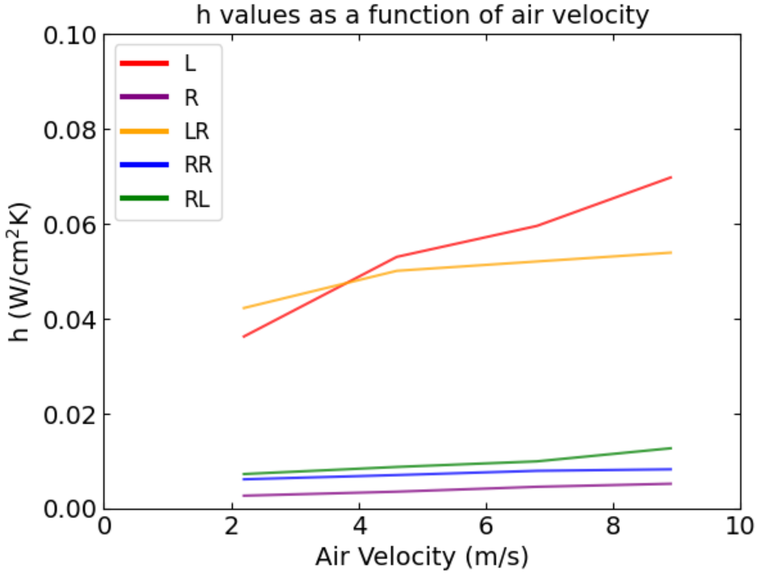
- Different regions of power density: L, R, LR, RR, RL (e.g. LR is LEC with RSU behind)

- Plot q vs ΔT separately for each region and each air velocity; extract h from slope









Remaining R&D Milestones

Remaining R&D Milestones

eRD104 (service reduction)

Develop powering scheme based on serial powering to mitigate service space needs of DC-DC scheme (December 2023)

Complete. A serial powering scheme has been developed that will make it possible to power a group of up to four EIC Large Area Sensors with a single current loop. This scheme relies on the development of an Ancillary ASIC, separate from the EIC Large Area Sensor. Specifications have been developed, a technology choice has been made, and an initial MPW submission with test-blocks has been made. Further work will be carried as PED.

Evaluate radiation tolerant FPGAs and high-speed fiber optic transmission option with beam test. Complete prototype multiplexing firmware (December 2024)

The readout and slow control scheme has been developed in conjunction with the serial powering scheme. The core components for the baseline scheme, beyond the Ancillary ASIC, are the VTRx+ optical link module developed for the higher radiation environments at the LHC and lpGBT (low power Gigabit Transceiver). Test setups for this scheme and for the originally envisioned alternative scheme based around commercial components are in place at ORNL. Bench tests have been performed. A test board for high-speed data transmission is now available at ORNL and is being refined.

Remaining R&D Milestones

eRD111 (SVT)

Report completed on barrel and disk cooling options, allowing cooling choice (December 2023)

Report is outstanding. ALICE ITS3 has demonstrated that air cooling is feasible for their array of vertex layers. SVT will make use of the ITS3 sensor for its Inner Barrel. Air cooling by forced convection internal to the support structures of the SVT Outer Barrel and Disks has been investigated for anticipated power density profiles associated with the EIC Large Area Sensor currently under development. This has been done with thermomechanical mockups and, in select cases, cross-validated with ANSYS simulations. Air cooling is considered a viable option for SVT operations near ambient temperatures, provided that the power dissipation in the EIC LAS sensor can indeed be reduced as projected compared to the MOSAIX periphery and that power dissipation in the Ancillary ASIC will be well below that of the EIC LAS itself. Liquid cooling has material and service load implications and trade-offs in its use in strategic places are being investigated.

R&D completed for stitching of sensors (September 2024)

Tiling studies on the staves of the SVT Outer Barrel and the Disks, combined with current foundry insights, have shown that single segments with 5 or 6 stitched Repeated Sensor Units will result in an EIC LAS that meets SVT acceptance and other requirements. For reference, the SVT Inner Barrel will make use of wafer-scale MOSAIX sensors that contain three to five segments each with 12 stitched Repeated Sensor Units. With this specification for the EIC LAS, the SVT will have approximately 4,000 EIC LAS.

Developing EIC LAS through modification of MOSAIX requires access to the MOSAIX design database (technology transfer) and is subject to a CERN-EIC agreement. This currently hampers progress.

Remaining R&D Milestones

eRD113 (MAPS/ITS3/MOSAIX)

End of R&D Milestone: EIC vertex sensor (MOSAIX) quantification finalized (September 2025)

Tape-out of ER2/MOSAIX at CERN is currently anticipated to be in May or June 2025. Samples are then expected by year-end and initial validation a few months after. Work beyond ER2 will be carried as PED, since this is towards production-readiness sensors.