



dRICH photosensors

Roberto Preghenella INFN Bologna

on behalf of the dRICH Collaboration

preghenella@bo.infn.it PID review, 2 April 2025

Outline

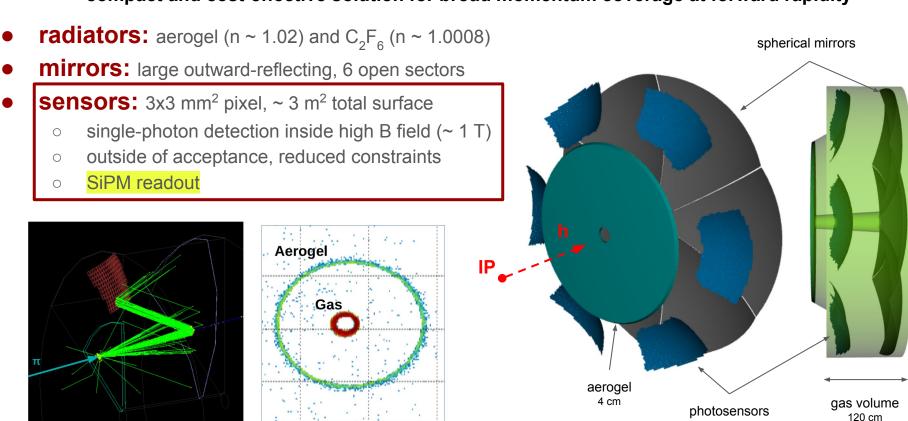
- introduction
- sensor technical specs
- radiation level estimates
- high-temperature annealing
- sensor optimisation
- photodetector QA

the presentation will also address comments received from the last review report

The dual-radiator (dRICH) for forward PID at EIC



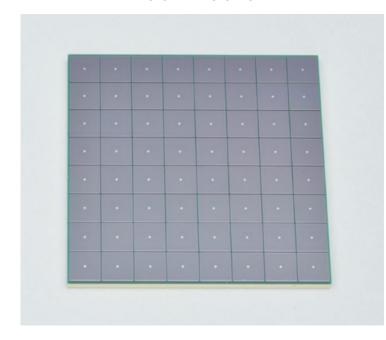
compact and cost-effective solution for broad momentum coverage at forward rapidity



SiPM technical specs

baseline sensor device

64 (8x8) channel SiPM array 3x3 mm² / channel



Parameter	Value	Notes
Package type	SiPM array	
Package dimension	$< 26 \times 26 \text{ cm}^2$	
Mounting technology	surface mount	
Number of channels	64	
Matrix layout	8 × 8	
Channel size	$3 \times 3 \text{ mm}^2$	
Fraction of active area in package	> 85%	
Microcell pitch	50 - 75 μm	
Protective window material	silicone resin	radiation & heat resistant
Protective window refractive index	1.55 - 1.57	
Spectral response range	300 to 900 nm	
Peak sensitivity wavelength (λ_{peak})	400 - 450 nm	
Photon detection efficiency at λ_{peak}	> 40%	
Breakdown voltage (V _{break})	< 60 V	
Operating overvoltage (Vover)	< 5 V	
Operative voltage (Vop)	< 64 V	
Max V _{op} variation between channels	< 100 mV	at $T = -30^{\circ}C$
Channel dark count rate (DCR)	< 50 kHz	
DCR at $T = -30^{\circ}C$	$< 5 \mathrm{kHz}$	at $T = -30^{\circ}C$
DCR increase with radiation damage	$< 500 \text{ kHz}/10^9 \text{ n}_{eq}$	at $T = -30^{\circ}C$
Residual DCR after annealing	$< 50 \text{ kHz} / 10^9 \text{ n}_{eq}$	at $T = -30^{\circ}C$
Terminal capacitance	< 500 pF	
Gain	$> 1.5 10^6$	
Recharge time constant (τ)	< 100 ns	
Crosstalk (CT)	< 5%	
Afterpulsing (AP)	< 5%	
Operating temperature range	−40 to 25°C	
Single photon time resolution (SPTR)	< 200 ps FWHM	

Table 8.5: Baseline specifications of the SiPM sensor devices for the dRICH photodetector. All parameters are defined at room temperature ($T = 25^{\circ}C$) and at the operating voltage V_{op} , unless otherwise specified.

SiPM requirements for RICH optical readout





pros

- cheap
- high photon efficiency
 requirement
- excellent time resolution
- insensitive to magnetic field
 requirement

cons

large dark count rates not radiation tolerant

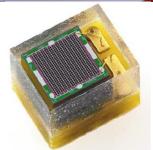
technical solutions and mitigation strategies

cooling
timing

annealing

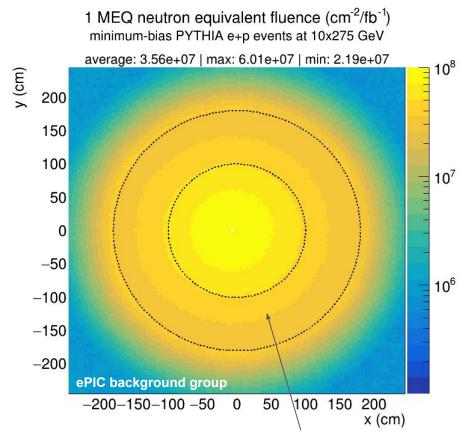


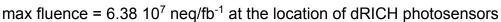


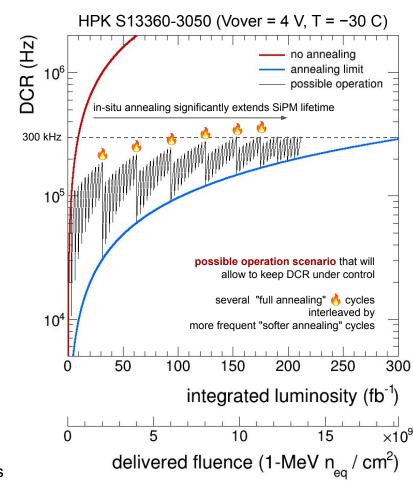


Radiation level estimates update



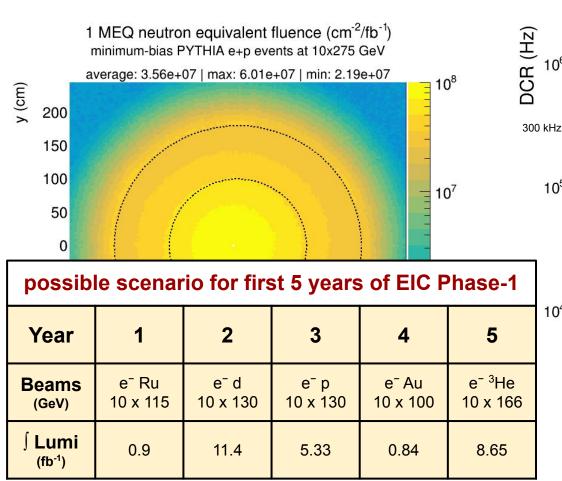


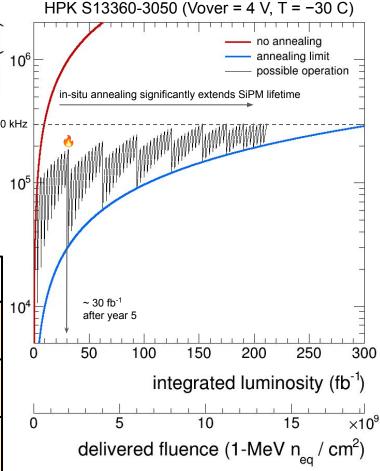




Radiation level estimates update







<u>Comment:</u> We advise exploring the operation of SiPMs at a lower temperature (for example -40C) to guarantee a low level of DCR.

The baseline for the SiPM operation temperature in the experiment is T = -40 C. We show predictions at T = -30 Cas they are based on R&D measurements performed at that temperature. For reference, we reached T = -40 C in recent beam tests and below T = -50 C in laboratory tests, using commercial fluid-based chillers assisted by Thermoelectric Cooling elements (not foreseen to be used in the experiment). These and future studies will provide guidance and reference data for the advance and the engineering of the SiPM cooling system.

High-temperature annealing

done R&D on SiPM radiation damage and recovery with annealing

- o irradiation tests on large samples of SiPMs with protons, neutrons and gamma
- high-temperature annealing based on "oven" annealing
 - ~ 3% irreducible residual damage with T = 150 C integrated for 150 hours
- tested realistic situation with repeated irradiation-annealing cycles
 - irreducible residual damage builds up

developed "online" self-heating annealing process

- o "oven" annealing is not a practical approach in a large detector (it is also not desirable to often dismount it)
- performed detailed studies as a function of temperature and time
- o achieved the "oven" performance with forward-bias current

engineering annealing towards safer control in the experiment

- laboratory measurements of a promising temperature control strategy
- fluid-assisted to reduce stress on electronics and power requirements

designing electronics that fulfils annealing requirements

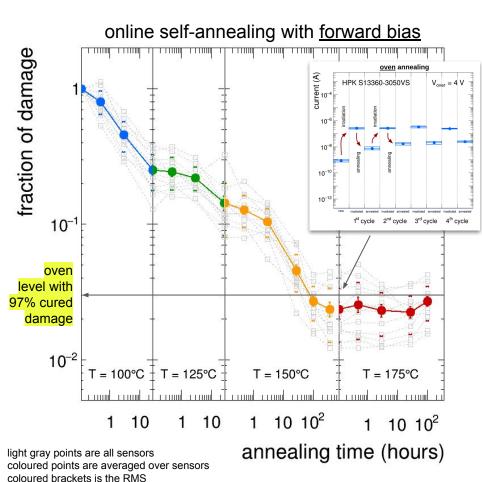
- circuitry that withstands high currents
- protect the ASIC
- board production starting in coming weeks
 - annealing tests to be concluded by the end of 2025

<u>Comment:</u> The reviewers also suggest considering the option of replacing the SiPM array once during the experiment lifetime as an alternative to the "oven" annealing process.

The forward-bias self-annealing technique can achieve a similar recovery performance as that of the "oven" annealing process. Performing "oven" annealing is not foreseen anymore. Nonetheless, we consider the suggestion to replace the SiPM arrays as an alternative to avoid over-annealing. We are also closely following advancements in new SiPM technologies for a potential future upgrade.

Detailed studies of SiPM online self-annealing





test on a large number SiPM sensors how much damage is cured as a function of temperature and time

the same sensors have undergone self-annealing increasing temperature steps increasing integrated time steps

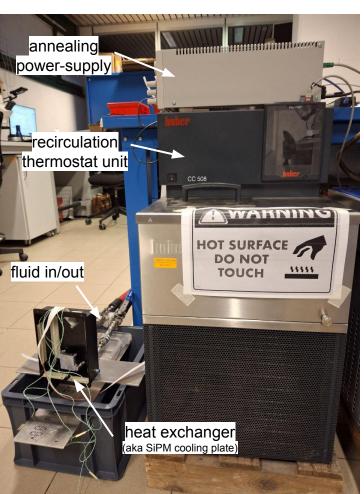
- started with T = 100 C annealing
 - performed 4 steps up to 30 hours integrated
- followed by T = 125, 150 and 175 C

residual damage saturates at 2-3% reached same level of "oven" annealing

at a higher T = 175 C we do not to cure more than that

Fluid-assisted online self-annealing process



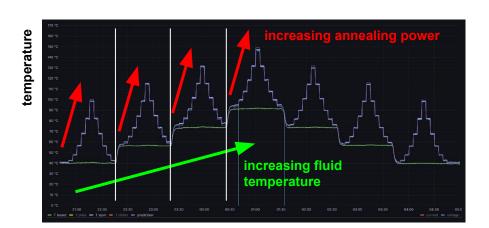


new dedicated laboratory test-stand

fluid-based (silicone) circulating thermostat system keep the SiPM PCB board at a controlled temperature cooling (-55 C) and heating (105 C) mode possible while delivering forward-bias current for annealing

SiPM temperature measurements as function of

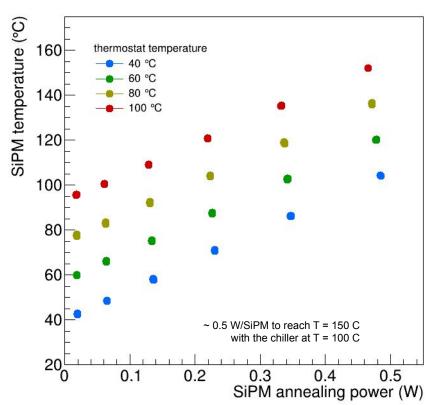
- circulating-fluid temperature
- annealing power



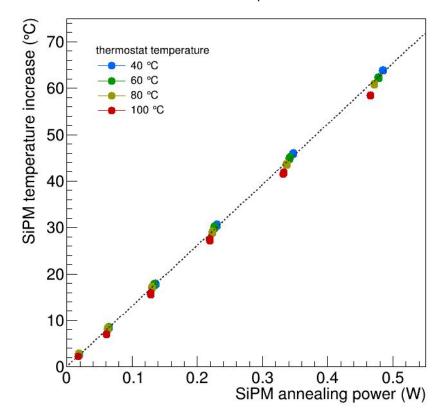
Forward-bias annealing control



SiPM temperature increases proportionally to annealing power



constant increase wrt. the temperature of the PCB board

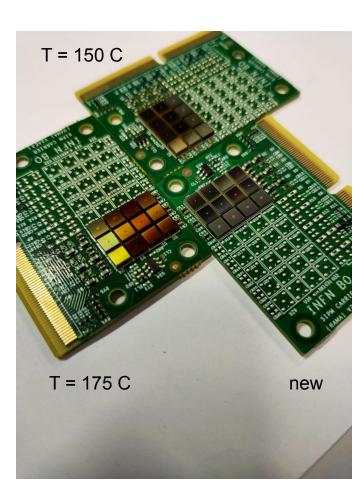


<u>Comment:</u> To reduce dark current, heavy annealing is planned. It is required to check that the charge collection efficiency is not reduced due to over-annealing. The reviewers understand that this is part of the ongoing R&D campaign and that encouraging first results have been obtained.

We tested the forward-bias self-annealing technique at different temperatures and integrated annealing times. We observed an <u>unexpected degradation of the protective silicone window</u>. A corresponding decrease in PDE is measured. Such effects were not observed with "oven" annealing. This is not considered significantly worrisome, as no degradation is observed for the required self-annealing temperatures and integrated times. Nevertheless, further tests will be carried out.

Detailed studies of SiPM online self-annealing



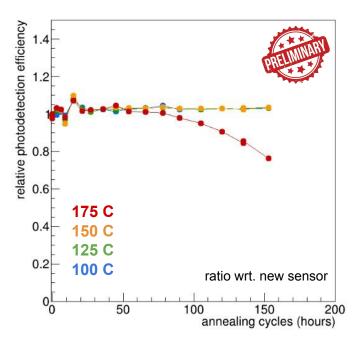


after many hours of online annealing

we noticed alterations on the SiPM windows in particular in one board that underwent

500 hours of online annealing at T = 175 C

the sensors appear "yellowish" when compared to new



preliminary results indicate efficiency loss after 100 hours of annealing at T = 175 C

up to T = 150 C temperatures the sensors are unaffected up to 150 hours of integrated annealing

this is not worrisome, because as we have seen **we don't need to go beyond T = 150 C**

but this was unexpected: previous measurements after long **oven annealing do not show any modification** of SiPM efficiency / transparency

we plan a new set of measurements with the SiPM annealing to be done in dry environment

<u>Comment:</u> The online annealing procedure requires forward biasing of the sensors creating local heat generation and large current flows close to the front-end electronics. Precautions will have to be taken to avoid damage to the ASIC. It was understood that this is a part of the R&D effort, for example, through the use of MOSFETs to protect the readout.

The circuit that allows high-current forward-bias annealing and at the same time protects the ASIC and ensures signal integrity has been studied. The latest design employs diodes instead of MOSFETs to reduce complexity in the electronics. A <u>dedicated "annealing" board is being designed for realistic tests</u> that will be performed by the end of 2025.

<u>Comment:</u> For online self-annealing, all materials, including glue, PCB, etc., have to be checked to see if these are tolerant to the high temperature and if the thermal cycling does not affect the components due to CTE mismatch.

In conjunction with the tests to evaluate the electronics circuits for annealing, we plan to carry out some <u>tests to study and quantify the performance of the present design of the PDU and of its components and materials</u>. These studies will also provide critical guidance for the final engineering as well as important reference <u>data for simulation of heat-dissipation</u> and the design of the cooling system.

Annealing FEB and PDU head prototypes



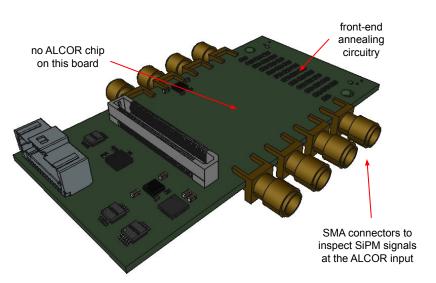
currently designing a special "Annealing-FEB"

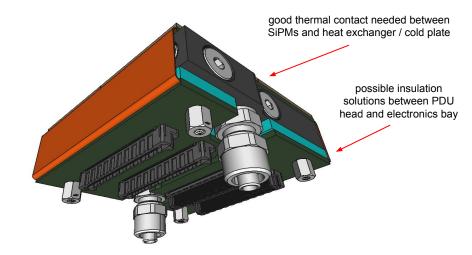
features

- all necessary circuitry as the final FEB
- but no ALCOR chip, instead it has
- SMA connectors to inspect SiPM signals on scope

goals

- test realistic dRICH annealing electronics
- validate basics annealing elements
- study/engineering of annealing process details





Annealing-FEB mates with the PDU as a normal FEB

Few prototypes of the latest version of PDU head will be produced **goals**

- first tests of assembly procedures and materials
- study thermal performance within PDU elements
- test SiPM signal transmission/integrity towards ALCOR
- test annealing cycles with a complete realistic PDU module

Assembly of a small dRICH photodetector box to aid engineering simulations, heat propagation and cooling requirements

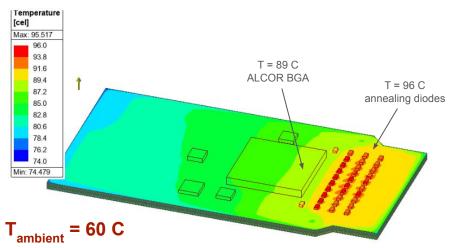
Annealing in the dRICH PDU

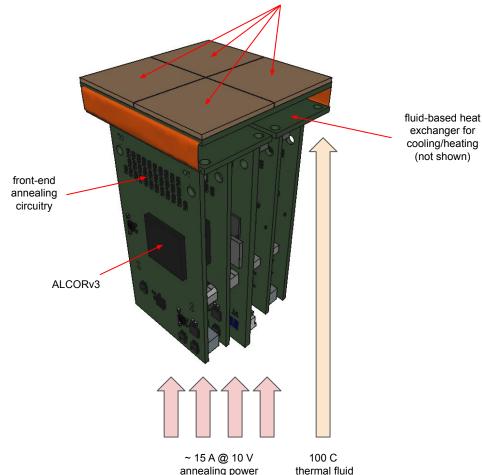
4x NTC temperature sensors on the side of the PCB in contact with the heat exchanger

preliminary thermal simulations

of the FEB board while performing annealing embedded in a static T = 60 C ambient note: this is a first and simplified simulation of the board without air circulation and without taking into account other heat sources and the complexity of the surrounding environment

first **guidance** on the possible temperature profiles useful to put **requirements** on dRICH box cooling valuable to **compare** with simplified test benches





Optimisation of photosensor performance

timing performance measurements

- shown already during last review
- better resolution with larger 75 μm SPAD sensors (larger signal)
 - already good at low over-voltage
 - possible to improve with next version of ASIC (larger bandwidth)

DCR vs. PDE performance measurements

- o clear that S13360 Hamamatsu sensors are superior than S14160 ones
- o better performance from 75 μm SPAD sensors wrt. 50 μm, also after irradiation & annealing

beam test measurements

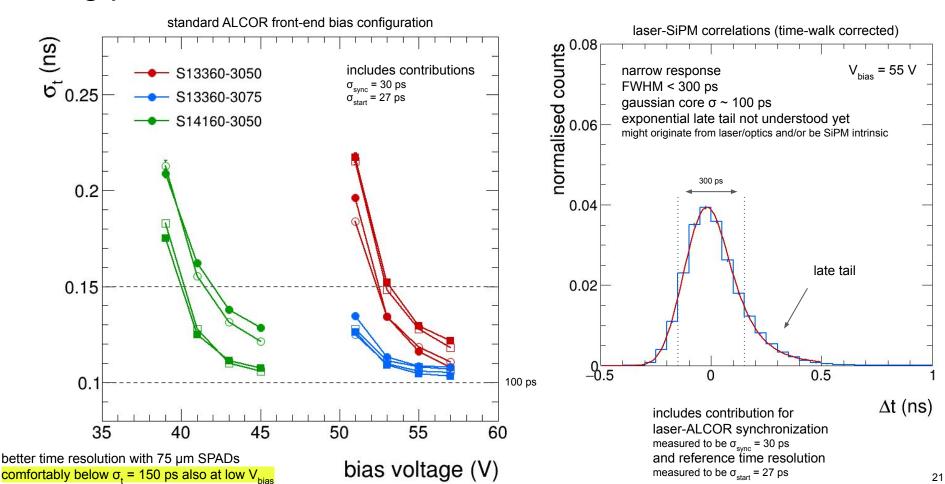
o confirmation also with Cherenkov light that 75 μm SPADs detect more photoelectrons

new UV-enhanced Hamamatsu devices

- faster recharge time
- larger efficiency
 - final evaluation and beam tests by end of 2025

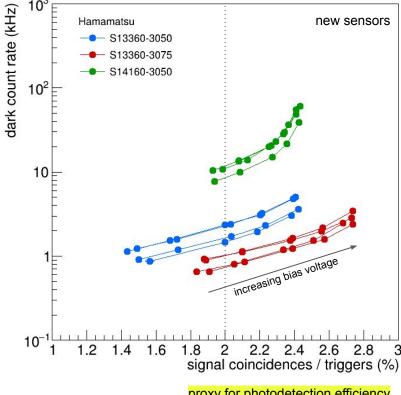
Timing performance measurements with ALCOR





DCR vs. PDE comparison between sensors

3 Hamamatsu sensor types, 4 sensors each measured as NEW



proxy for photodetection efficiency



these studies have been performed with the full ALCOR readout prototype electronics chain

at the same level of detection efficiency namely, the probability to detect light from laser pulse different sensors have different DCR level

best: S13360-3075

most promising sensors, large pitch SPADs (75 μm)

second: S13360-3050

same technology, medium pitch SPADs (50 µm)

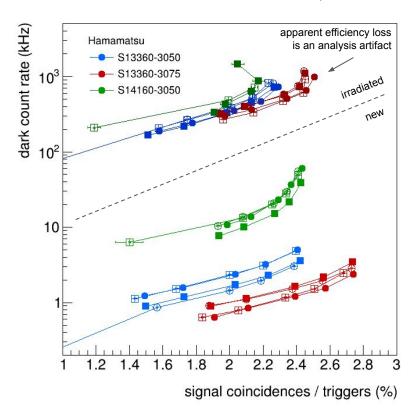
worst: S14160-3050

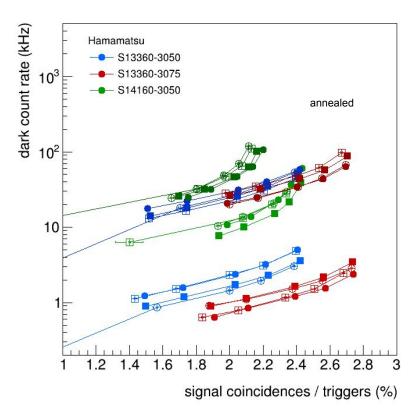
different technology, medium pitch SPADs (50 µm)

DCR vs. PDE comparison between sensors



after proton irradiation with 10^9 1-MeV n_{eq}/cm^2 and after over annealing (150 hours at T = 150 C)



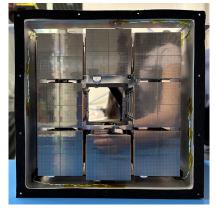


S13360-3075 sensors (75 μ m SPADs) are always at the bottom-left meaning it has higher PDE at the same DCR troubles with S14160-3050 sensors after irradiation, they also show lower efficiency after annealing

Comparison between different SiPM sensors



same Hamamatsu technology, different SPAD sizes on the beam line

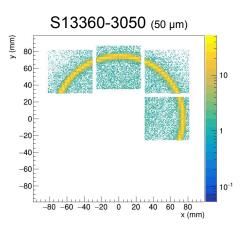


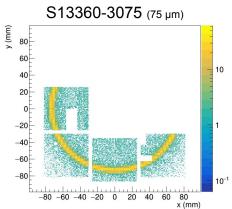
dRICH readout plane in 2024 beam test at CERN-PS

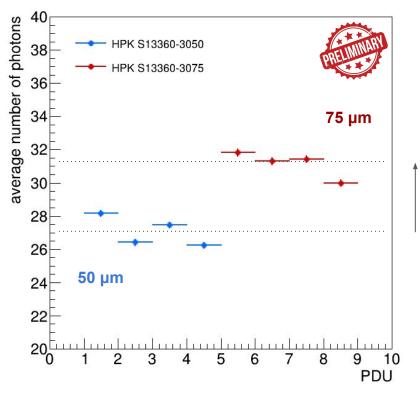
equipped with

- 4x PDUs with 50 μm sensors
- 4x PDUs with 75 μm sensors

to test Cherenkov performance of different SPAD sizes

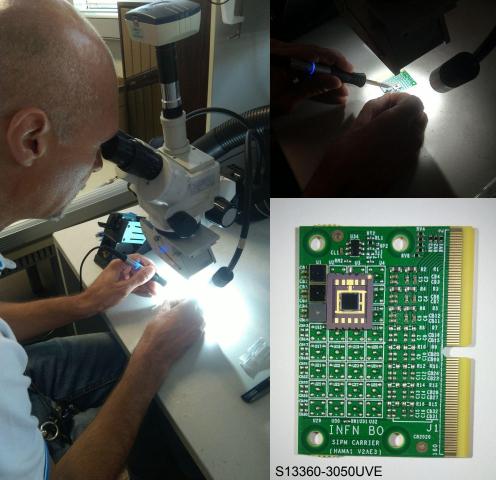






New Hamamatsu SiPM prototypes (UVE)





newly-developed Hamamatsu SiPM sensors based on S13360 series

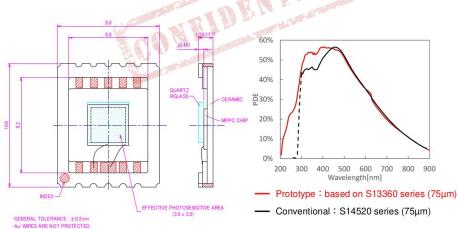
received few samples of 50 μm and 75 μm SPAD sensors

on paper they look VERY promising

- improved NUV sensitivity
- improved signal shape
- improved recharge time

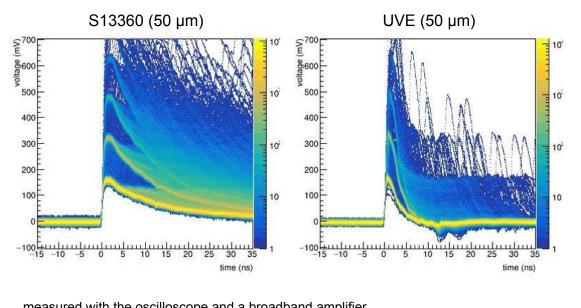
mounted on EIC SiPM test boards performed characterisation measurements

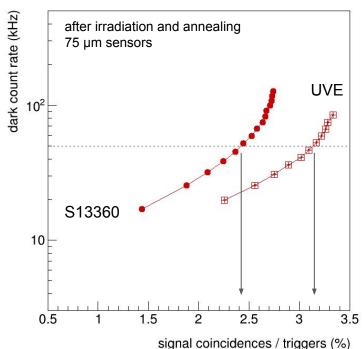
irradiation, annealing, laser, ...



Faster recharge time, higher PDE

we compared the standard commercial Hamamatsu S13360 sensors with the UVE prototypes





measured with the oscilloscope and a broadband amplifier

UVE sensors have > 5x faster recharge time with the same signal amplitude

→ lower pile-up probability at high DCR

measured with the ALCOR electronics readout chain

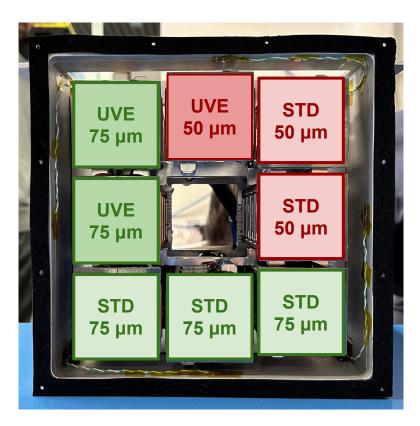
UVE sensors have > 30% higher PDE at the same DCR of 50 kHz note: this is measured with a 400 nm laser and the prototype have a guartz protective window

check with Hamamatsu for custom devices with silicone protective window

New Hamamatsu SiPM prototypes on the beam line



aim at a the next dRICH beam test to evaluated the sensors with Cherenkov light



meeting with Hamamatsu engineers

- productive meeting in September 2024
- they can provide what we want, namely
 - SiPM matrices 8x8 with UVE sensors
 - SMD mounting
 - silicone resin window

purchased and received

- 4x matrices with 50 μm SPADs
- 12x matrices with 75 μm SPADs
- several single-SiPM sensors

goal

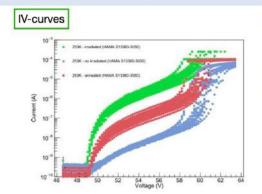
- assemble few new PDUs
- use them in the next beam test
- evaluate expected PDE improvement

Photosensors Quality Assurance



ALCOR based QA stations being developed at INFN CS-SA-CT and INFN TS in collaboration with local Universities







- 253K-no irradiated
- 253K-annealed
- 253K-irradiated



In-depth characterization station operative at INFN-BO: PDE - Timing





Summary



- dRICH SiPM readout fulfills requirements
 - insensitive to magnetic field
 - excellent single-photon timing and efficiency
- technical solutions to mitigate radiation damage
 - low temperature operation
 - "in-situ" self-annealing with forward-bias currents
 - engineering of annealing process and electronics
 - design & production of prototypes
 - measurements from realistic test stands in 2025

optimisation of SiPM photosensors

- o better performance from larger SPADs (75 μm) commercial Hamamatsu sensors
 - across the line: time resolution, DCR vs. PDE, beam tests
- further optimisation of signal shape and PDE is possible
 - laboratory measurements on UV-enhanced Hamamatsu sensors
 - tailored pre-production of photosensors received
 - final evaluation and beam tests of UVE by end of 2025

clear path towards TDR and production

- sensor procurement operations starting in 2026
- QA tests stations and manpower are available