OAK RIDGE National Laboratory

H2GCROC3A testing

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(Debrecen)
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H2GCROC3A architecture

Overall chip divided in two symmetrical parts:

- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

Measurements:

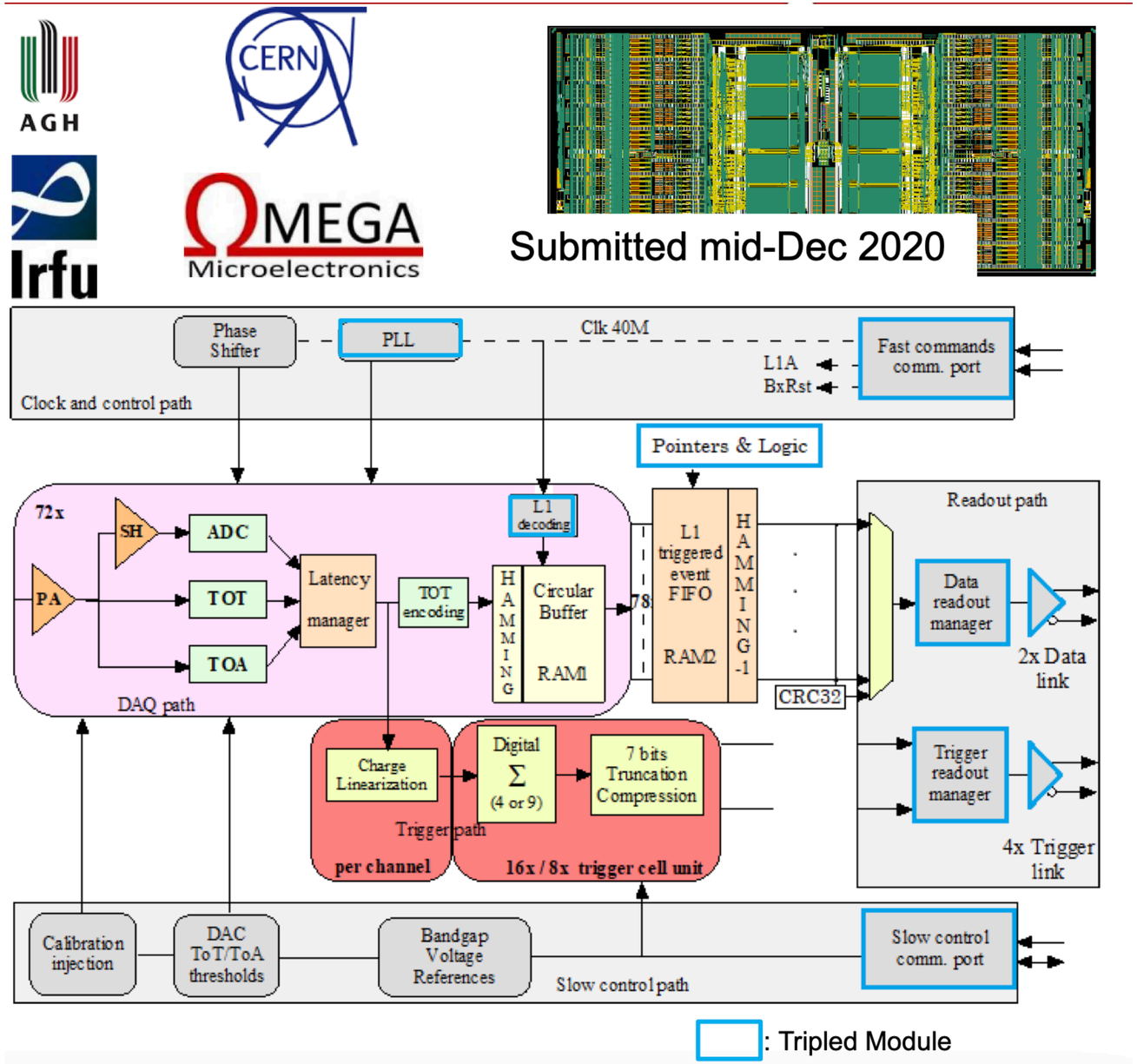
- Charge:
  - ADC peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution
  - TDC: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - Time of arrival, 10 bits (25ps)

Data flow:

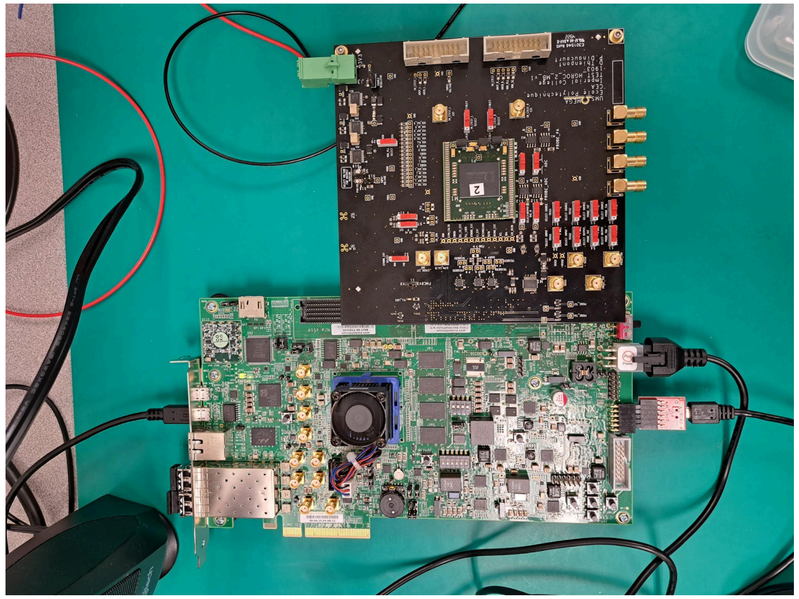
- DAQ path:
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- Trigger path:
  - Sum of 4 or 9 channels, linearization, compression to 7bits
  - 4 x 1.28 Gbps links

Control:

- Fast commands, 40MHz and 320MHz clock
- I2C for slow control

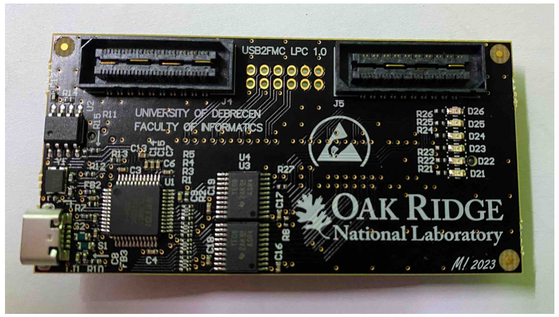


What do we have? What we produced so far



First mezzanine + carrier board designed by Omega:

- Received the chip and produced couple of mezzanines and carrier boards for testing
- Understanding the communication, setup of the chip
- We can physically solder inputs (SiPM) on channels, but this is more for single-channel testing



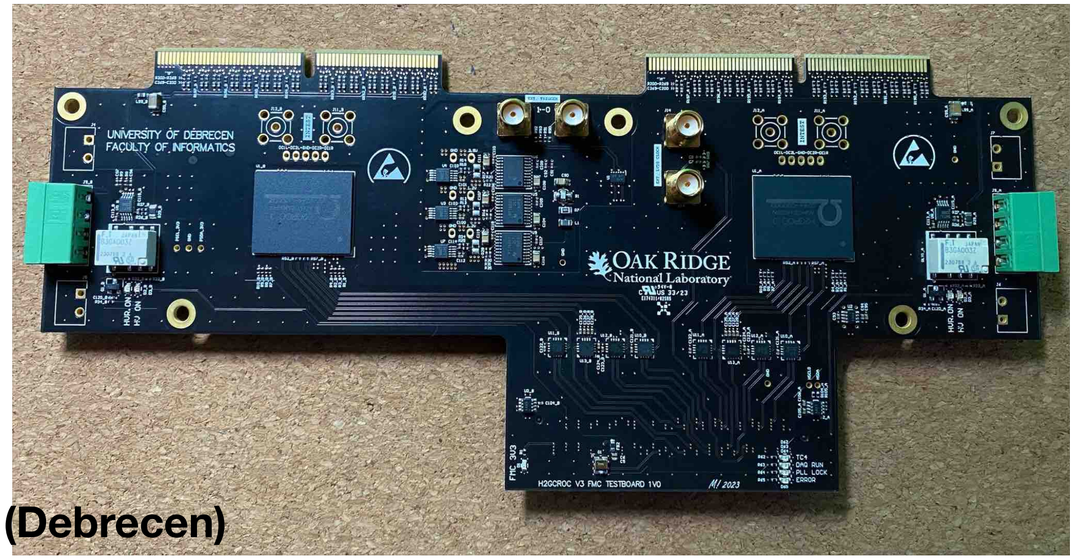
ComBoard1.0:

- USB3 readout communication
- Testing the Samtec Cables (connectors attached)

ProtoBoard1.0:

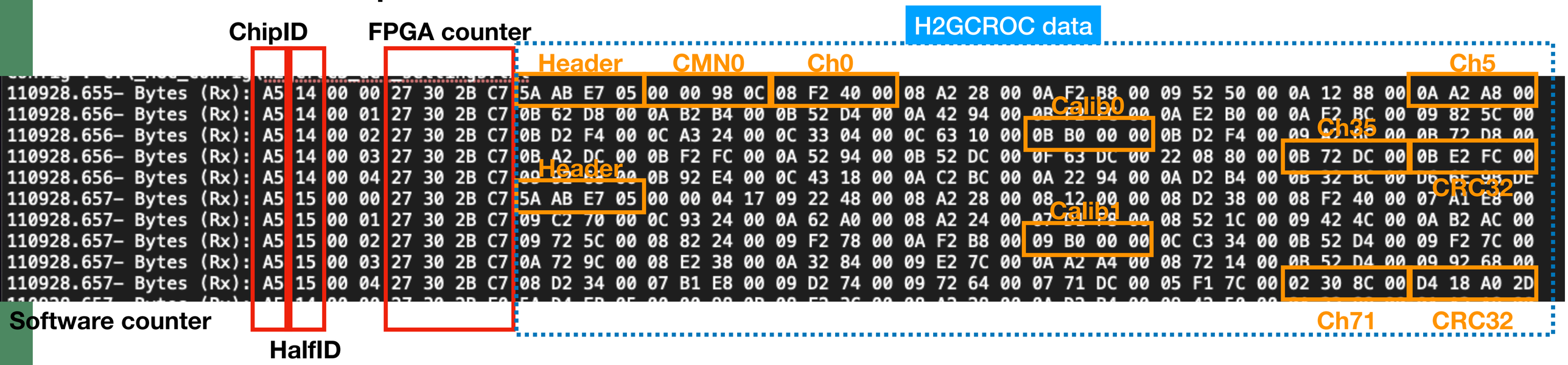
- Produced 2 of these boards so far with H2GCROC3A
- Made so it is compatible with the CAEN commercial readout
  - The upper golden pins can accept the CAEN backboards (2x)
- 64x2 = 128 channel readout - not every of the 72 channel is connected
- LVDS readout via the FMC connector
- Compatible with the KCU105 (firmware, software done):
  - Still work-in-progress, there are improvements coming as we speak

ProtoBoard1.0



Thanks a lot to Miklos Czeller and Gabor Nagy (Debrecen)

Data format explained



Ch0 `08 F2 40 00`

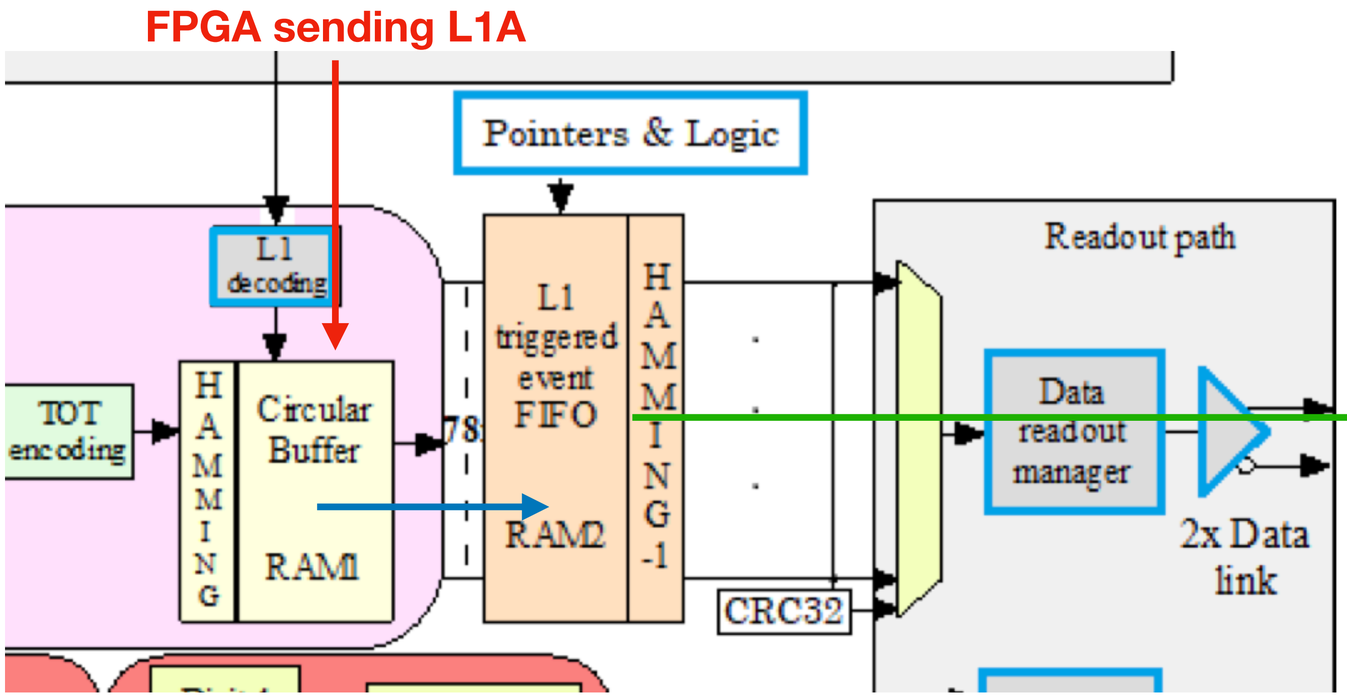
0 0 0010001111 0010010000 0000000000

Tc Tp ADC(BX-1) ADC(BX) TOA(BX)

Different data format with different charge inputs:

Tc	Tp	10-bit	10-bit	10-bit	Explanation
0	0	ADC(BX-1)	ADC(BX)	TOA(BX)	TOA and TOT threshold is not reached
0	1	ADC(BX-1)	ADC(BX)	TOA(BX)	TOA threshold reached, TOT not
1	0	ADC(BX-1)	TOT(BX)	TOA(BX)	TOT threshold reached
1	1	ADC(BX)	TOT(BX)	TOA(BX)	Characterization

One known problem quickly discovered – this is only H2GCROC3A



How we see it working:

1. **FPGA sends an L1A trigger signal**
2. **RAM1->RAM2 moving data**
3. **RAM2 trickles down the data as they come in**

Problem arrises in step 2:

- **When RAM1—>RAM2 move is done, the power can decrease**
- **If the next L1A comes quickly, then it might flip 1—>0 bit**
- **Depends on the frequency of the L1A coming in**

Problem fix:

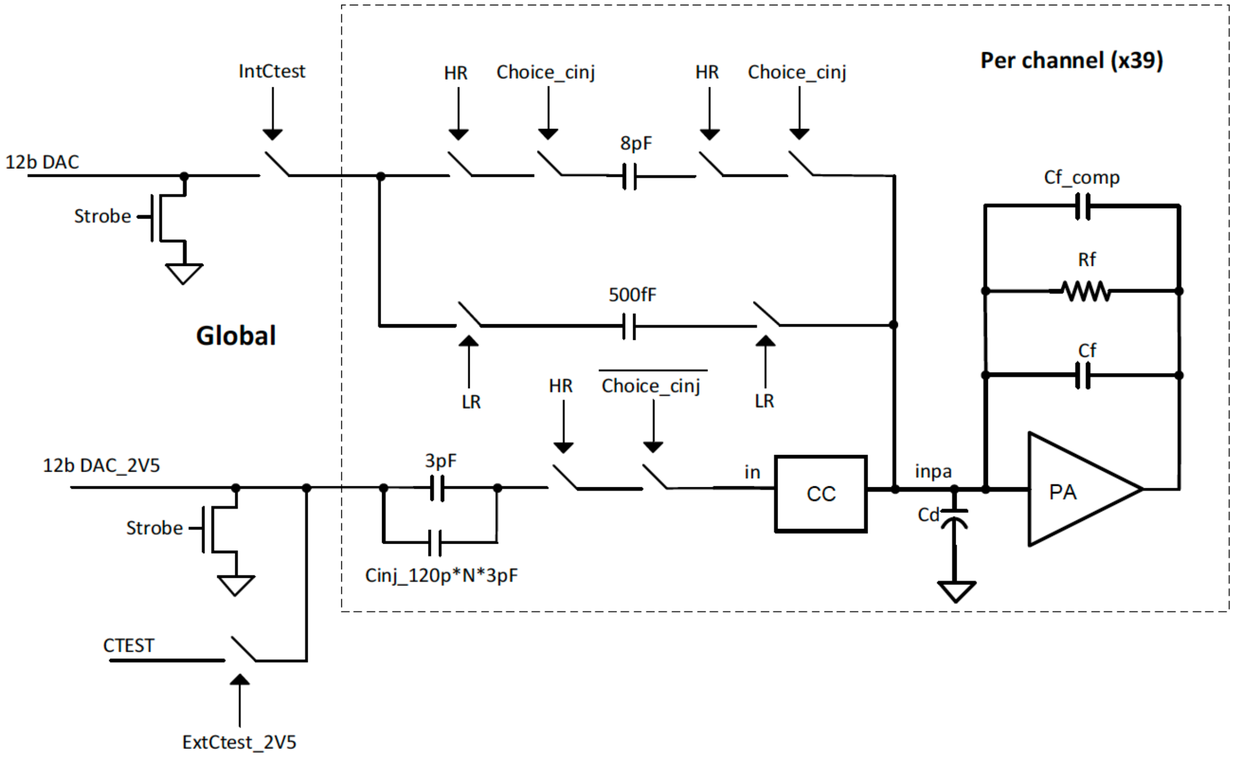
- Connect the VH10 pin to the 1.2 V
- This prevents the drop of power and corruption of the data
- Hamming code has to be ==0 in order to see no corruption

This problem is annoying, we fix it with implementation of dead time. We found 1 μs is sufficient for see no significant Hamming code errors

We connected the 1.2V and will retest

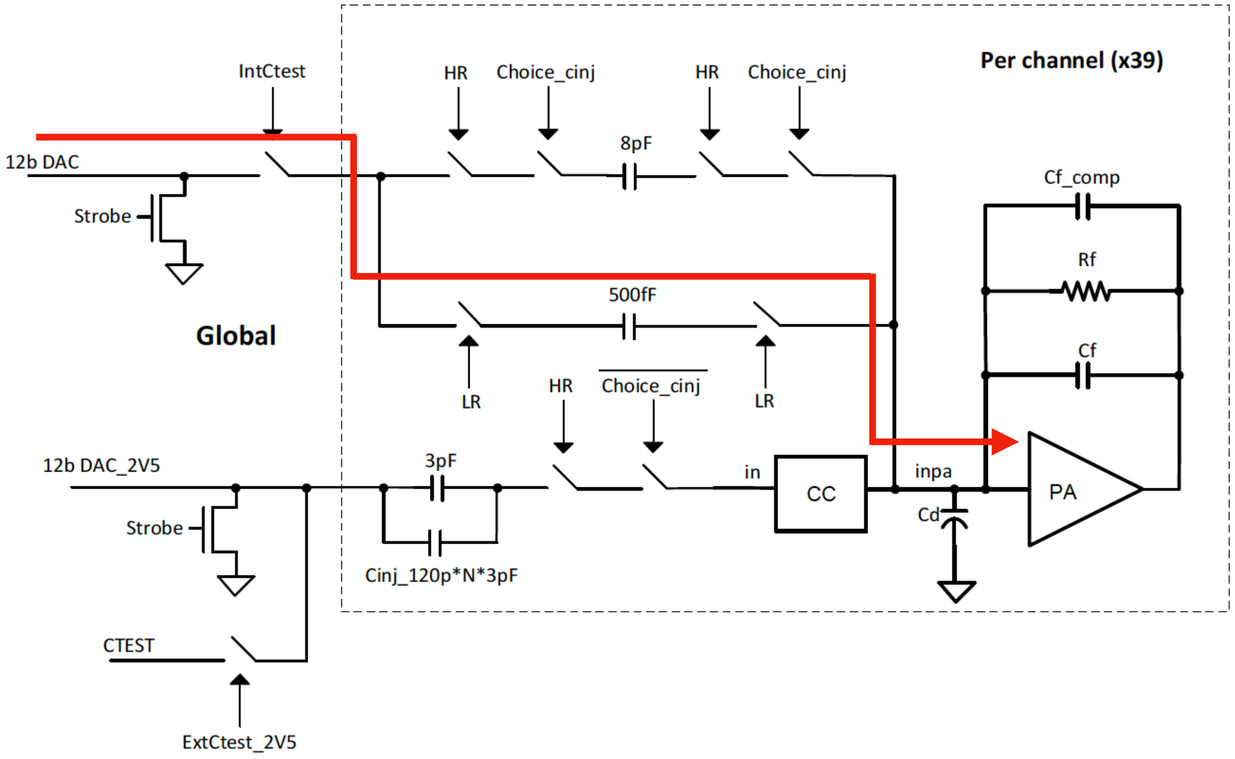
This bug is fixed in the H2GCROC3B - available in early November

Internal injection circuit



Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

Internal injection circuit



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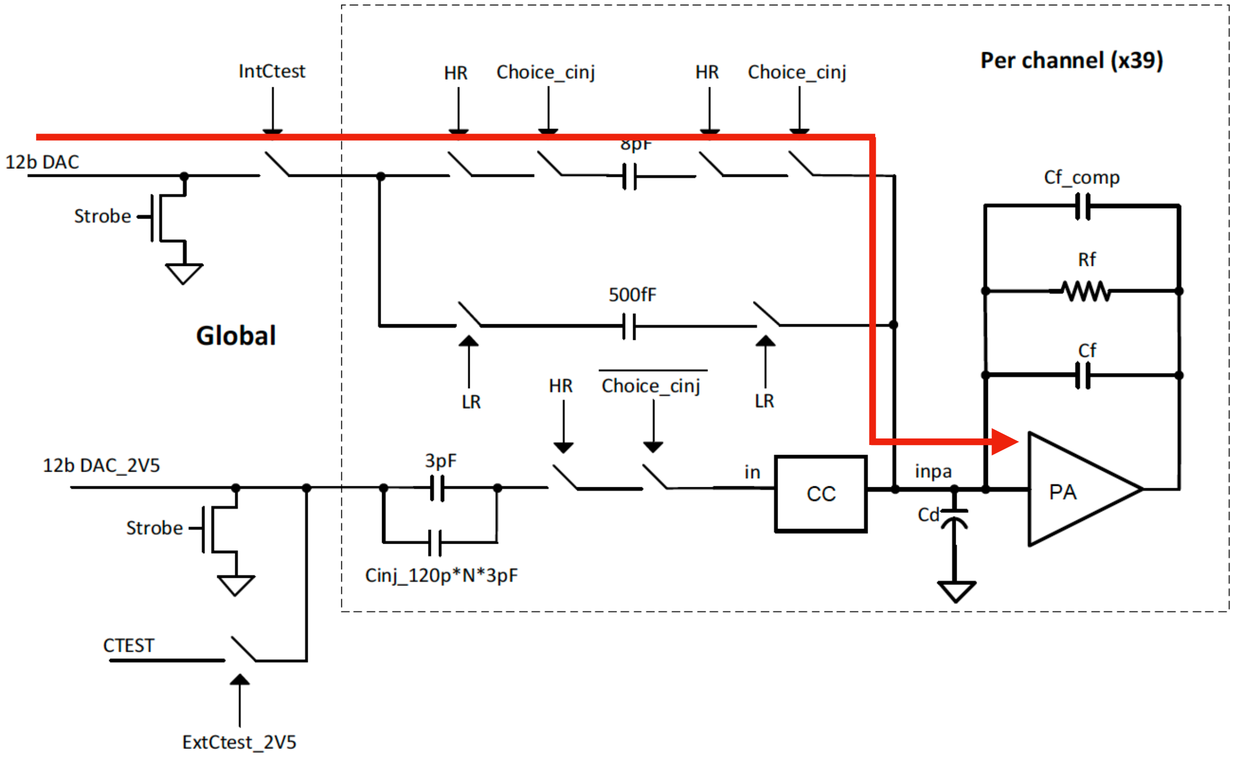
Low injection path:

- Goes through the 500fF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the ADC range in small steps
- TOA threshold setup

Internal injection circuit

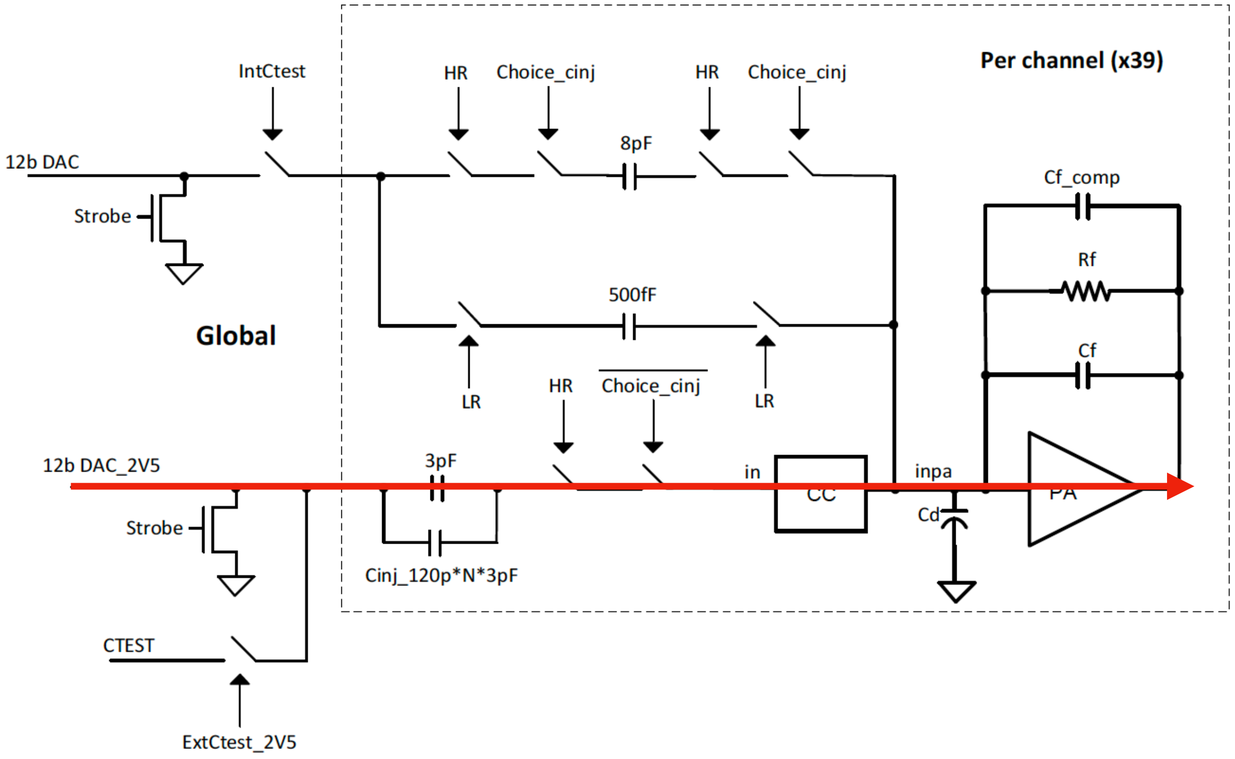


Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

High injection path:

- Goes through the 8pF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the TOT threshold
- Linearity on entire dynamic range

Internal injection circuit



Three different internal injection path:
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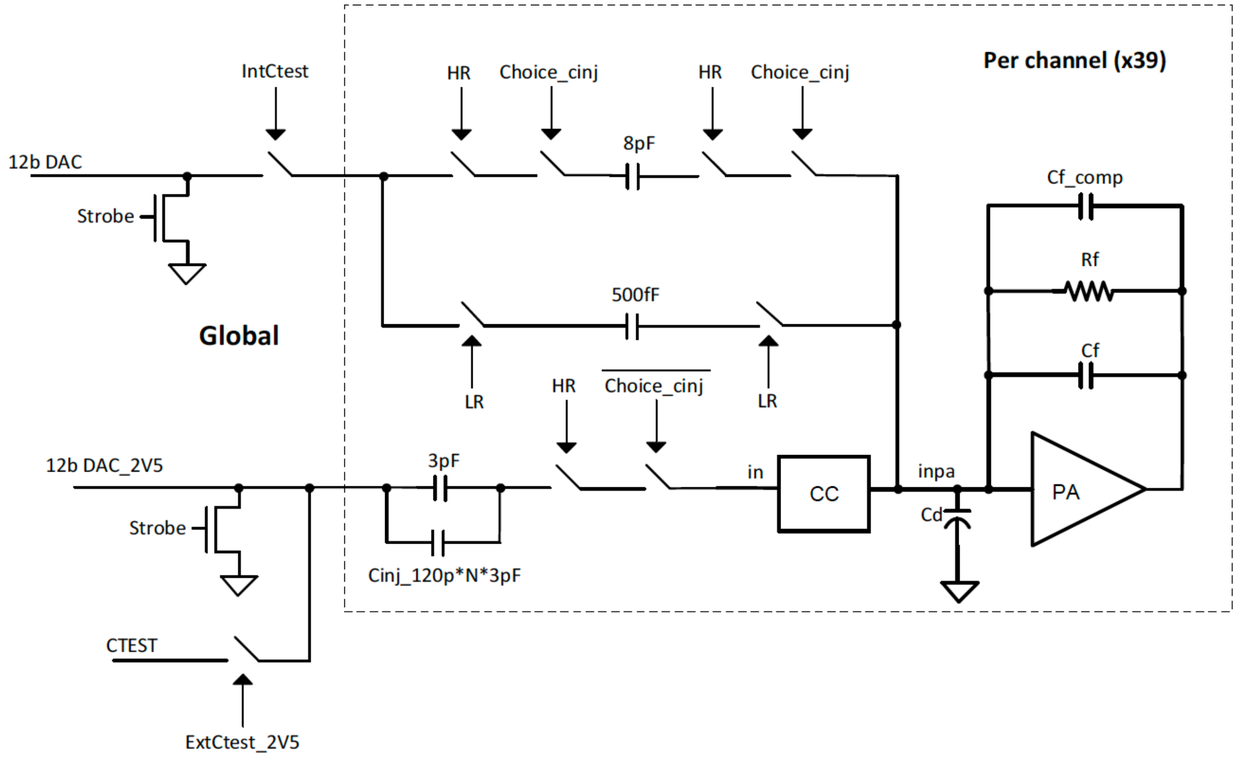
2V5 injection

- Same as an external signal (mimics the SiPM input)
- Setup the current conveyor attenuation of the signal

Internal injection circuit



The following tables show how to select the different configurations for internal/external calibration:

	DAC LR	DAC HR	CINJ 3pF	CINJ 3pF*N	CTEST 3pF	CTEST 3pF*N
HighRange	0	1	1	1	0	0
LowRange	1	0	0	0	0	0
Choice_cinj	X	1	0	0	0	0
Cinj_120p	0	0	0	1	0	1
IntCtest	1	1	0	0	0	0
ExtCtest_2V5	0	0	0	0	1	1
Calib INPA	0 - 500fC	0 - 8pC	-	-	-	-
Calib IN	-	-	0 – 3pC	0 – 3pC*N	-	-
Calib Ext Inj	-	-	-	-	CTEST * (0 – 3pC)	CTEST * (0 – 3pC*N)

This is the map of I2C registers to set each injection path

Three different internal injection path:
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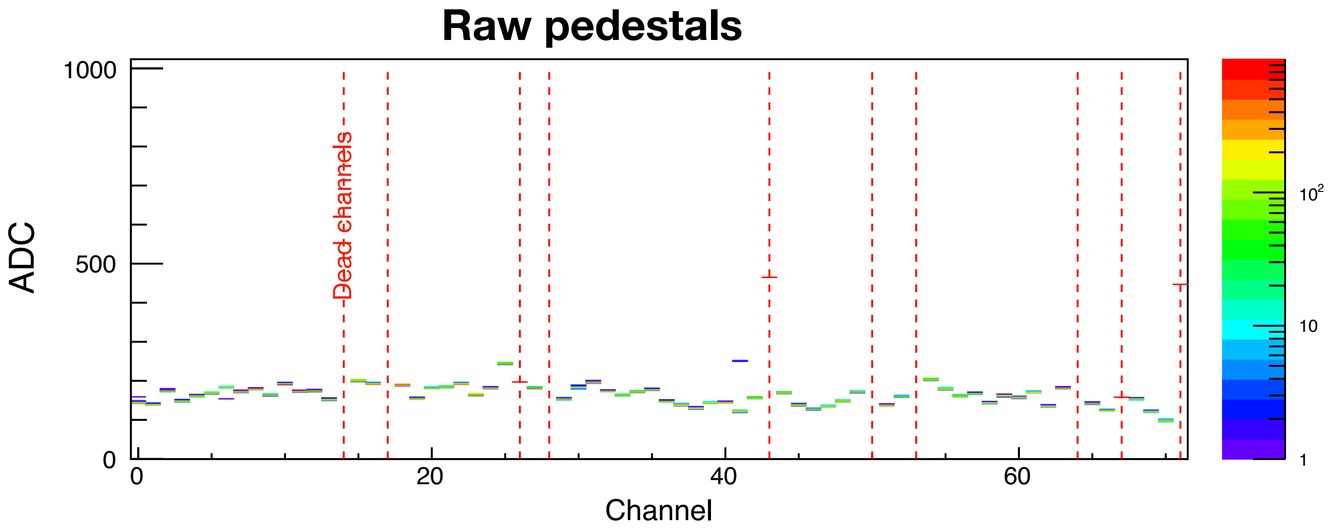
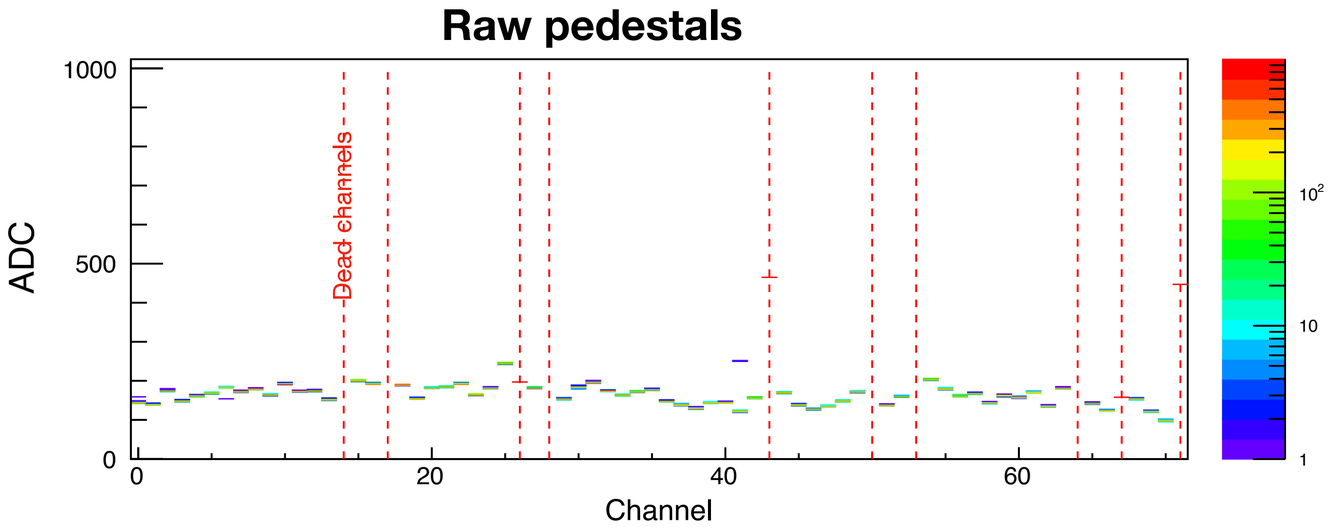
First test, pedestals



Pedestals as we turn-on the chip:

- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

First test, pedestals

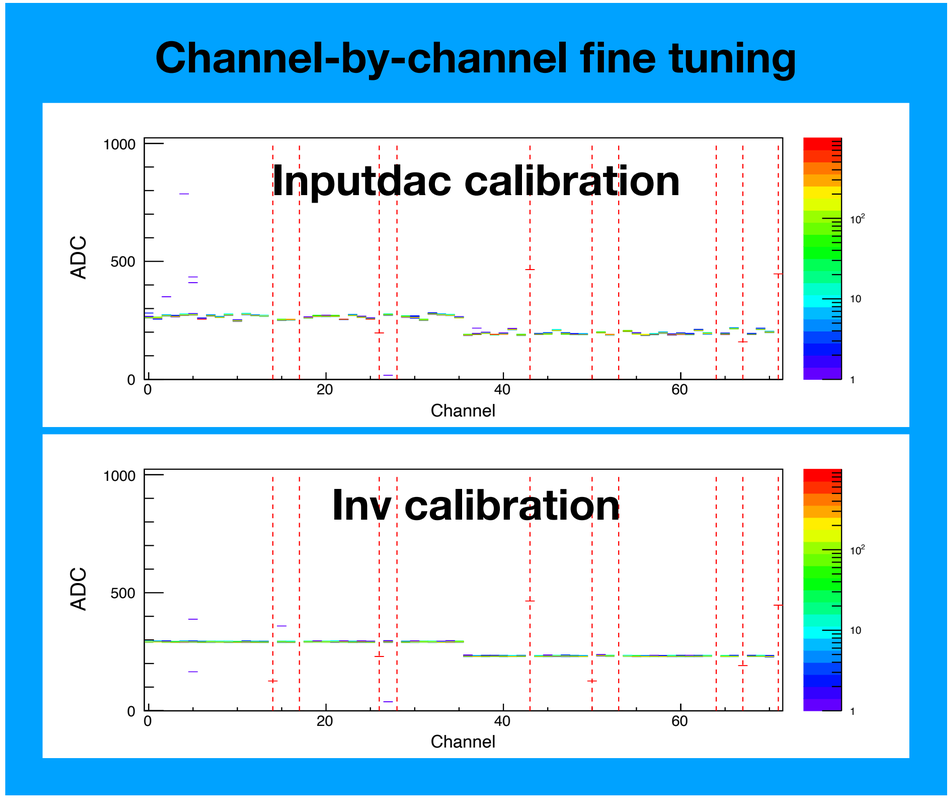


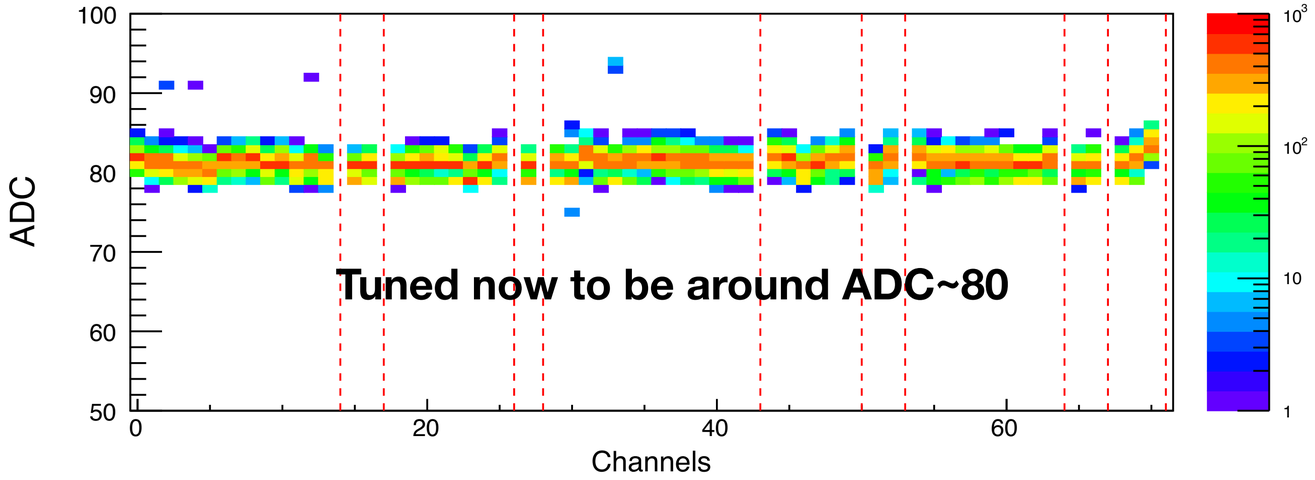
Pedestals as we turn-on the chip:

- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

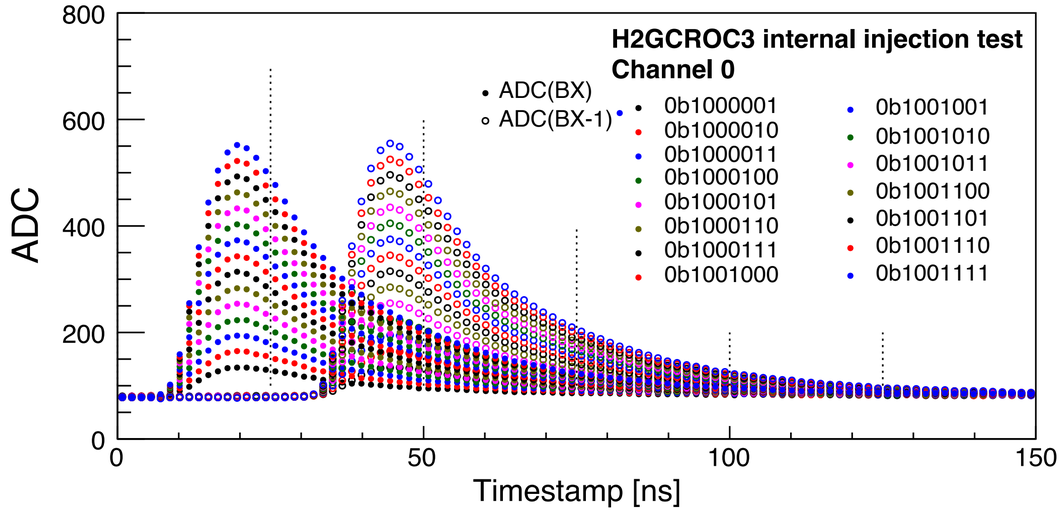
Pedestals after calibration:

- Channel-by-channel calibration is done:
  - Register_0 inputdac
  - Register_3 trim_inv
- We can set the global pedestals by half-chip:
  - Register_4 Inv_vref
  - Register_5 Noinv_vref



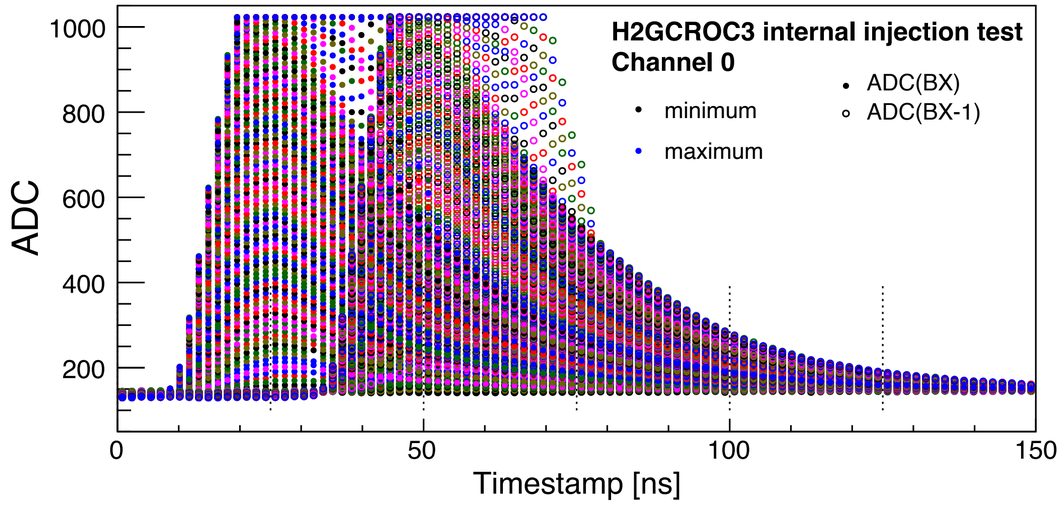


Signals!



Low injection test:

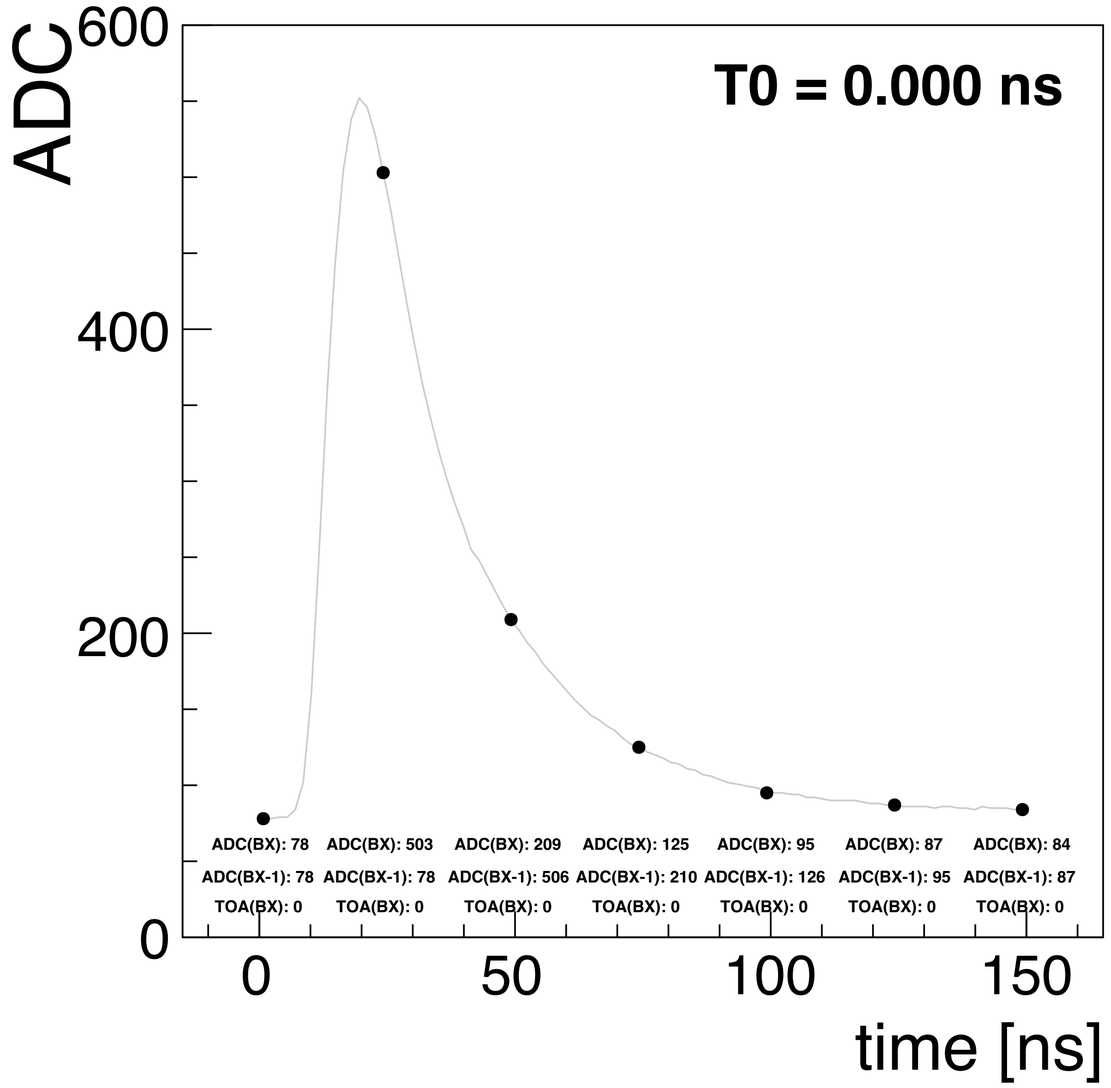
- The legend is different injections:
- 0b1001111 = low injection + “F00” = 3840 (almost maximum)
- Scanned the full shape of the signal:
  - The ADC and ADC(BX-1) is shown
- TOA and TOT purposefully turned off
- All channels were tested, in the backup



High injection test:

- TOA and TOT purposefully turned off
- Tested from lowest to higher signals
- Let the ADC saturate
- Shape is very consistent, does not change with the height

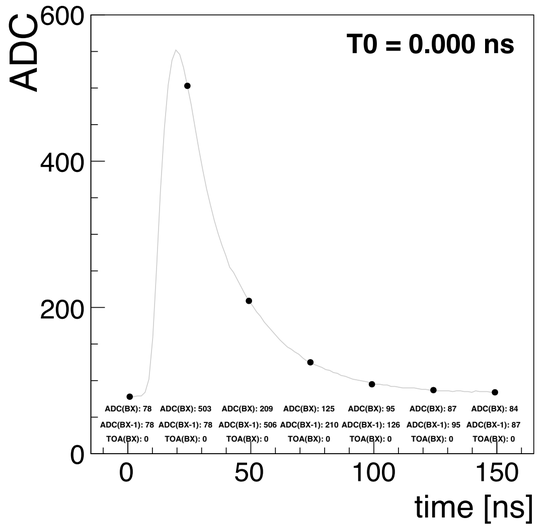
How it would look in ePIC

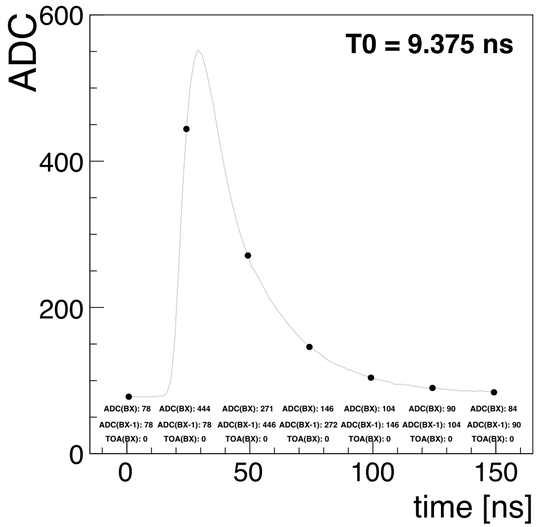


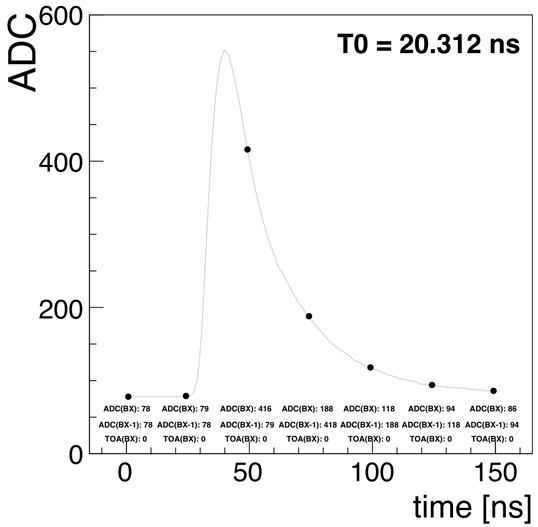
What we will see in the signal with the 25ns sampling:

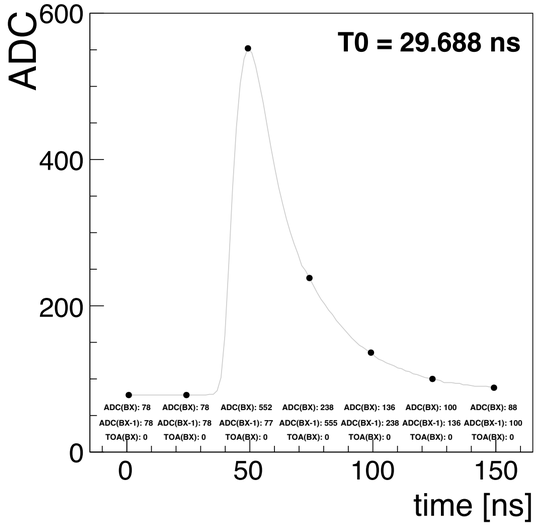
- This is real data, using the real shaper extracted from the ROC
- Each run was 5000 events:
  - Caveat = each point now is independent run
    - VHI10 problem, see slide 5
  - Then the ADC(BX), ADC(BX-1), TOA… etc means are extracted from 5000 measurements
  - This may result that the ADC(BX-1) != ADC(BX) - 25ns
- T0 = when the particle signal happened:
  - In EIC we expect ~10ns incident periods

How it would look in ePIC









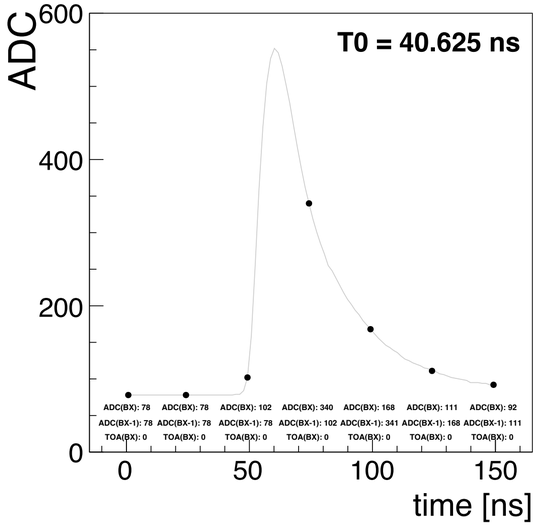


Illustration with real data:

- Each signal is shifted by about 10ns
- The points represent the samples we will obtain
- Numbers below the points show exactly the measurement

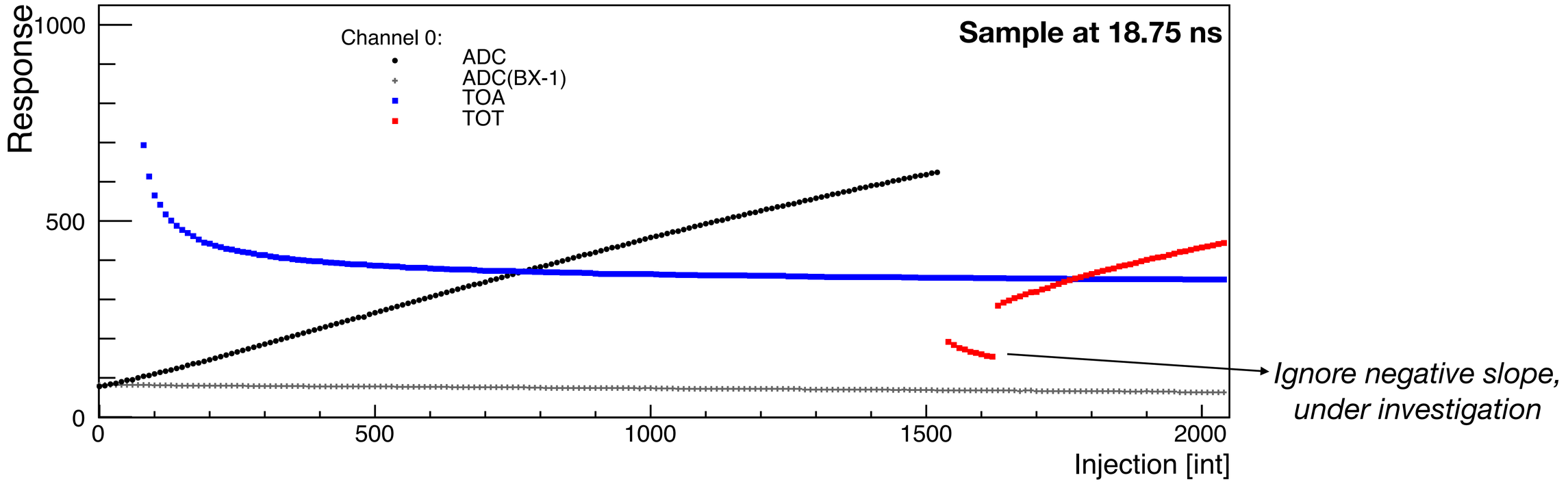
Reminder:
ADC(BX-1) != ADC(BX)-25ns,
because how the data is obtained

TOA and TOT calibration

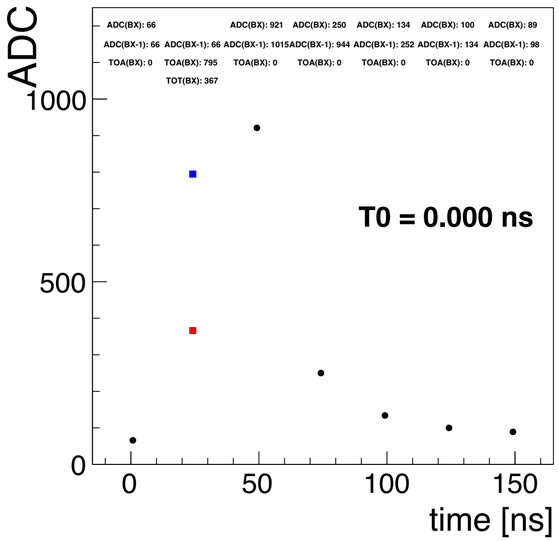
This is done with one fixed time for now (one sample from the whole shape)
Went through the lengthy calibration procedure for TOA and TOT:

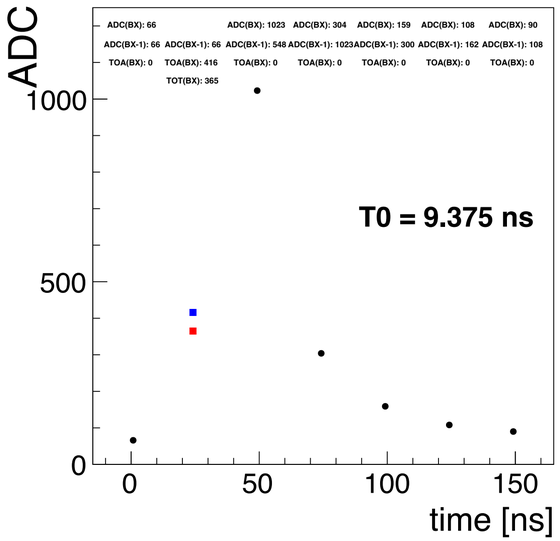
1. Set TOA global thresholds (for each side of the chip)
2. Set fixed injection large enough to pass TOA threshold
3. Scan channel-by-channel the TOA thresholds (5-bit 0..31)
4. Set channel-by-channel TOA for each channel, scan for two chip-halves
5. Set the global threshold so each half of the chip respond the same

… repeat again for TOT with larger injection, so it passes the desired TOT threshold



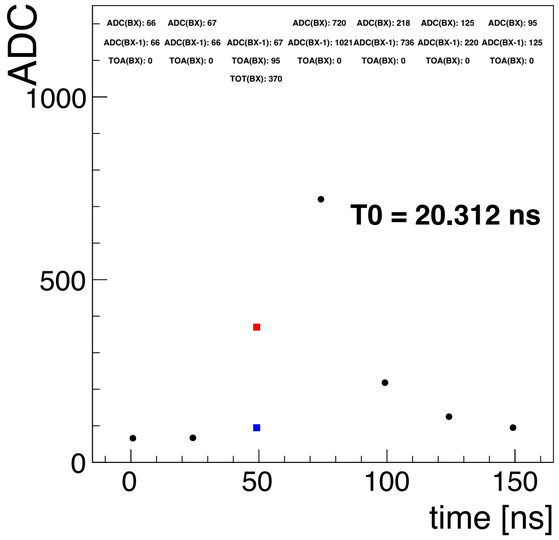
Sampling when reaching TOA/TOT

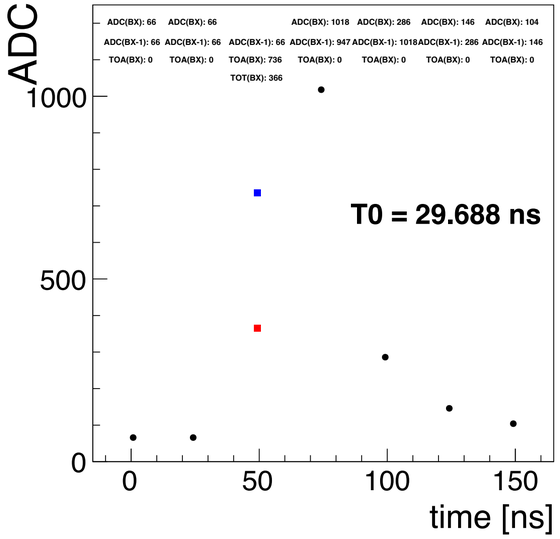


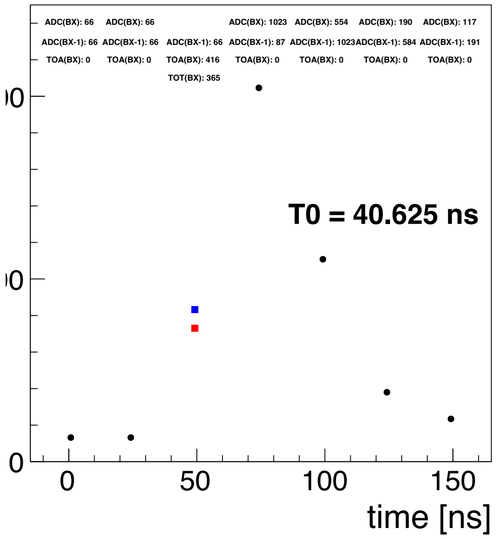


Same signal in different phases:

- TOA is changing - giving a clue in which phase we are
- TOT is constant
- Note the change of the data structure when the TOT is reached





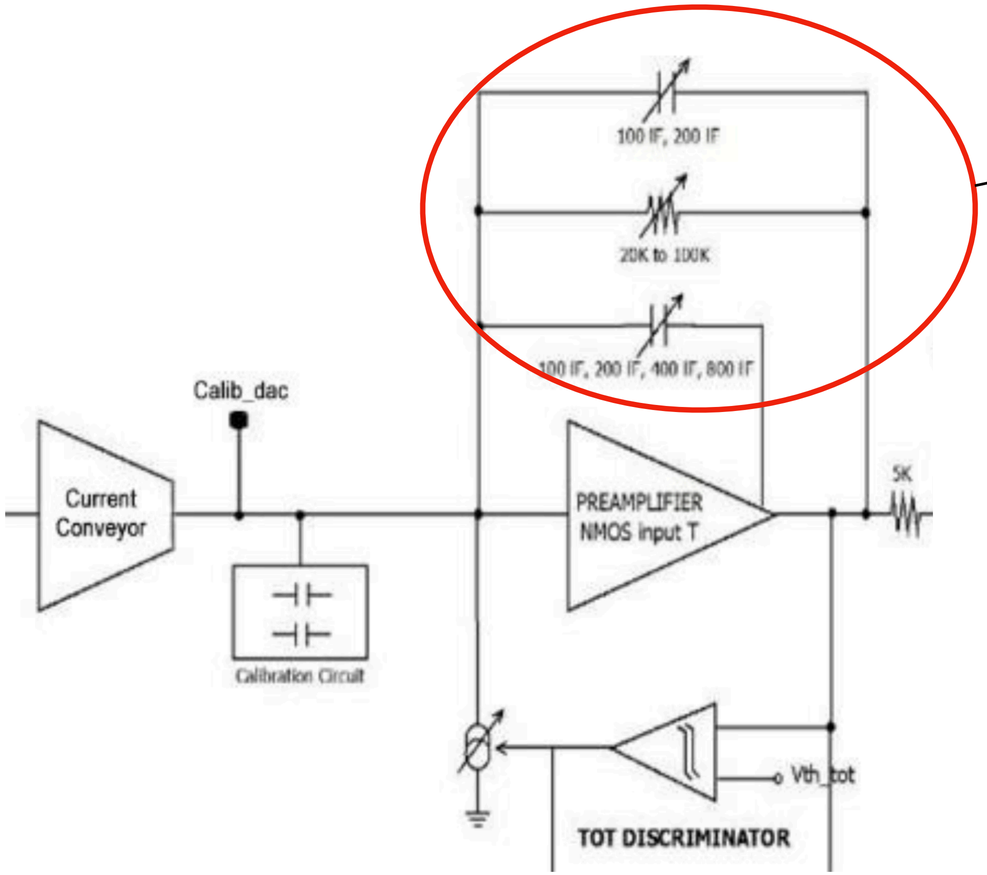


Using the TOT/ADC slope calibration, one can easily calculate the ADC_equivalent (as ADC is saturated) value

$$ADC_{\mathrm{eq}} = f_{\mathrm{adc}}\left[f_{\mathrm{tot}}^{-1}(TOT)\right]$$

$$ADC_{\mathrm{eq}} \sim 15\mathrm{bit\ value}$$

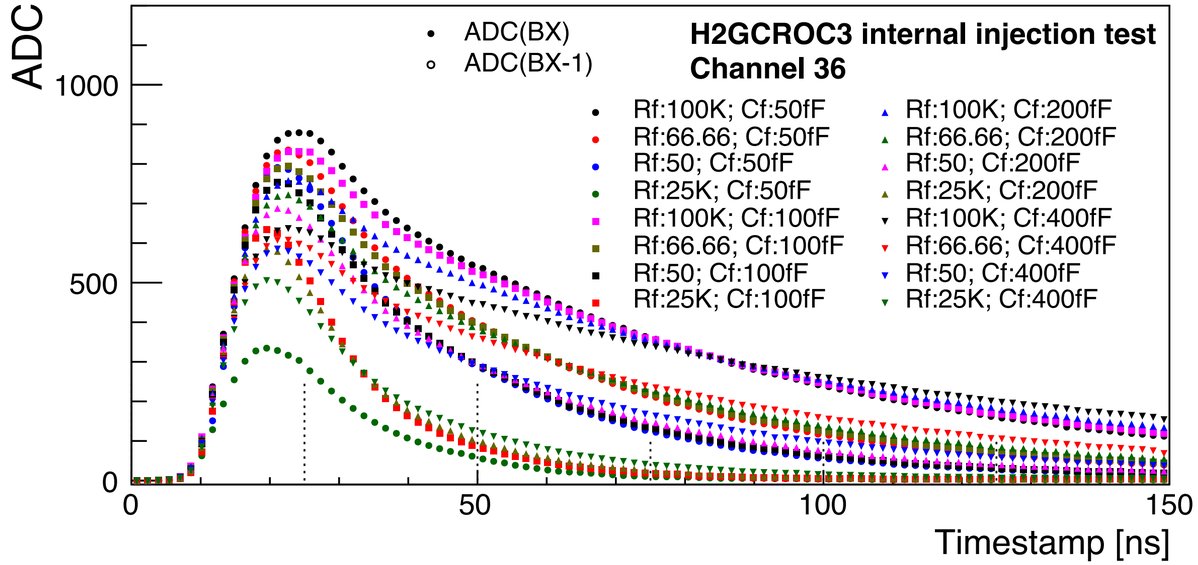
Gain checks



Cd (pF)	5, 10, 20	At the conveyor output and at the preamp input. To ensure the preamp stability.
Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50, 100, 200, 400	Same purpose than Cf capacitors but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table 1.1: Values for Rf, Cf and Cd

Same injection in the same channel

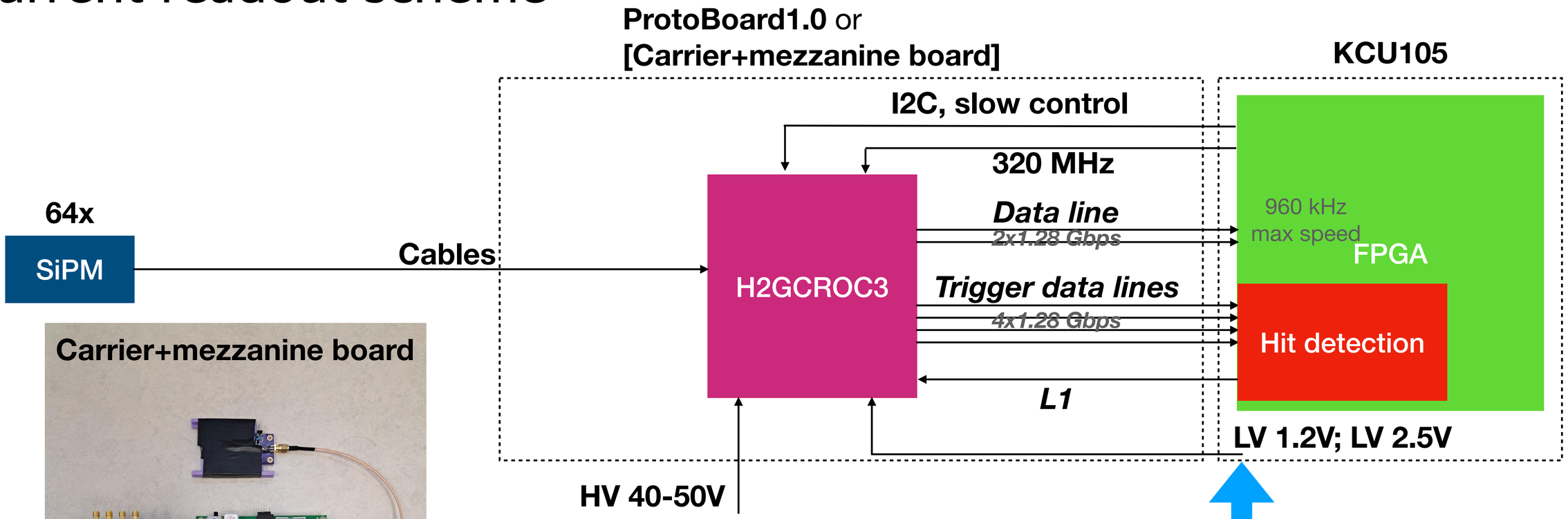


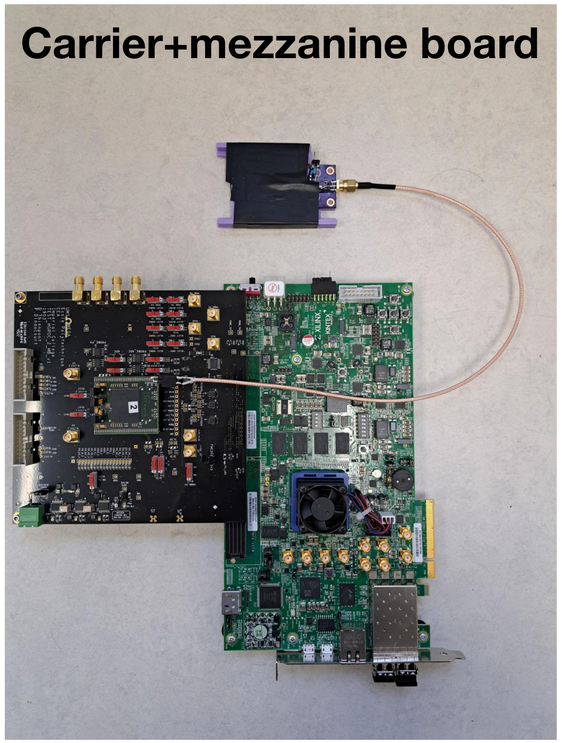
Pre-amp gains can be changed in the ASIC anytime, built-in setup can be further tuned to our needs (EIC)

With the quick test, 16 different gains were explored:

- Dynamic range can change a factor of 3!
- More setups can be added

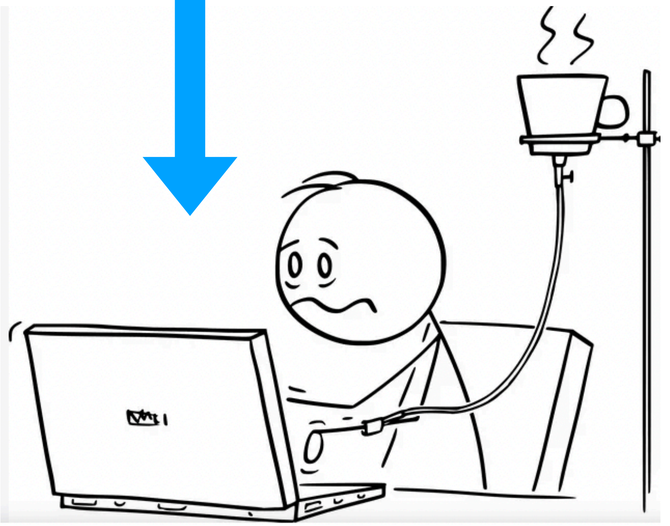
Current readout scheme



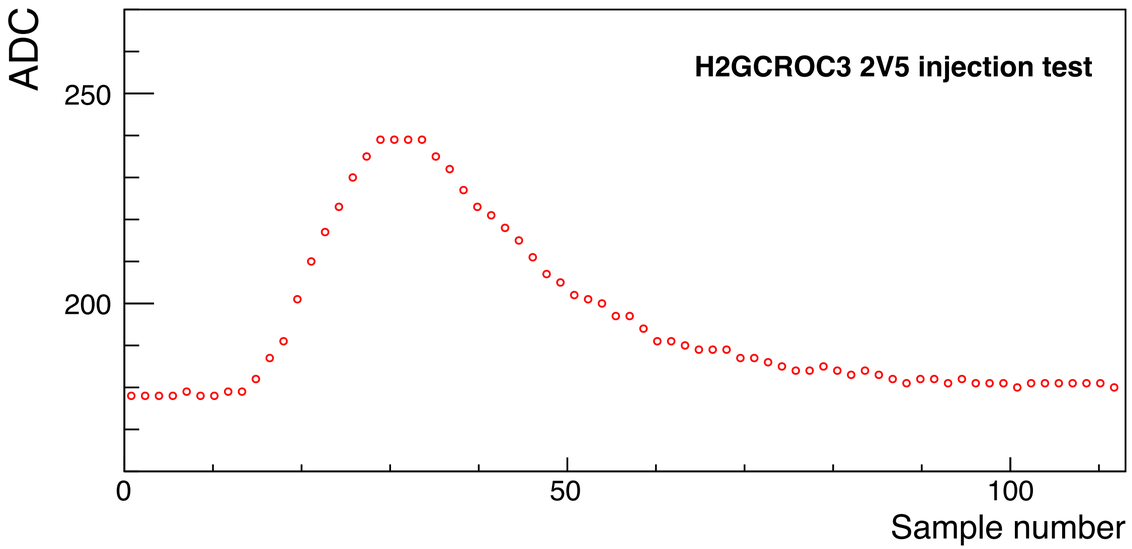


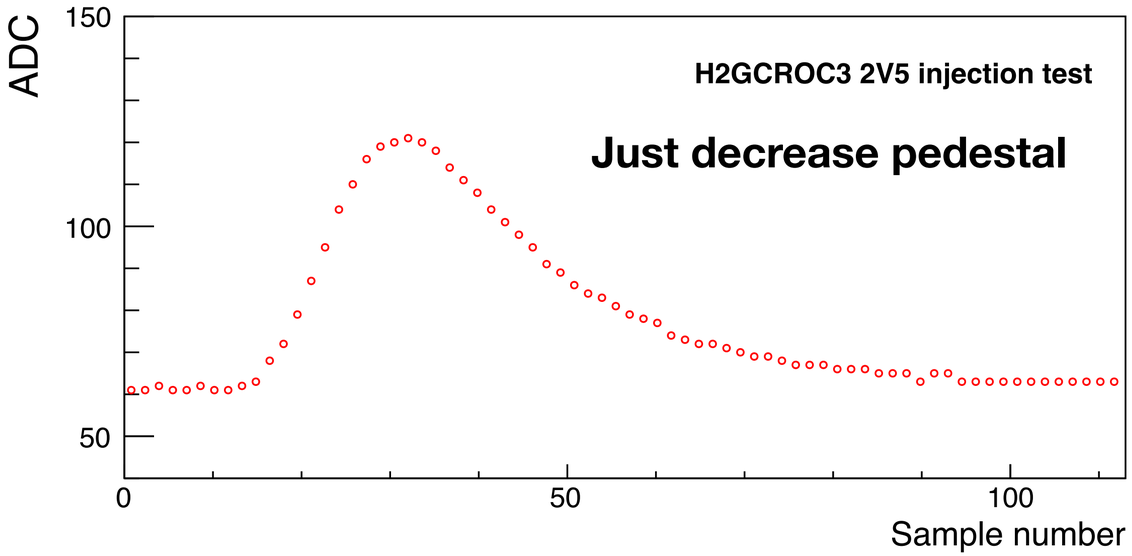
The firmware, software is set:

- Self triggering mode - we can decode the information in KCU and send a trigger signal (for now 1 usec dead-time is set)
- External triggering - any 1.8V signal can be accepted as trigger input



First results from 2.5 V injection test, plus external injection



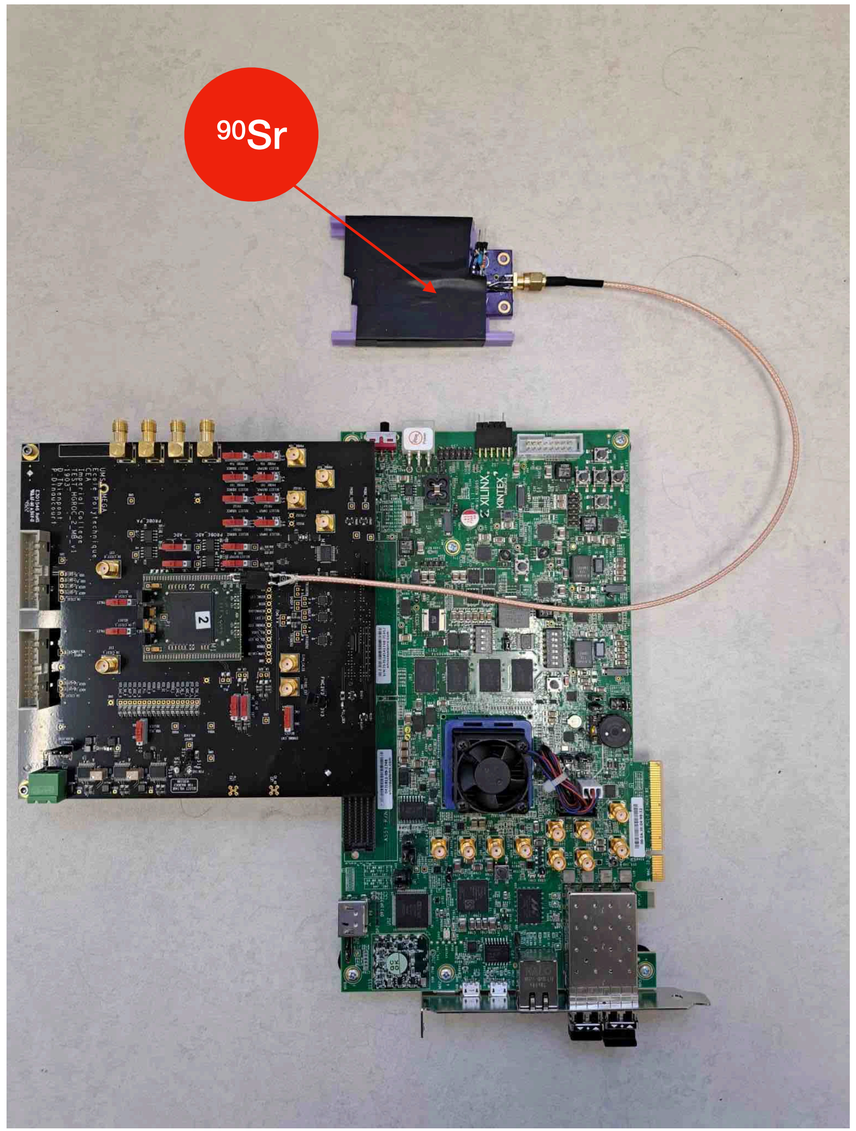


This is directly injecting to the input of the channel:

- Had some initial troubles to see the 2.5V injection, but after clearing up with Lida Kalipoliti from CMS, we got it right
- This is important step to connect the SiPM in the input:
  - Making sure all the pre-amps work: Low and High injection
  - Making sure the current conveyer is set properly: 2.5 V injection

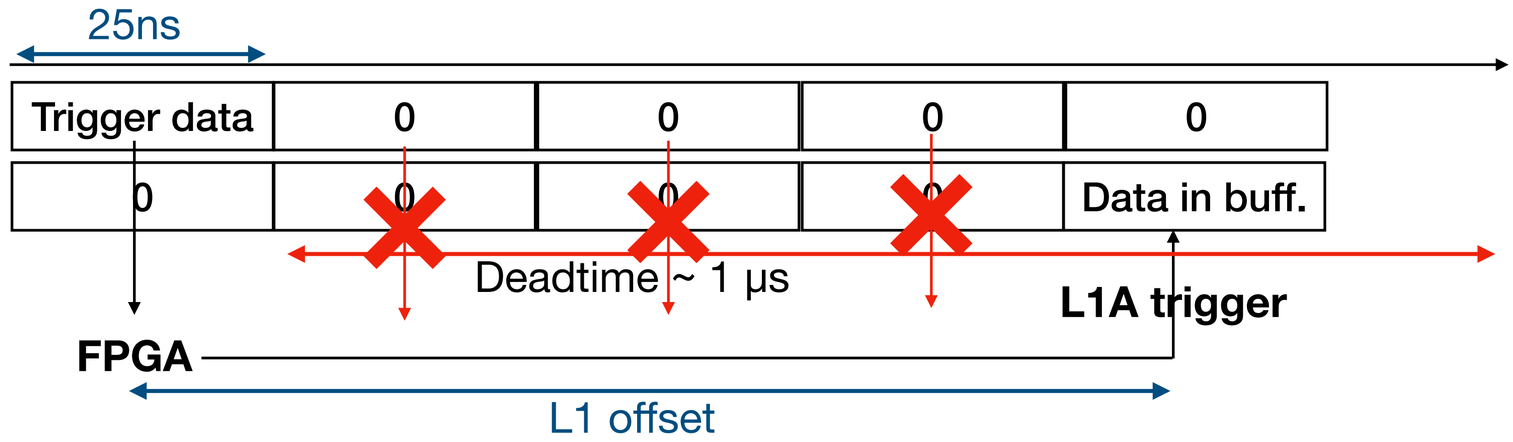
Finally seeing some data coming through the whole input

^{90}Sr source test

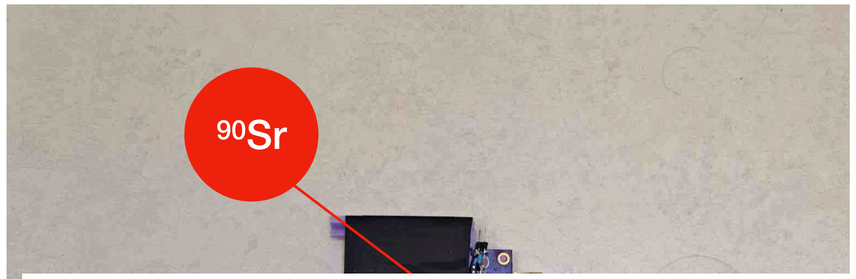


Self triggering test:

- We put the source directly on the 5x5 cm^2 scintillator
- External triggering is not possible, we utilize the self-triggering mode:
  - First 4 channels are summed up in the trigger line 0
  - Pedestals are loaded to the I2C of the chip
  - Compare the outgoing trigger data to a threshold:
    - If threshold is reached—> send the L1A trigger
    - The L1Offset sets how many clock cycles we wait

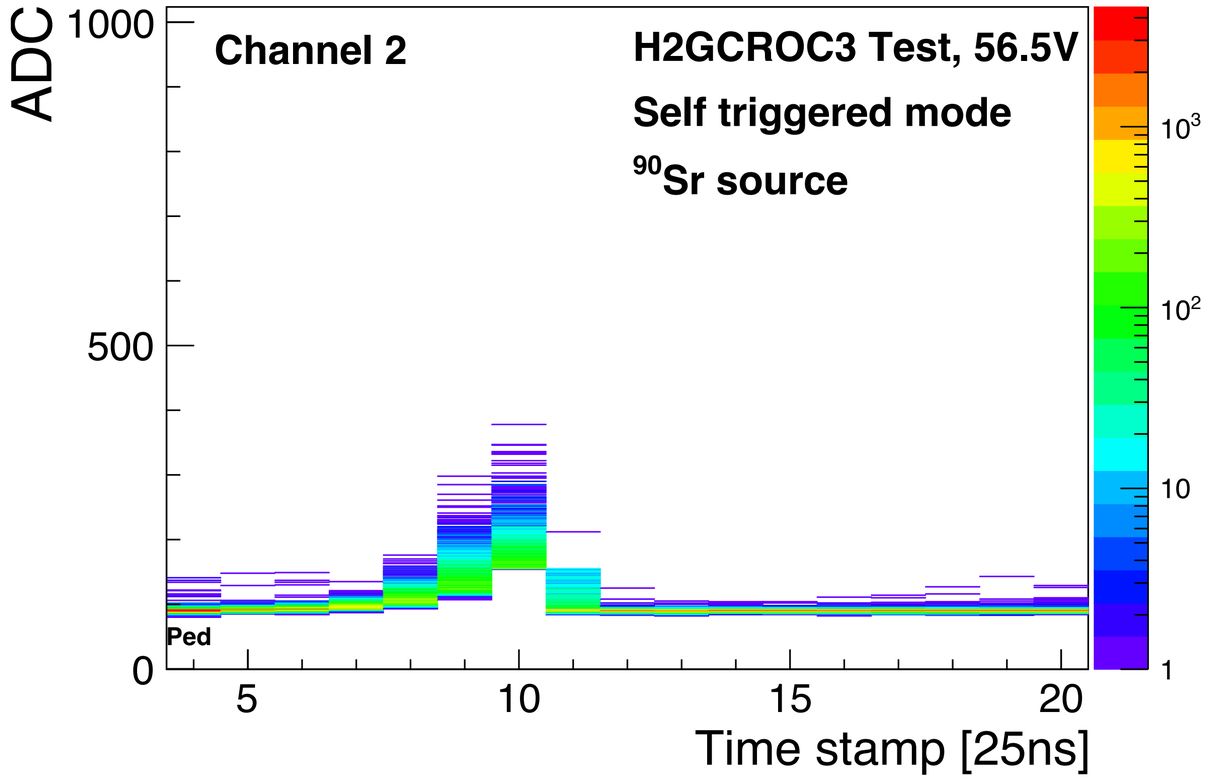


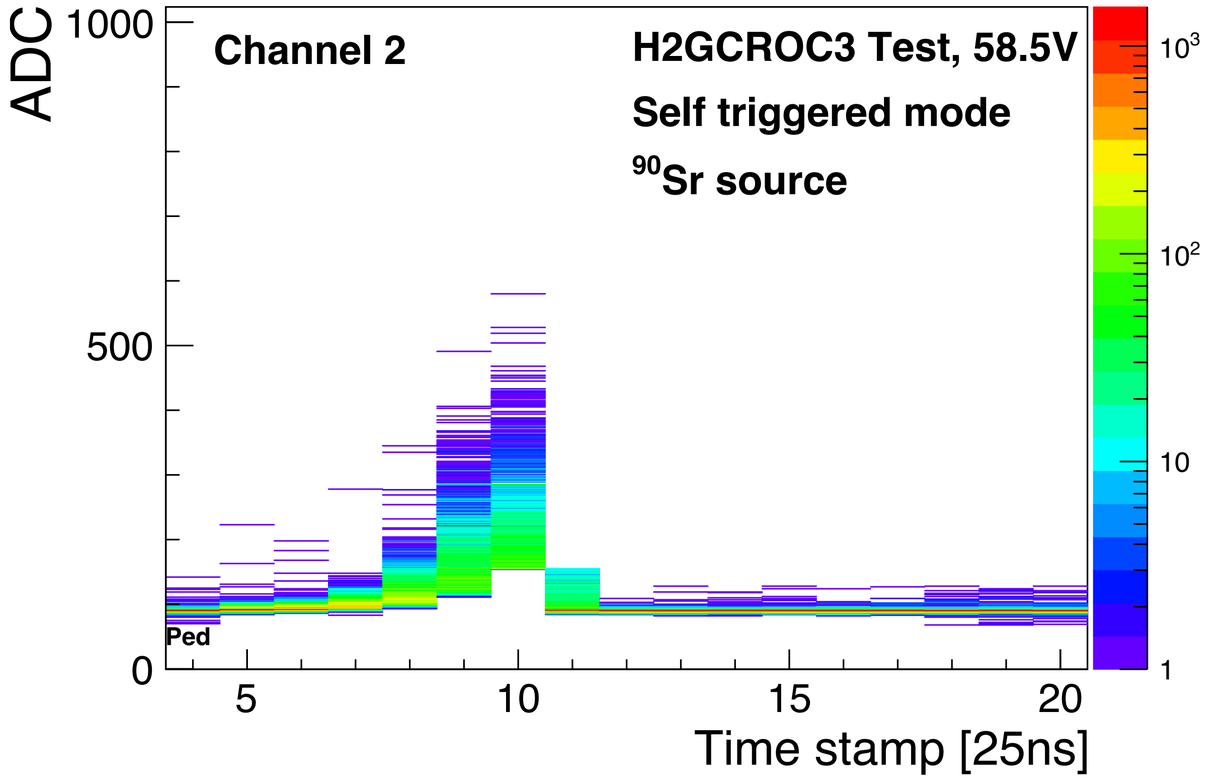
^{90}Sr source test



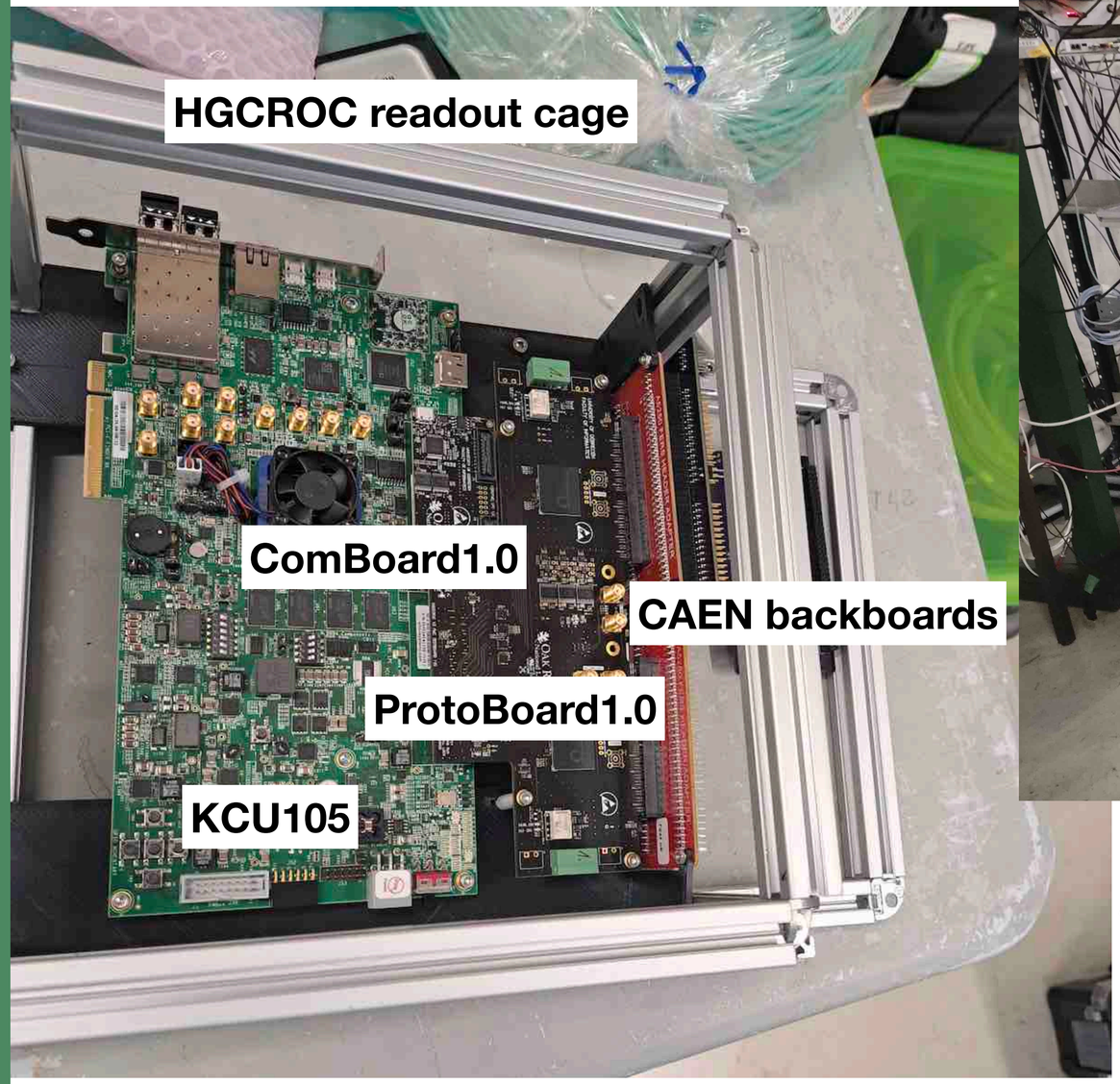
Self triggering test:

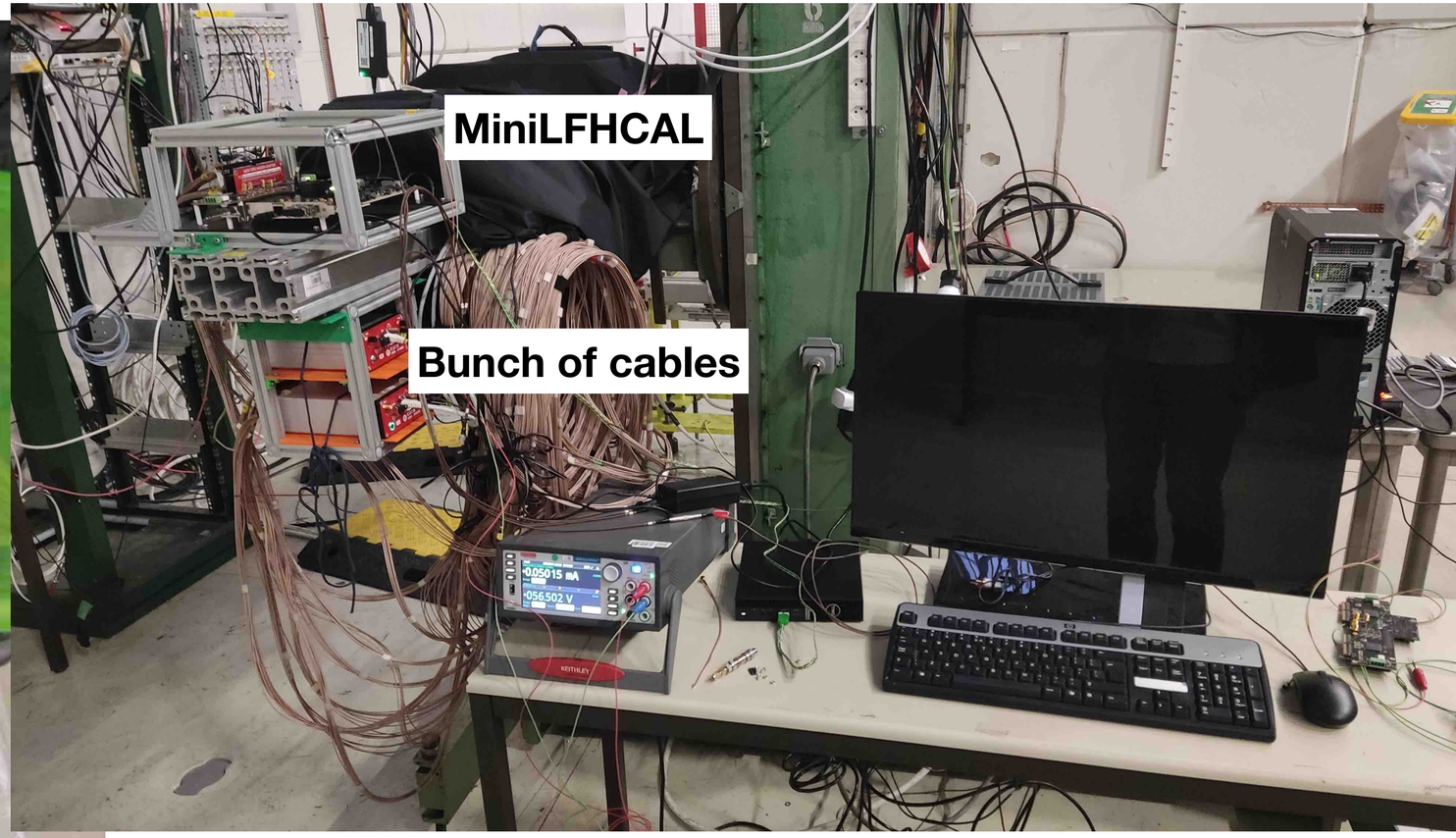
- We put the source directly on the 5x5 cm^2 scintillator
- External triggering is not possible, we utilize the self-triggering mode:
  - First 4 channels are summed up in the trigger line 0
  - Pedestals are loaded to the I2C of the chip
  - Compare the outgoing trigger data to a threshold:
  - If threshold is reached -> send the L1A trigger





Testbeam setup



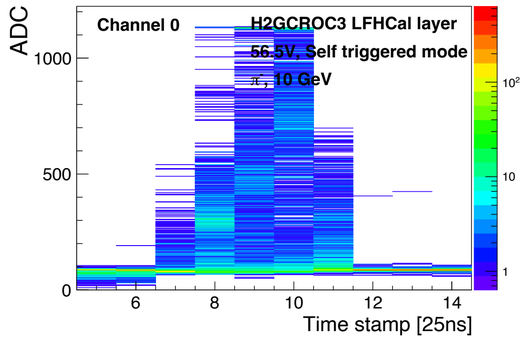


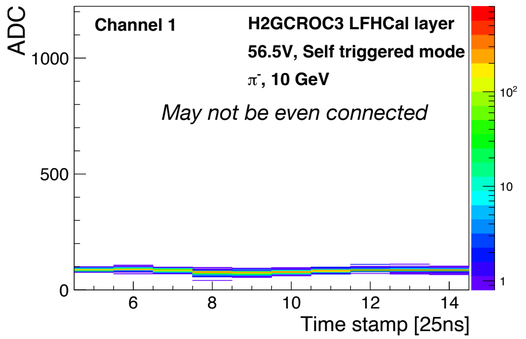
After a lot of debugging and searching for signal, we moved for a testbeam at PS with the MiniLFHCal

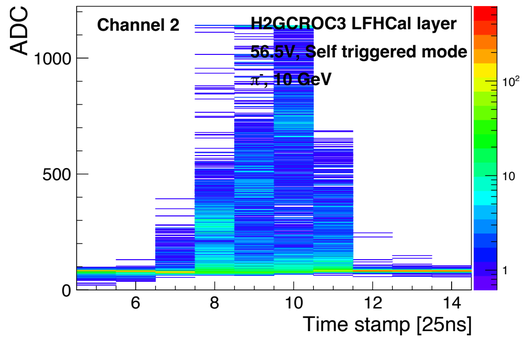
Testbeam results

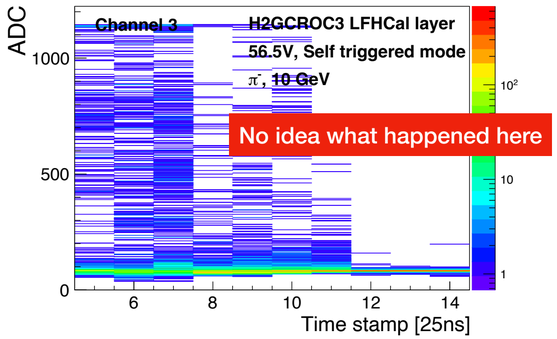
We first tried to see the signal:

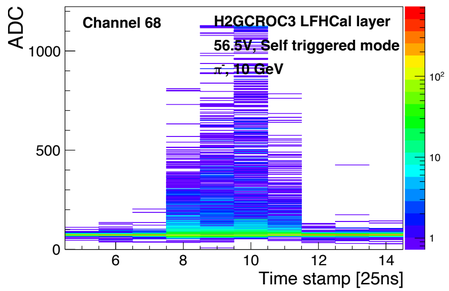
- Self triggering (the sum of first 4 channels for simplicity)
- Vary the L1offset to search for response

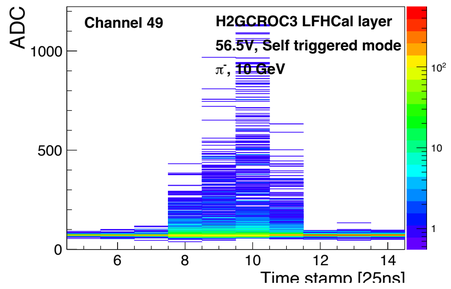


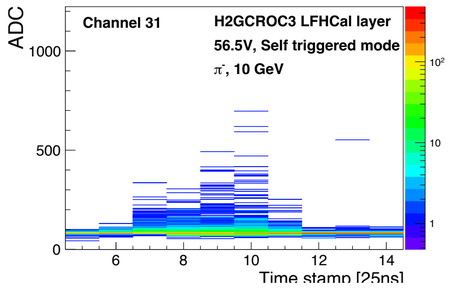


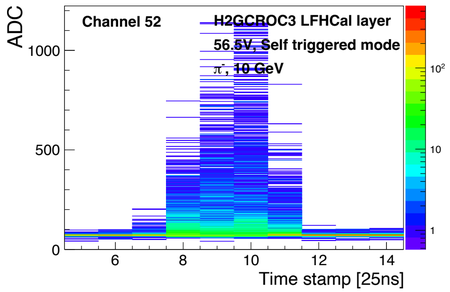


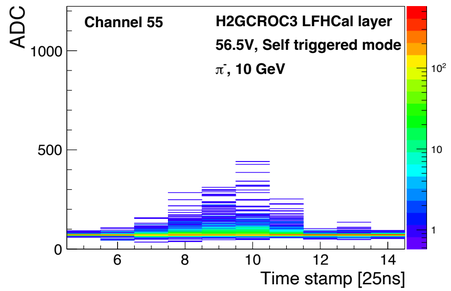


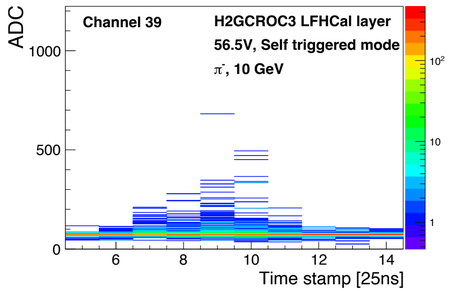








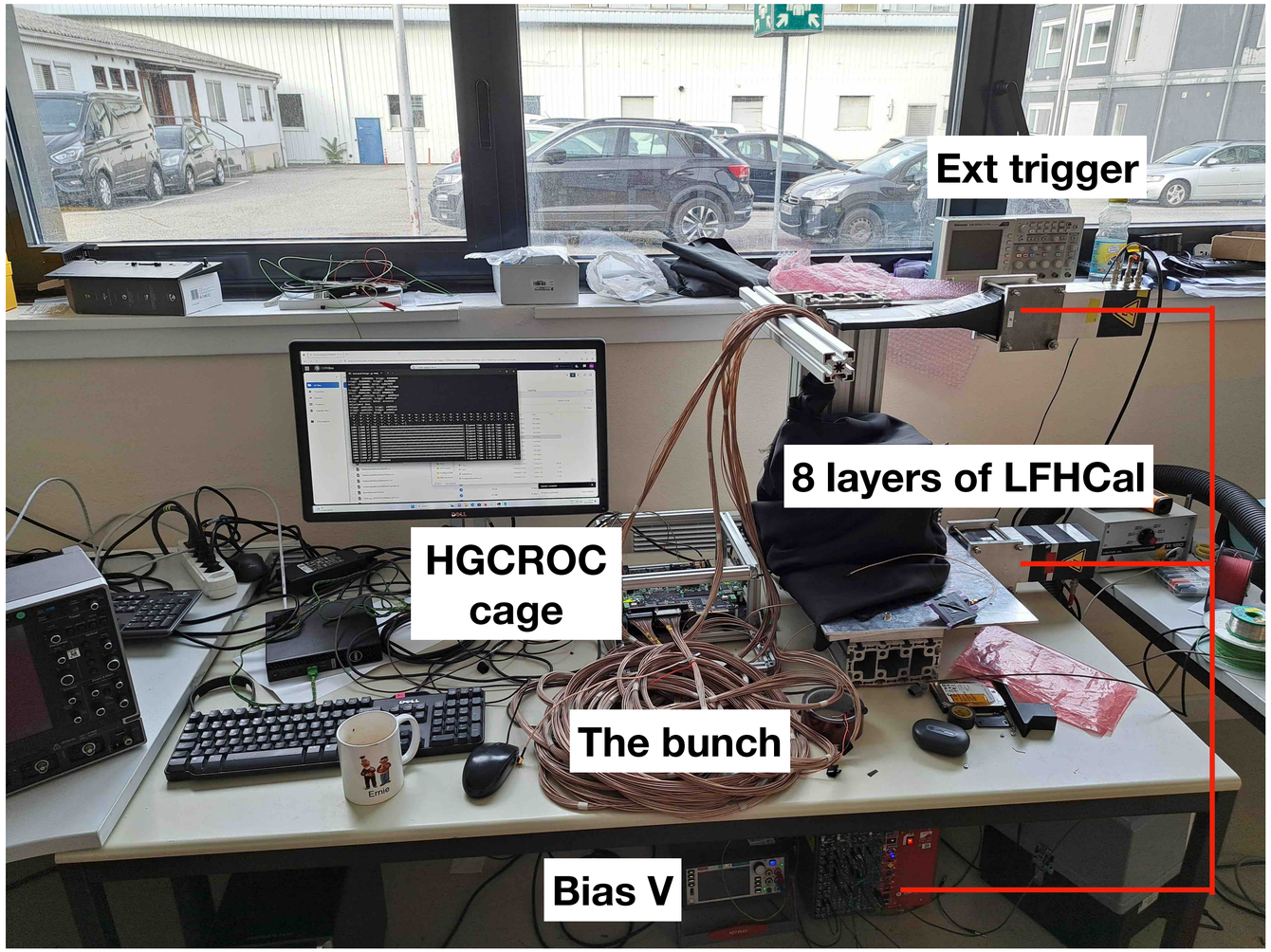




In all 40 channels responded some quite visible, some medium, some small

Unfortunately, then Linac got broken for the night and they could not restore the beam until we had to move out

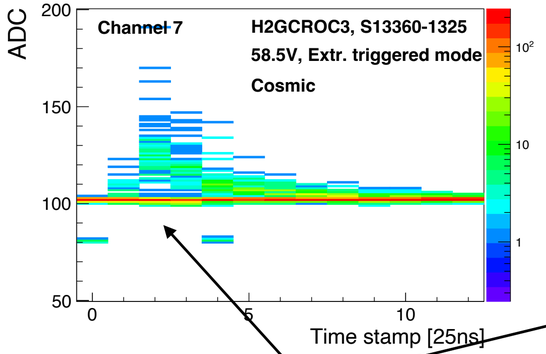
Not yet the end!



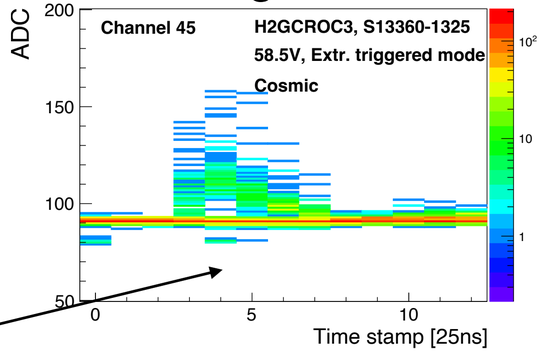
Never-give-up cosmic setup:

- Quickly done after the testbeam setup was removed
- 10x10cm^2 scintillator for external trigger
  - This is different, dropped the self triggering now

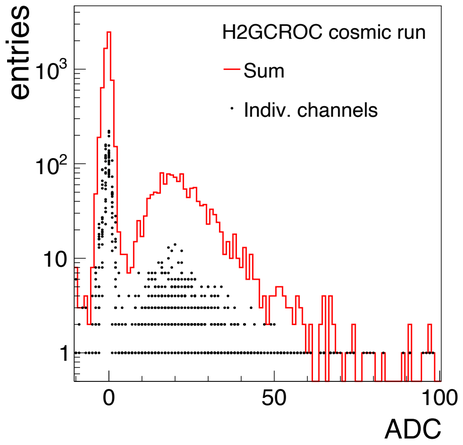
Shorter cable



Longer cable



Check the max for responding channels

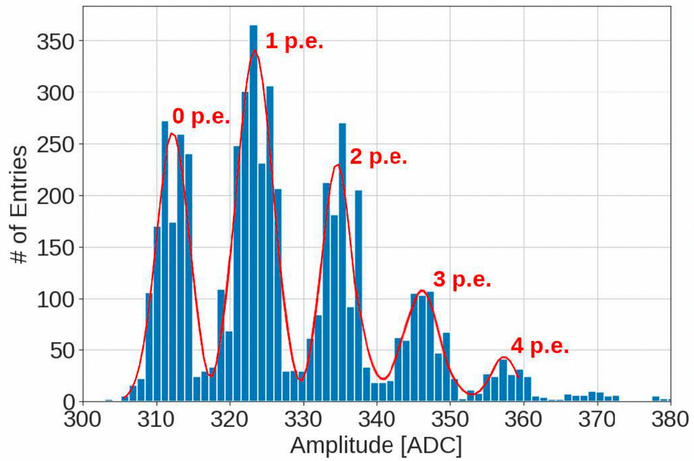


We see the MIP peak from the cosmic runs

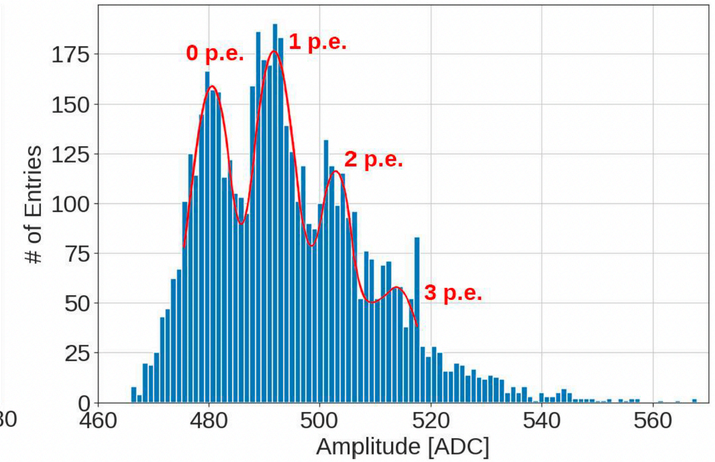
Extra stuff from Omega

Calibration: Single-photon-spectrum

- **2mm²:**



- **9mm²:**

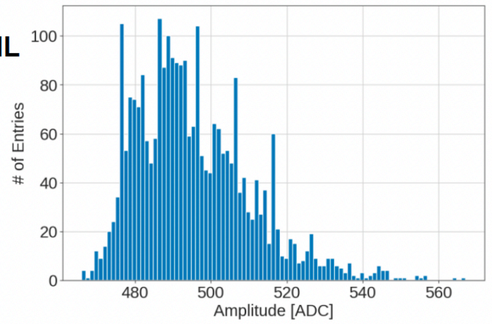


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:



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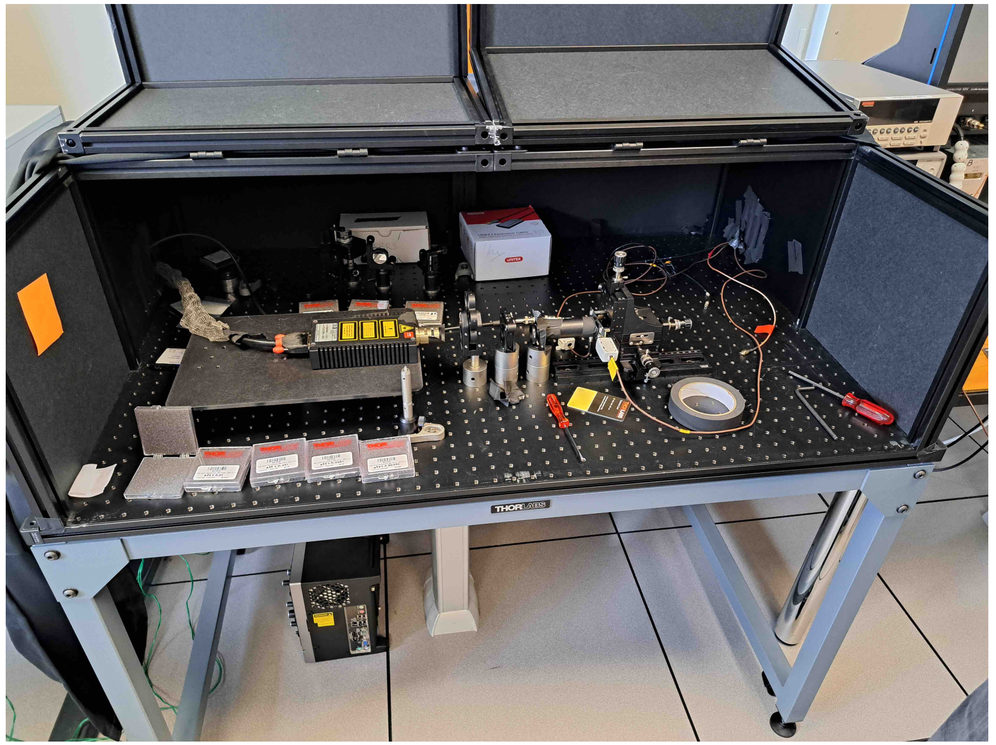
*Thanks to **Jose Gonzales** et al*



Some single photon spectra using the H2GCROC from the Omega test setup

- Small SiPM is clearly visible
- Larger ones are getting less visible (larger capacitance)
- They will also check the 36 mm² SiPM

Summary

Almost fully tested the H2GCROC3A:

- Discovered some known issues (long to list it):
  - Main problem is to read-out consecutive time bins (or 25ns samples)
- This will be most likely fixed in H2GCROC3B

Tests performed:

- Pedestal calibration is performed, they line up easily
- Low injection scan performed for all channels (plots in backup)
- High injection is checked with TOA/TOT turned off
- TOA and TOT calibration checked
  - The TOT can be converted to the ADC_equivalent value, giving us essentially 15-16-bit resolution
  - Shown an example how the readout would work in multiple bunch crossings

External signal:

- Checked the 2V5 injection (same as external from SiPM)
- Checked the self-triggered readout with 90Sr and also very short time (30 mins) in beam
  - Unfortunately, the beam was lost for the rest of the night
- Cosmic setup and seen the MIP peak in multiple channels
- Also the single photon spectra is possible to reconstruct:
  - Curtesy of the Omega test bench setup

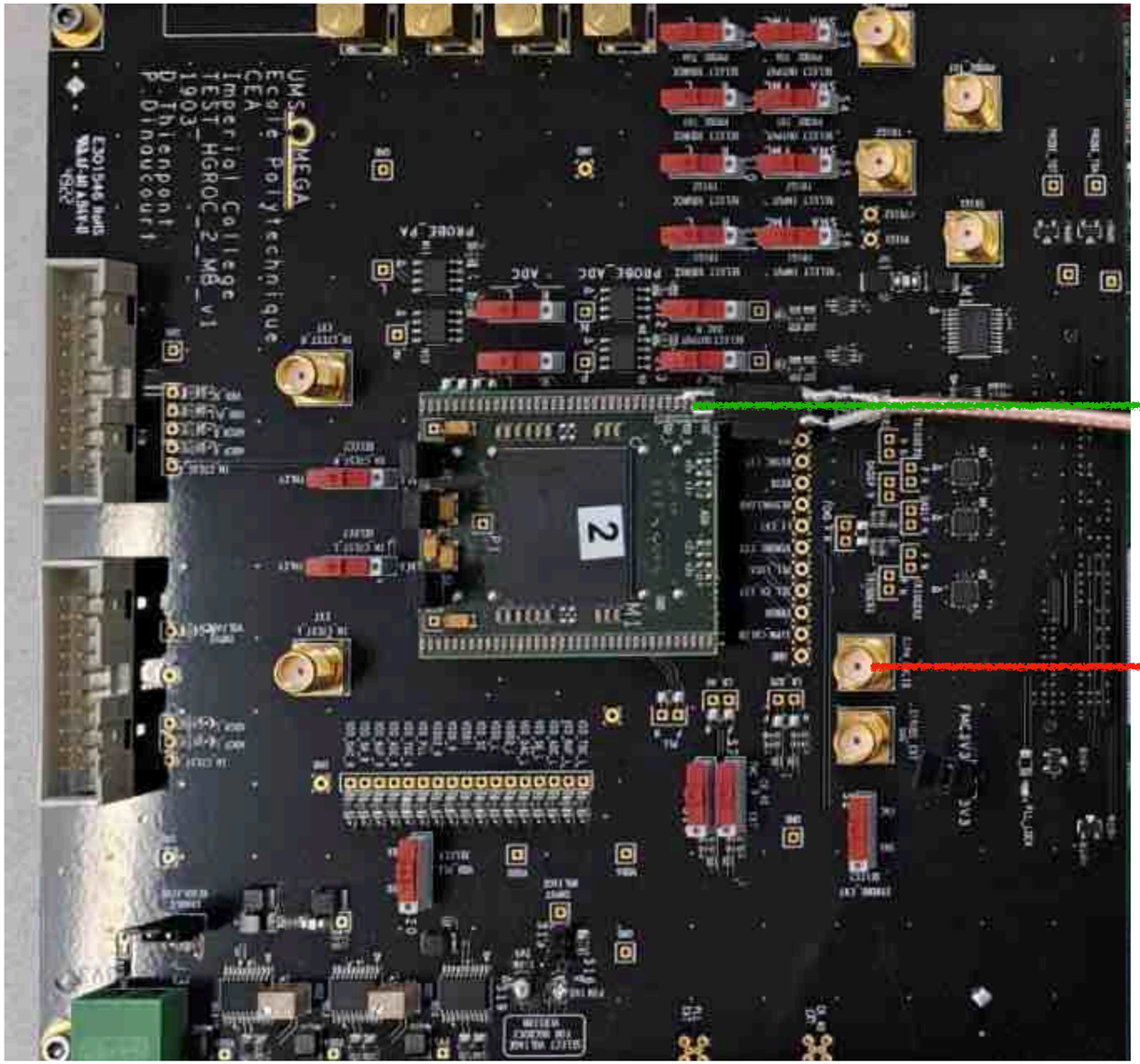
Future

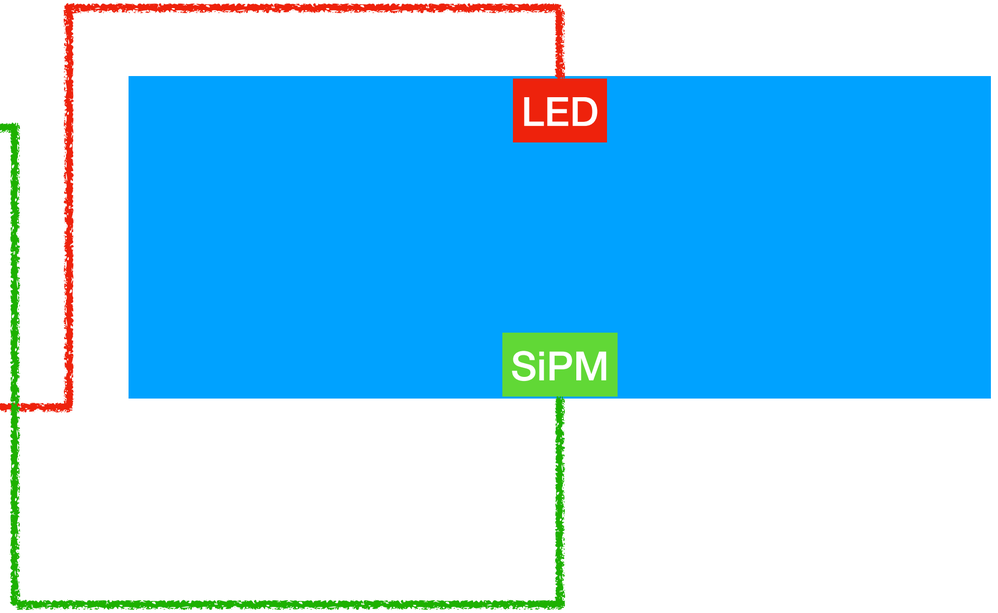
Apply to detectors:

- The new version with the fixes (H2GCROC3B) is coming soon (mid-Nov)
- We plan to produce ProtoBoard2.0 with improved communication also
- Firmware is updated to handle N-Hgcroc readout
  - We can also slowly move towards the RDO design
- Next testbeam probably in May:
  - LFHCAL full module - 520 channels
  - Cross checks with CAEN and HGCROC in same beams
  - Reconstruct the full resolution
- Next-next testbeam in October:
  - LFHCAL 6-8 full module - 56 or 64 channel per module - with summing modules

- Consult with other detectors to try to hook it up:
  - Barrel HCal - they have a working prototype
  - Backward HCal - ?
  - Insert - they have some tiles, but essentially it is the same as LFHCal tiles
  - Barrel ECal - the GlueX prototype - will contact Fernando, Zisis about the connection

Calibration Circuit Plan





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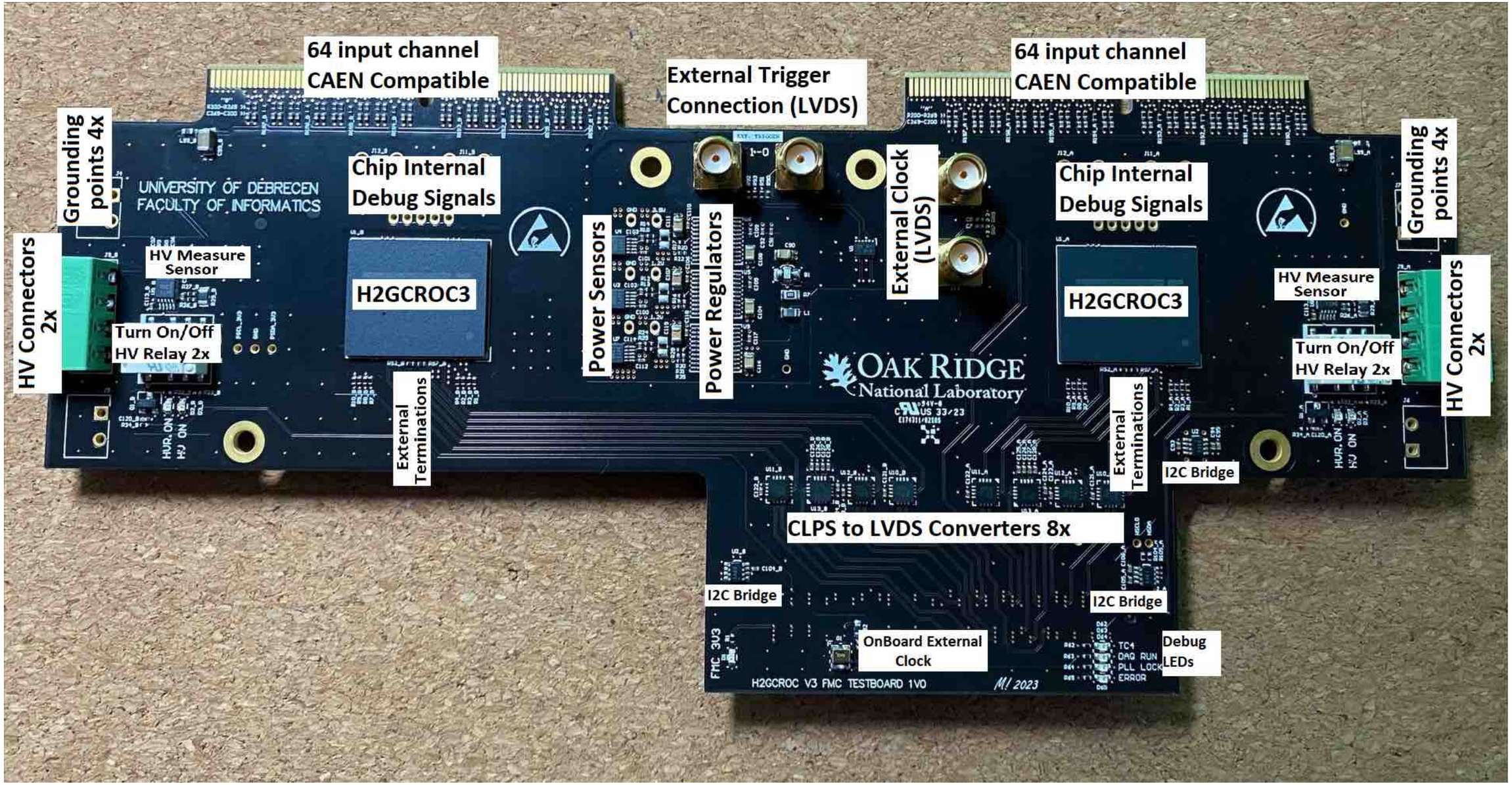
Backup

ProtoBoard1.0 (we have 2 of these)



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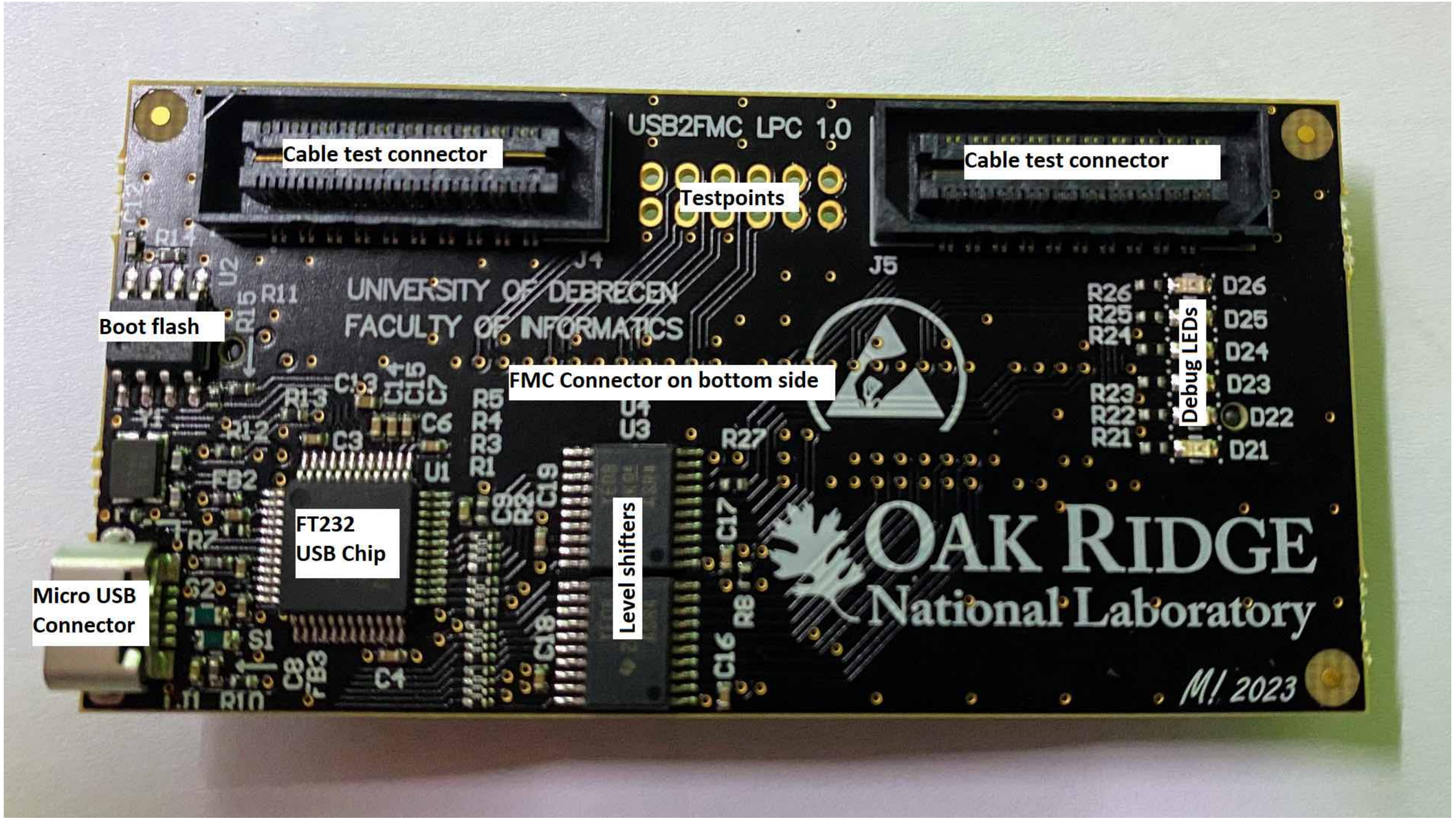
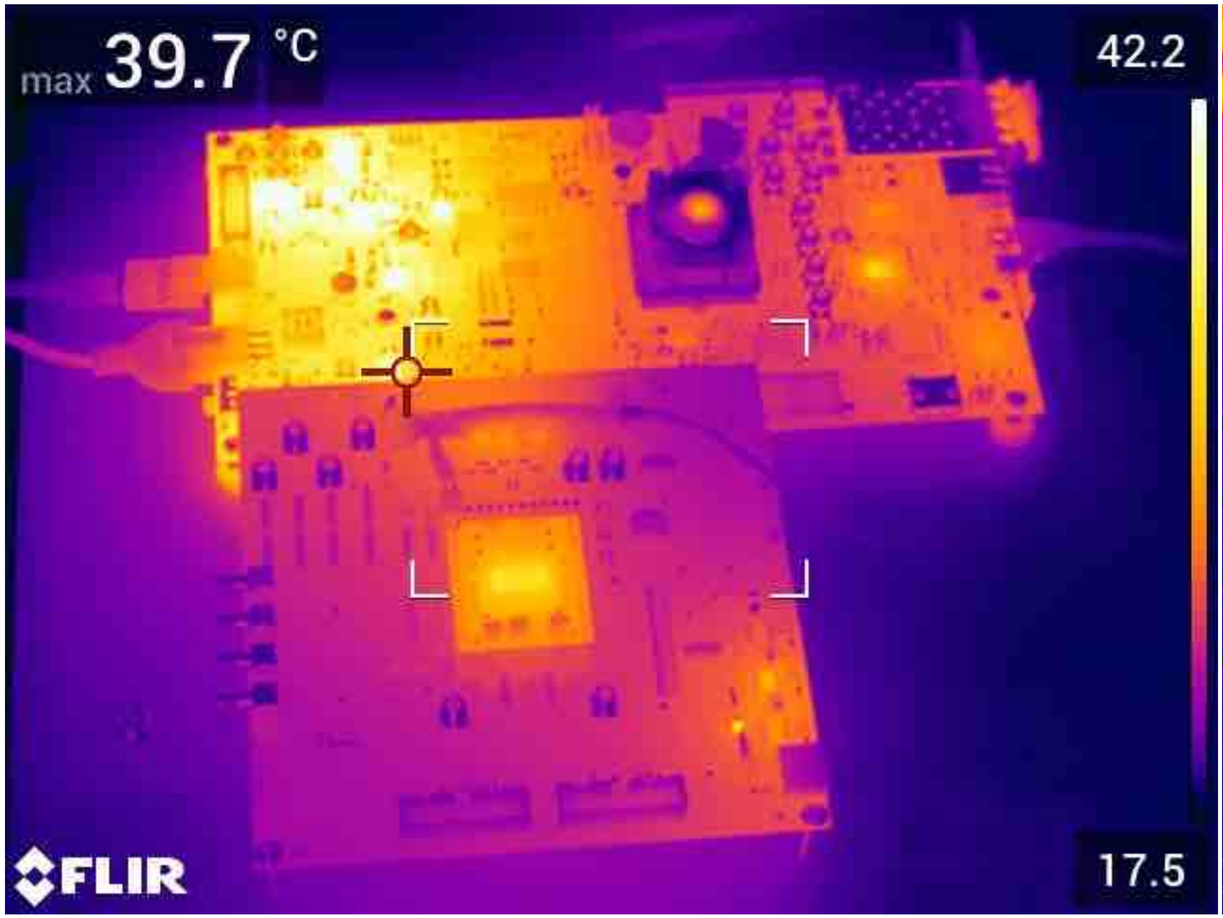
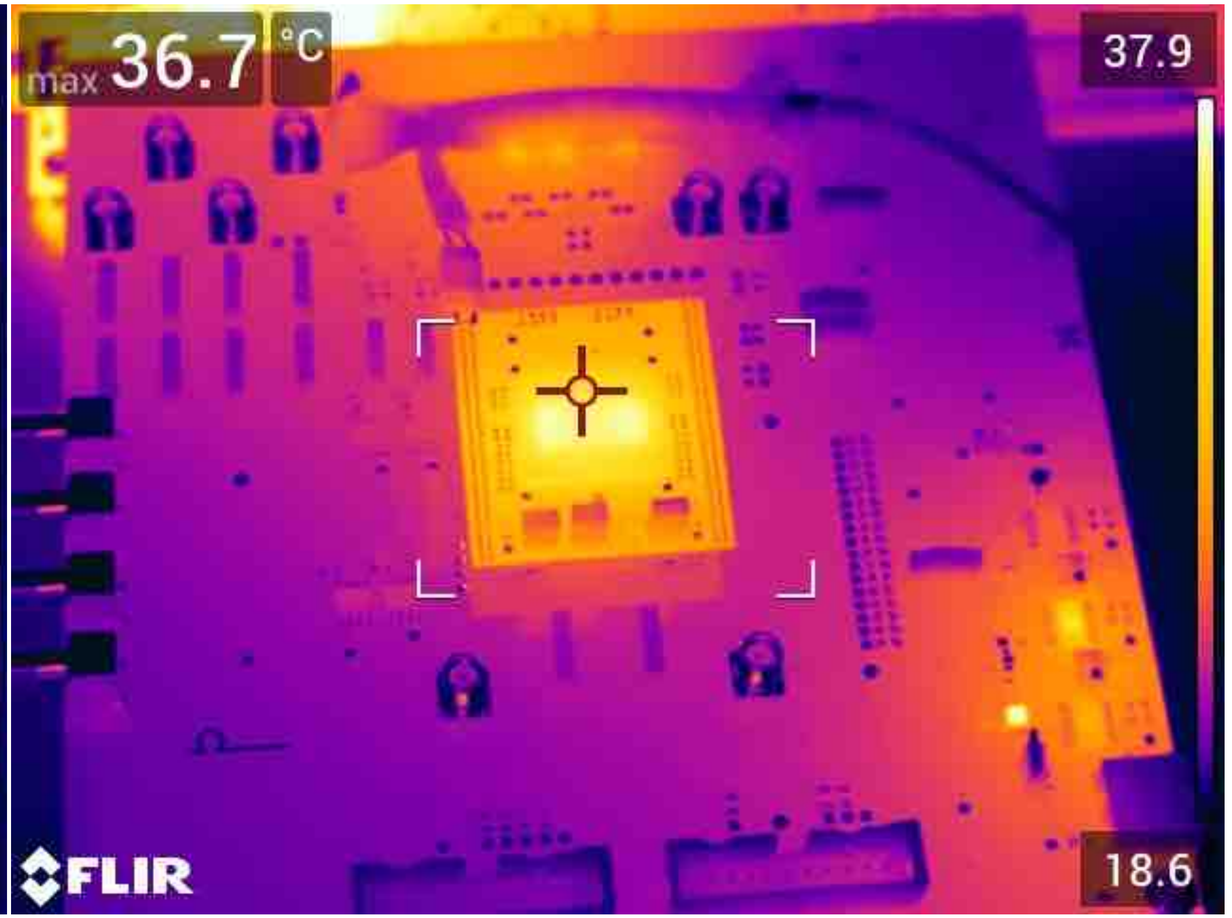
ComBoard1.0 (we have 5 of these)

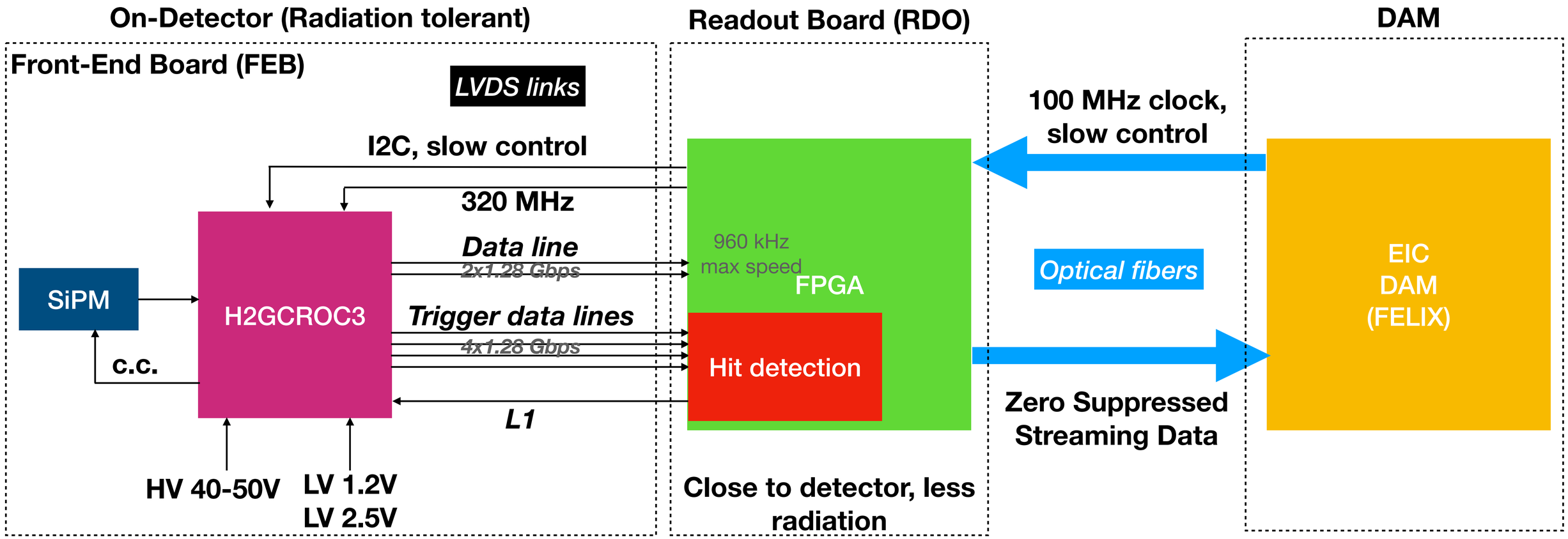


Some IR pictures while working





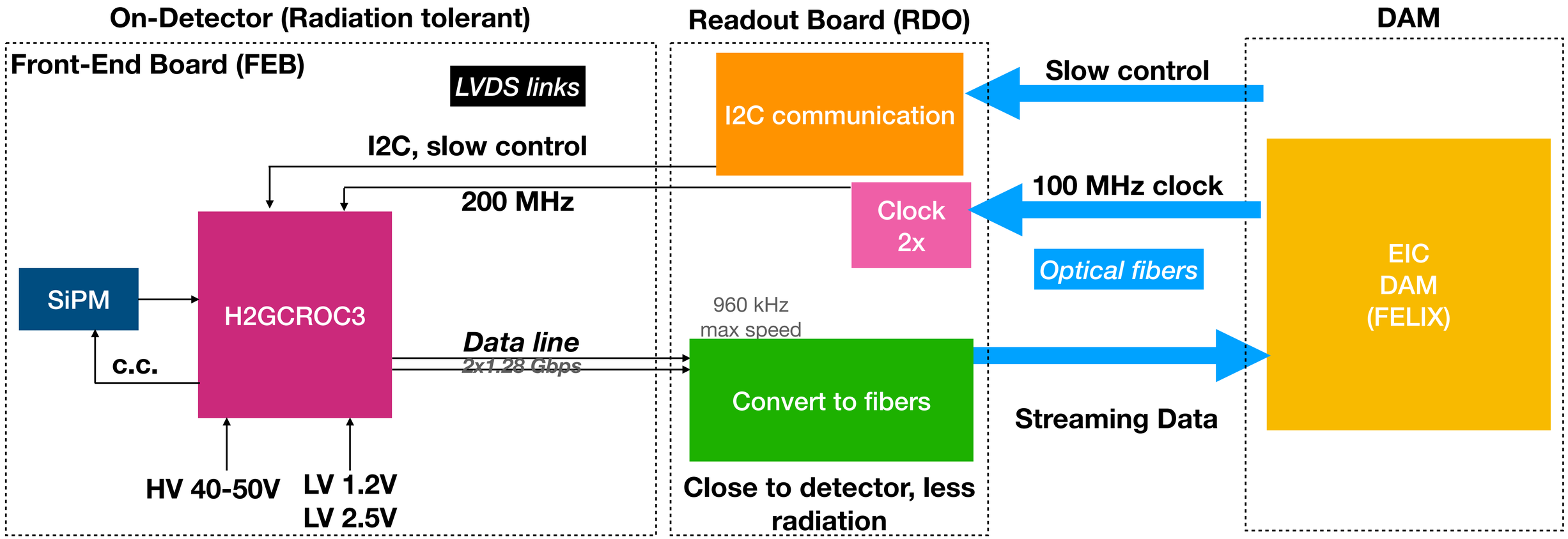
LFHCal readout hierarchy (as of now)



Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

LFHCal readout hierarchy (after the upgrade)



Data propagation from the detector to the EPIC DAQ system:

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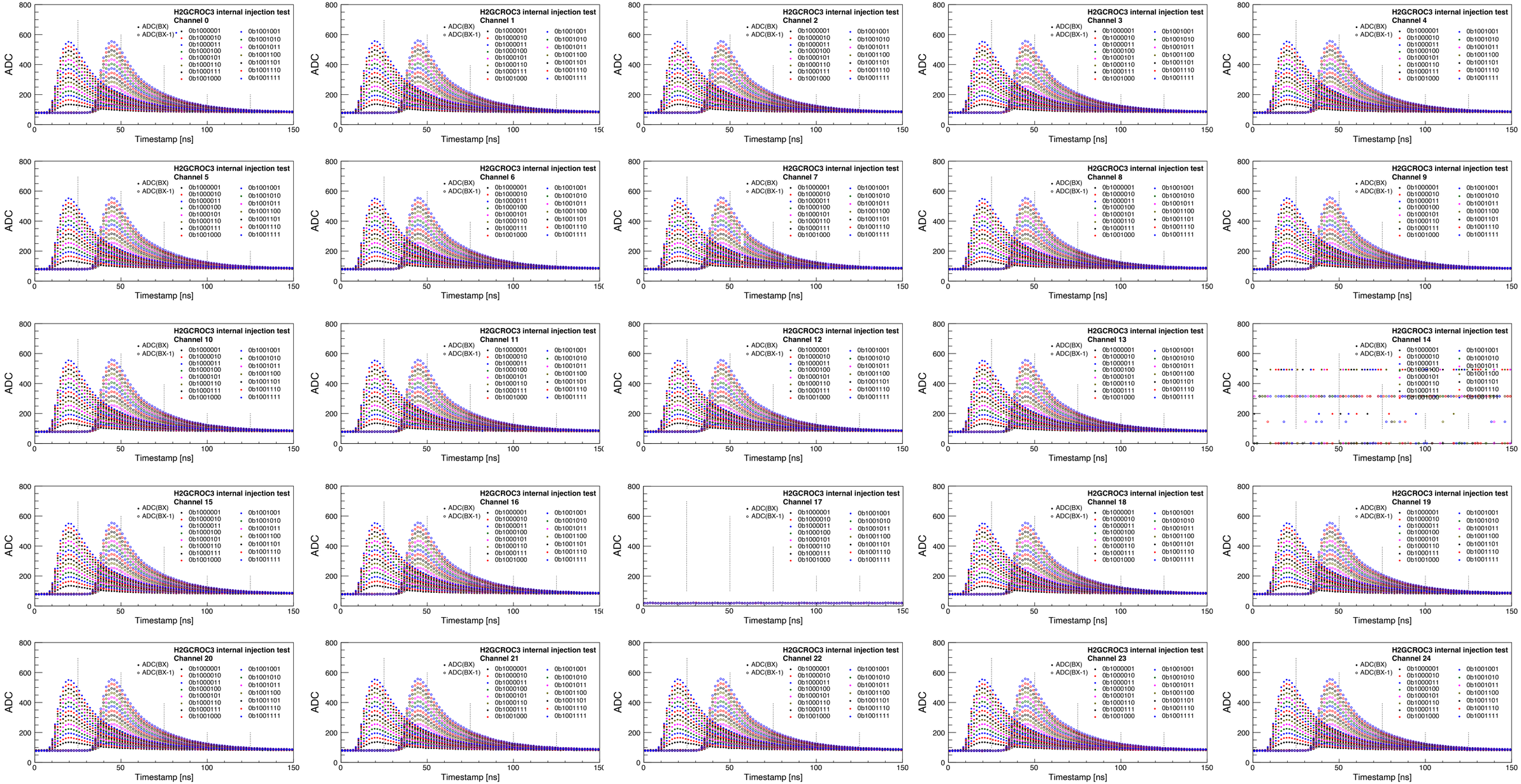
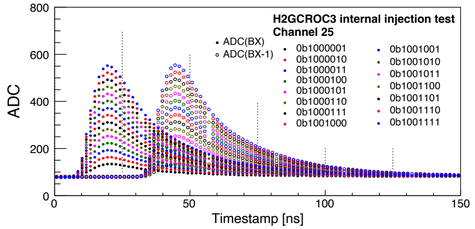
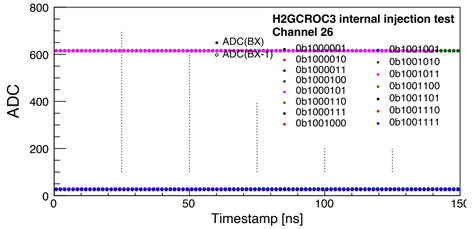
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

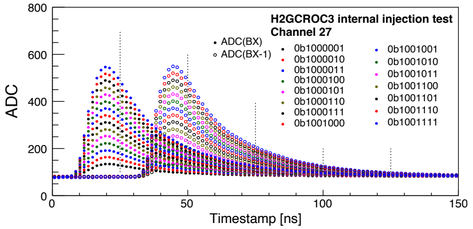
Injection

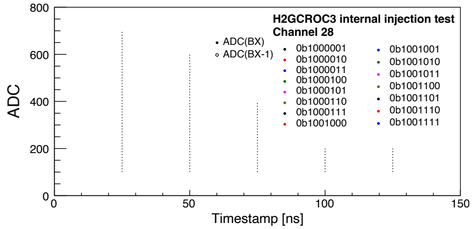

H2GCROC3 internal injection test
Channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 6
Channel 7
Channel 8
Channel 9
Channel 10
Channel 11
Channel 12
Channel 13
Channel 14
Channel 15
Channel 16
Channel 17
Channel 18
Channel 19
Channel 20
Channel 21
Channel 22
Channel 23
Channel 24
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

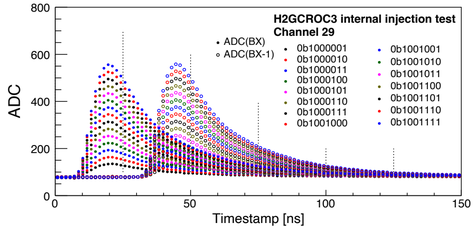
Injection

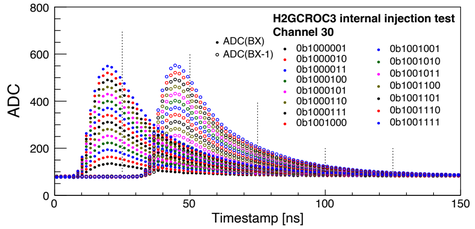

H2GCROC3 internal injection test
Channel 25
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

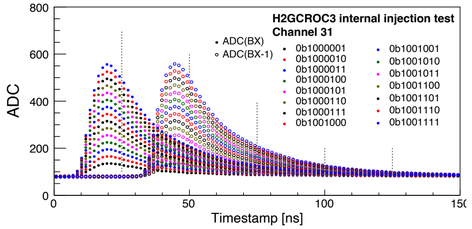

H2GCROC3 internal injection test
Channel 26
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

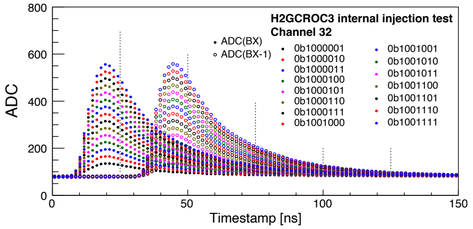

H2GCROC3 internal injection test
Channel 27
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

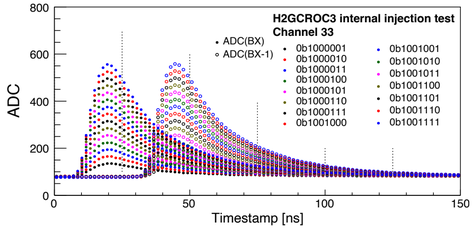

H2GCROC3 internal injection test
Channel 28
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

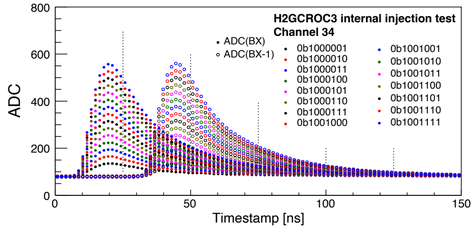

H2GCROC3 internal injection test
Channel 29
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

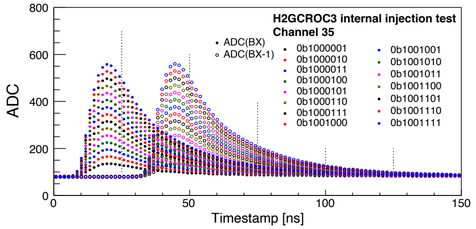

H2GCROC3 internal injection test
Channel 30
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

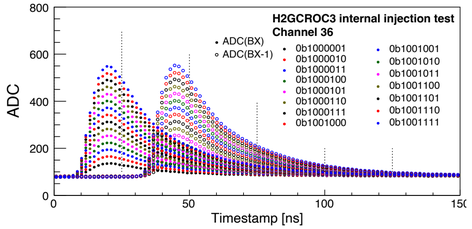

H2GCROC3 internal injection test
Channel 31
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

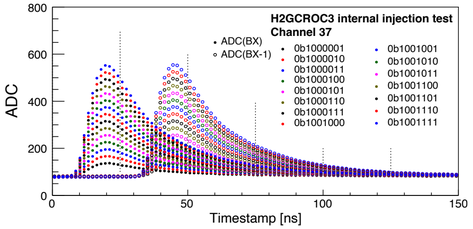

H2GCROC3 internal injection test
Channel 32
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

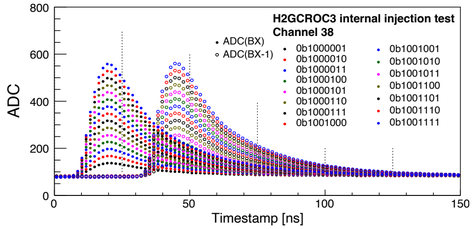

H2GCROC3 internal injection test
Channel 33
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

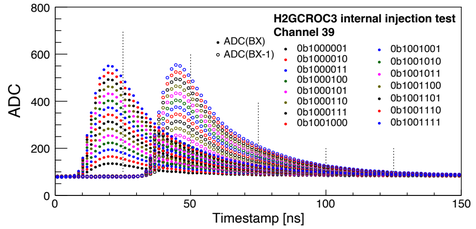

H2GCROC3 internal injection test
Channel 34
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

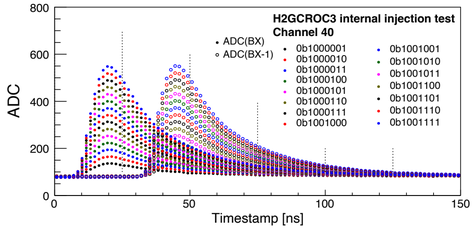

H2GCROC3 internal injection test
Channel 35
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

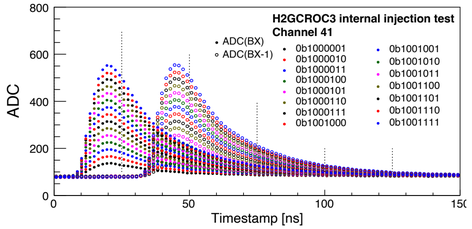

H2GCROC3 internal injection test
Channel 36
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

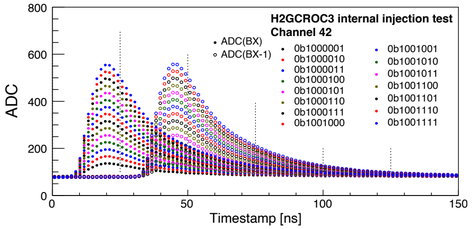

H2GCROC3 internal injection test
Channel 37
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

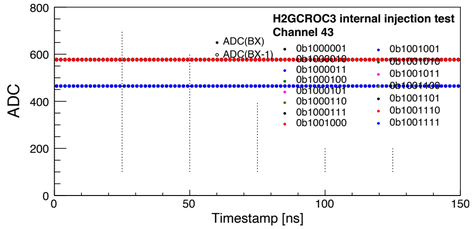

H2GCROC3 internal injection test
Channel 38
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

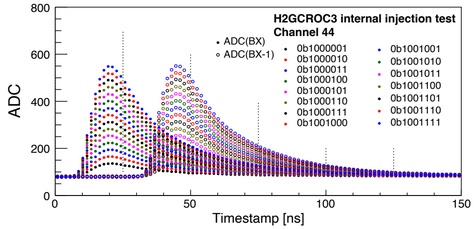

H2GCROC3 internal injection test
Channel 39
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

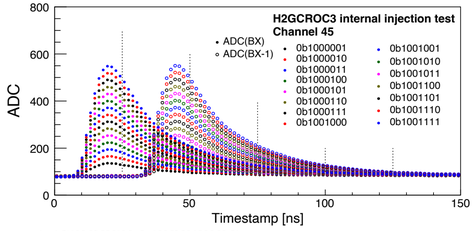

H2GCROC3 internal injection test
Channel 40
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

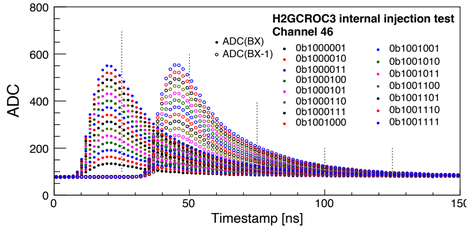

H2GCROC3 internal injection test
Channel 41
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

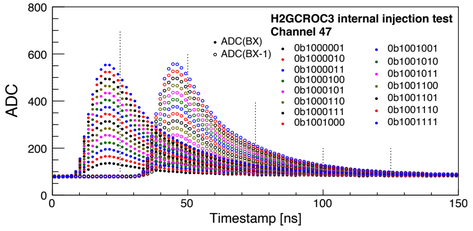

H2GCROC3 internal injection test
Channel 42
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

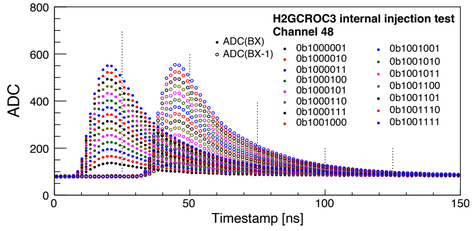

H2GCROC3 internal injection test
Channel 43
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

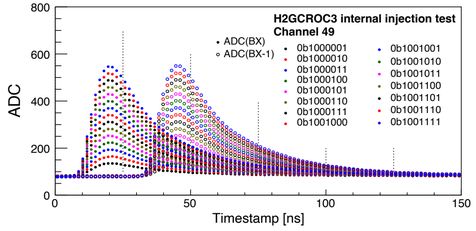

H2GCROC3 internal injection test
Channel 44
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 45
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

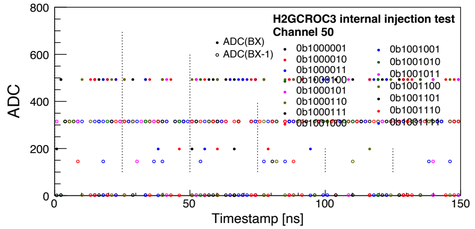

H2GCROC3 internal injection test
Channel 46
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

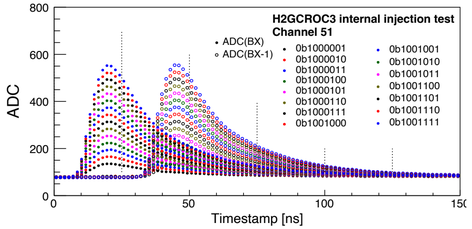

H2GCROC3 internal injection test
Channel 47
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

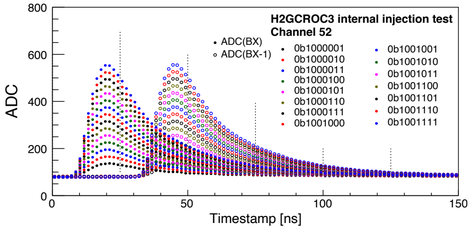

H2GCROC3 internal injection test
Channel 48
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

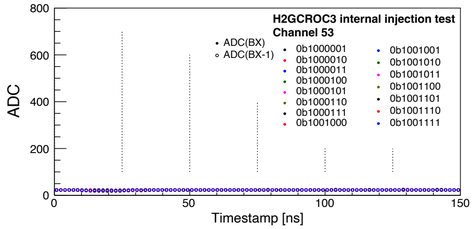

H2GCROC3 internal injection test
Channel 49
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

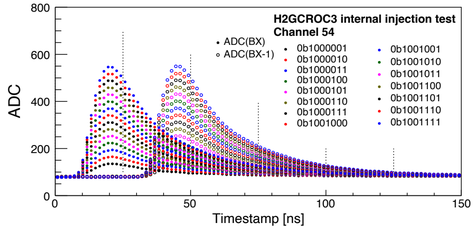
Injection

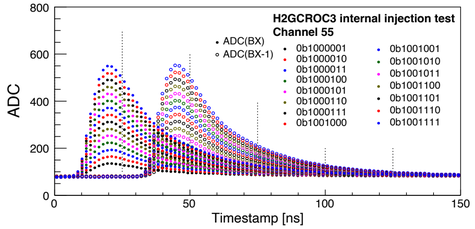

H2GCROC3 internal injection test
Channel 50
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

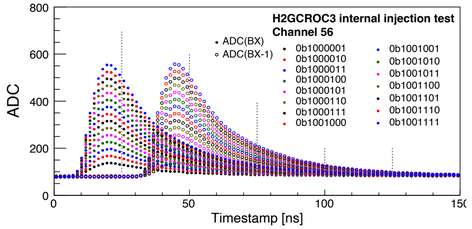

H2GCROC3 internal injection test
Channel 51
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

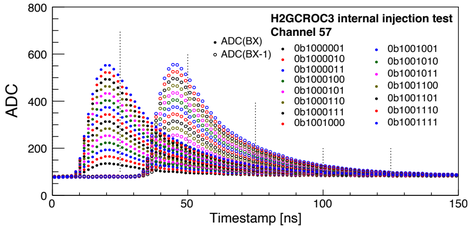

H2GCROC3 internal injection test
Channel 52
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

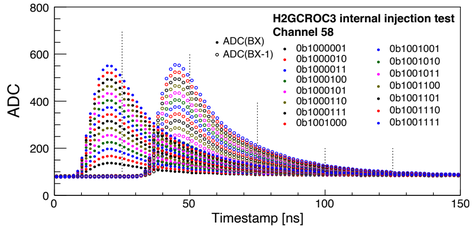

H2GCROC3 internal injection test
Channel 53
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

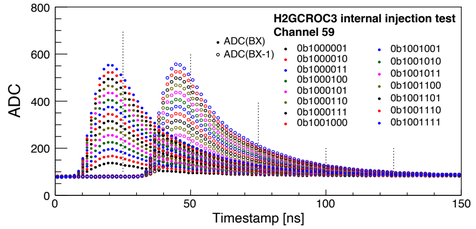

H2GCROC3 internal injection test
Channel 54
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

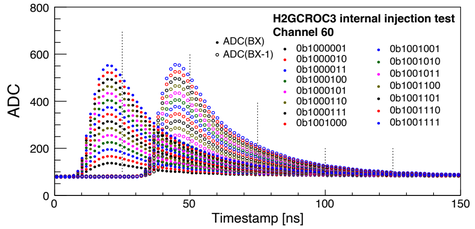

H2GCROC3 internal injection test
Channel 55
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

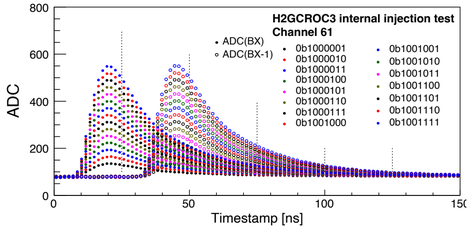

H2GCROC3 internal injection test
Channel 56
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

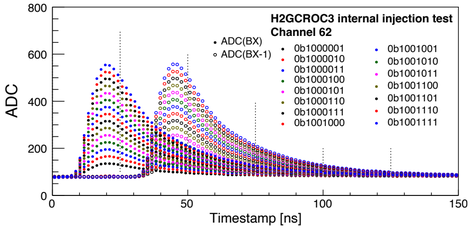

H2GCROC3 internal injection test
Channel 57
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

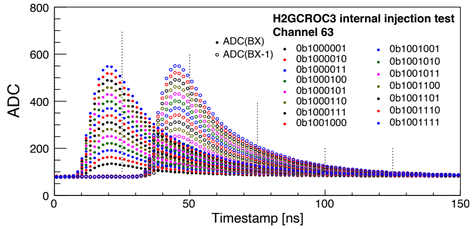

H2GCROC3 internal injection test
Channel 58
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

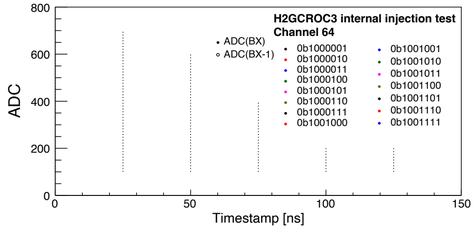

H2GCROC3 internal injection test
Channel 59
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

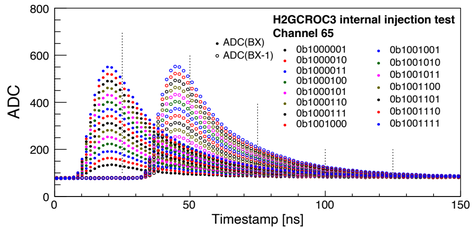

H2GCROC3 internal injection test
Channel 60
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

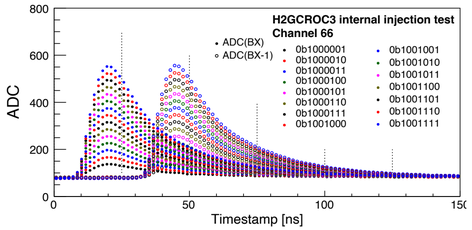

H2GCROC3 internal injection test
Channel 61
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

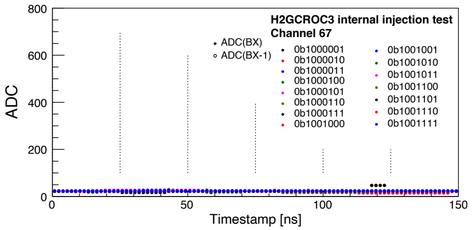

H2GCROC3 internal injection test
Channel 62
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

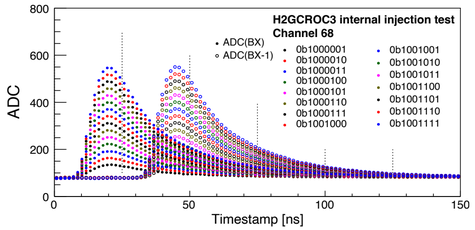

H2GCROC3 internal injection test
Channel 63
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

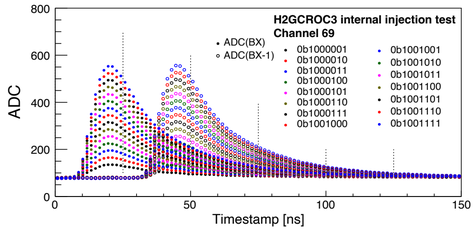

H2GCROC3 internal injection test
Channel 64
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

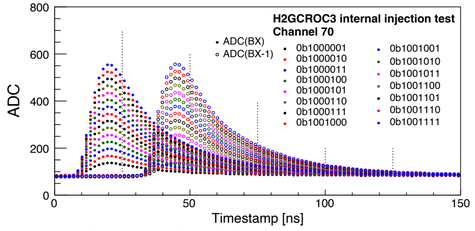

H2GCROC3 internal injection test
Channel 65
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

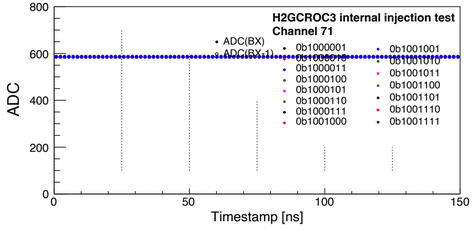

H2GCROC3 internal injection test
Channel 66
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 67
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 68
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 69
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 70
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 71
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]