

ePIC-BTOF用FPCの開発

ラダー用FPC
放熱テスト用試作のためのFPC

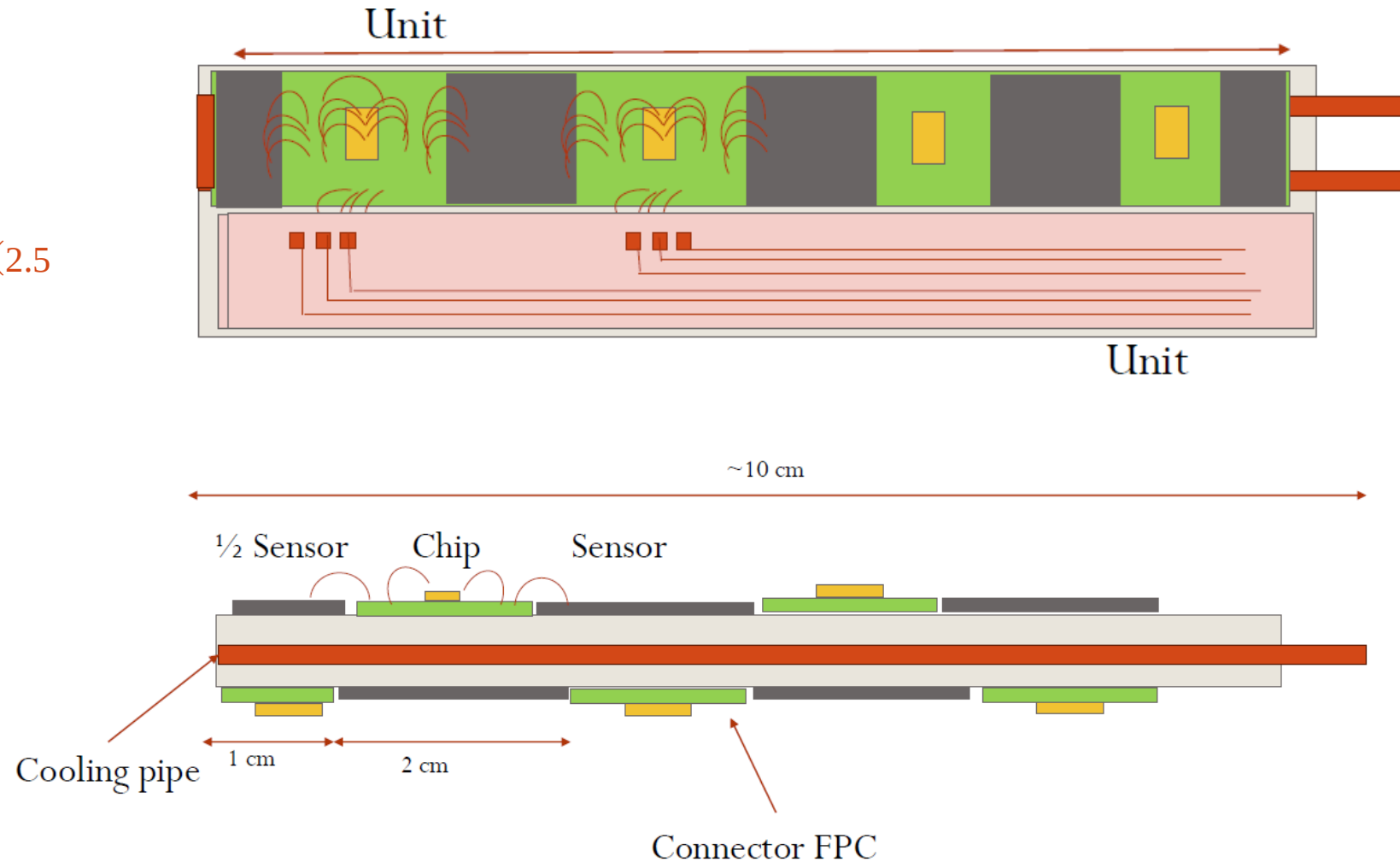
奈良女子大
蜂谷 崇

概要

- 2025/4/14 13:00~ ハヤシレピック社とFPC開発についての打ち合わせを行った。
 - レピック社： 曽我さん、星谷さん、柳川さん、
 - 中川さん、蜂谷、
- 検討項目
 1. 135cmの長尺FPCは作れるか？ 作れるとしたらどうやって。
 2. ThermometerProject用FPCを短期間でつくれるか。

これまで考えられていたデザイン

- 上半分がセンサー + ASIC
- 下半分がFPC
 - FPC用のスペースとして、下半分 (2.5 cm) しかない。



～30cm程度のFPCをつなぐことは可能か？

- Ladder : 135cm long with 34 sensors and 34 ASICs



- Minimize the additional connection
- Assembling this very long module is difficult
 - Yield rate will be issue during the production

- If split by 3 pieces, each FPC is 50cm long



- 50cm FPC can be made with minimum risk in production
 - Finer line & space available (60um x 60um)
- Multiple connection needed
 - Reduce active area by connecting these FPCs
- How connect each other ~ 200 lines + power + GND
 - spTAB bonding
 - Connector (micro pitch)
 - Fragile, (not so reliable?)



Simone's slide in Nov. 2024

FPC idea

- FPCs are spTAB bonded to be extended so it's flush

• Flex are stacked and glued on the stave one on top of the other

• Side view

11 2024/11/7 Dr. Simone M. Mazza - University of California Santa Cruz

FPCを実現するために考えないといけないこと

- 135cmの長さ
 - どうやってつくるか？ 実現可能か？
 - 形状はINTTのバスエクステンダ（最大130cm）に似ている
 - 全長を1枚？ 複数をつなぐ？
 - つなぐ場合の方法？ TABボンディングは？
 - FPC内の配線
 - 何層？
 - バスエクステンダの経験から1枚だと信号層は1層がよい 歩留まり
 - ASICとFPCの接続
 - ワイヤーボンディングを想定
 - TABボンディング可能か？
-
- レピック社にTABボンディングの経験はない。 試作・テストが必要
 - TABボンディングについて調べてくれる： レピック社柳川さん
 - 1枚

つなぐ方法



TABボンディング



補助FPCをつかってブリッジする

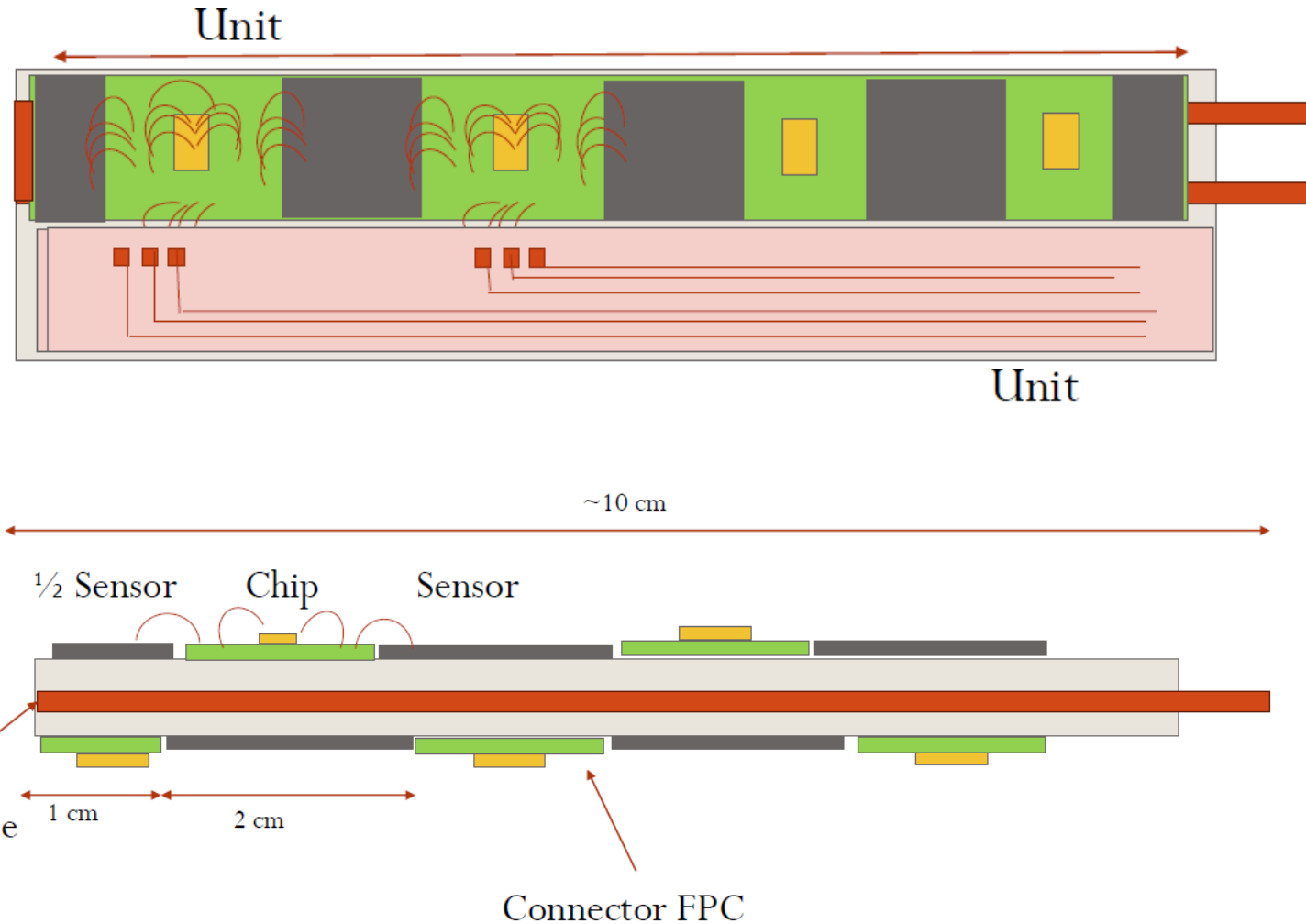


- TABボンディングの配置密度などの情報が必要

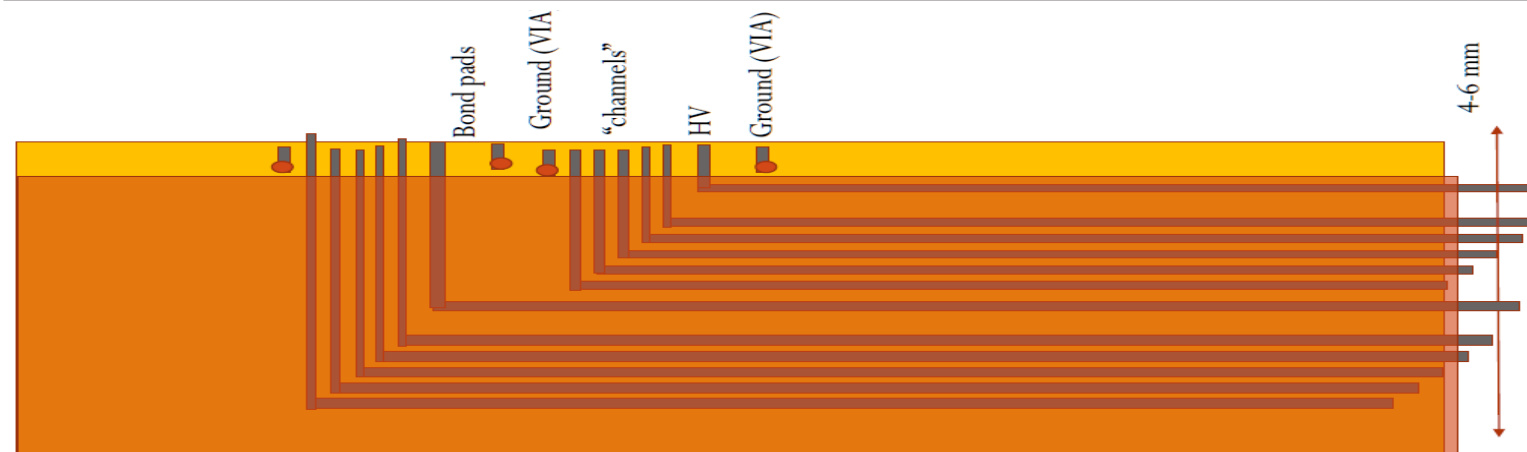
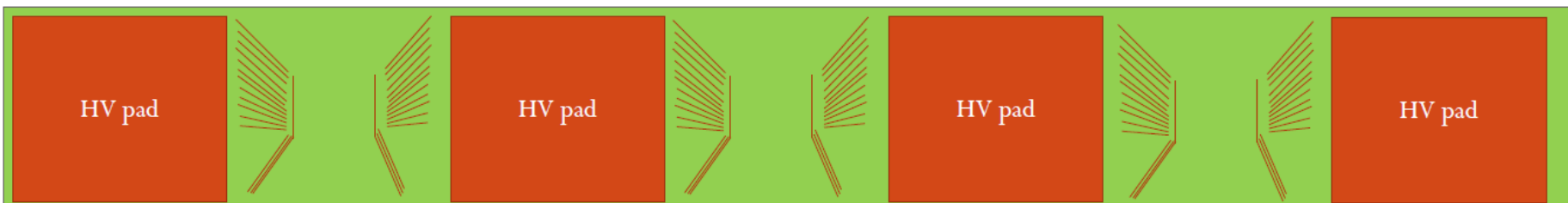
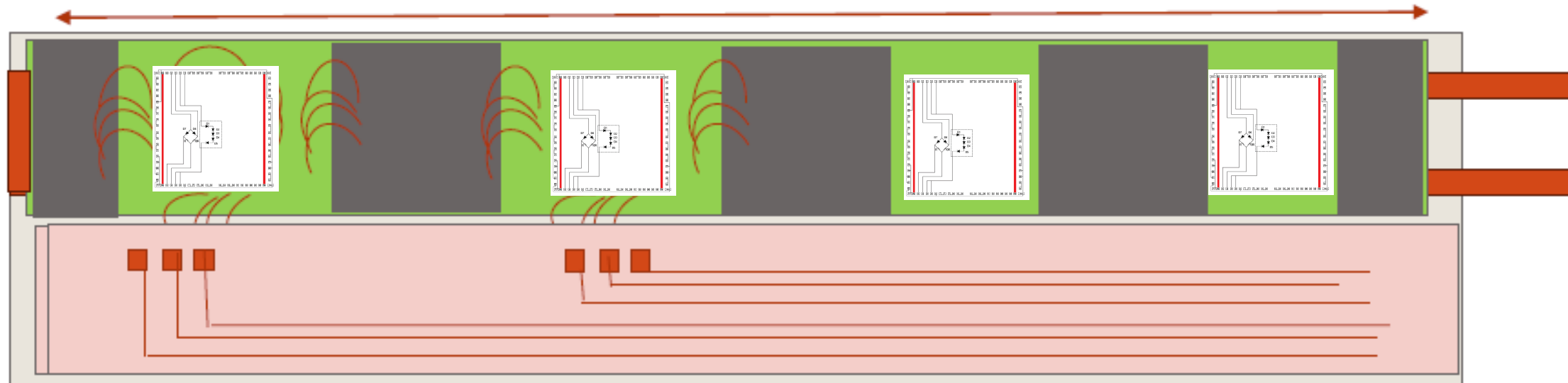
試作FPC

排熱テスト用試作機

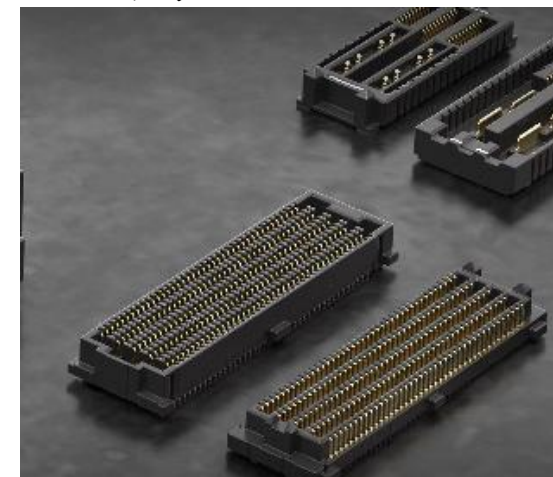
- ゴール: 実装 + 排熱をテストする
 - 組み立て + 実装のテスト
 - 熱の逃げ道をみる
- 進め方:
 - パーデュ大 + ORNL : ステーブ (構
造材) + FPCとの張り合わせ
 - FPC from JAPAN (Takashi and so on)
 - UCSC will glue, verify positioning and
wirebond sensors and silicon heaters
 - Heaters (1x1cm) have embedded
temperature sensor and a series of bond pads
to be paired with sensor.
 - Purdue or ORNL will assemble the two half
staves with cooling pipe
 - UCSC will perform electric and thermal tests
- HPK sensors arrived at UCSC, many are
NOT working, so ok to be used in this
project



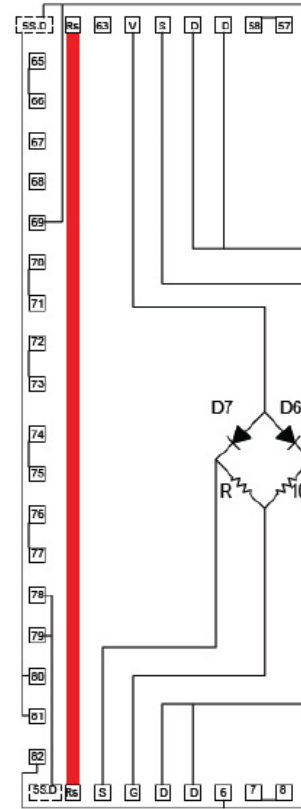
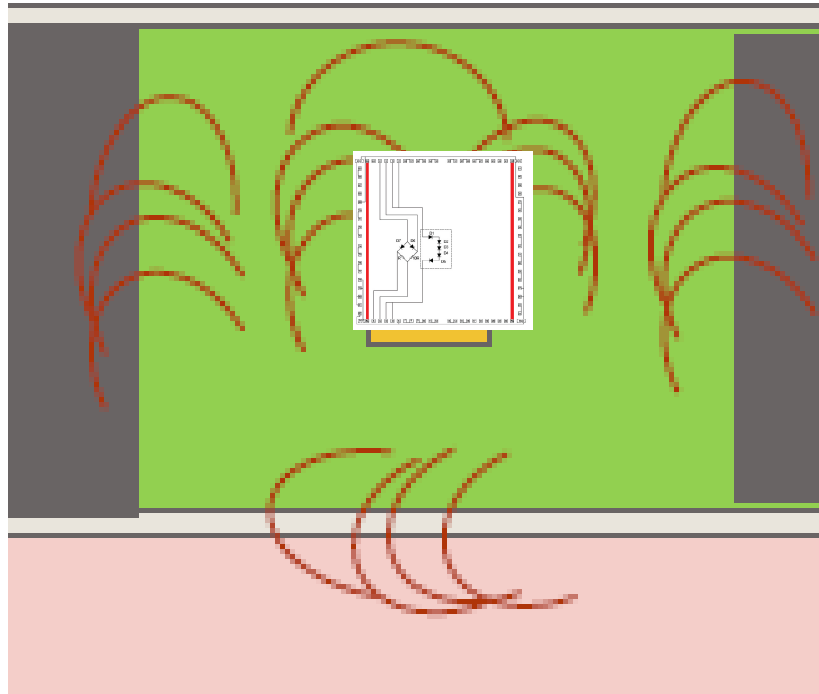
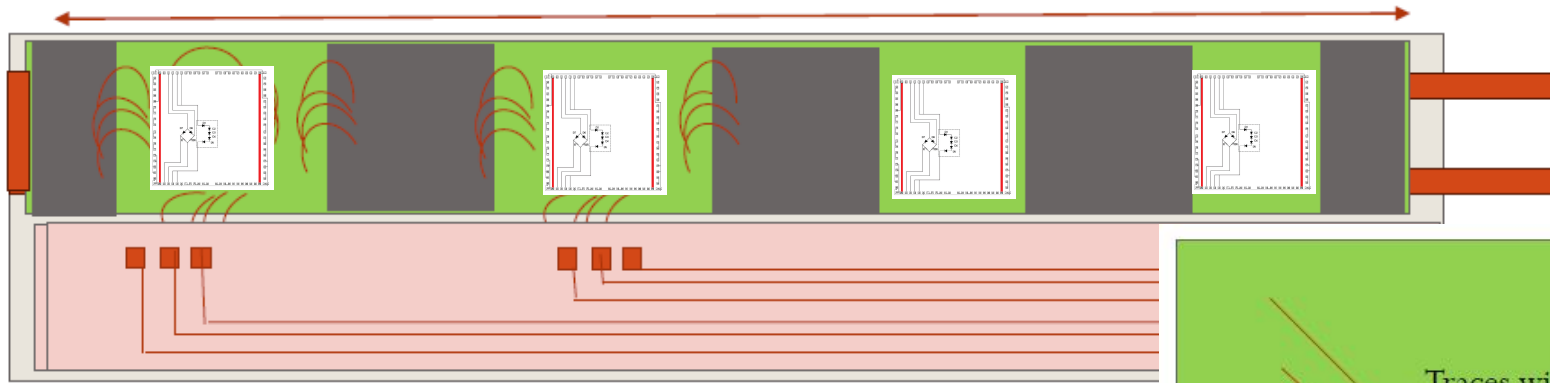
Unit



この端のコネクタをどうするか？



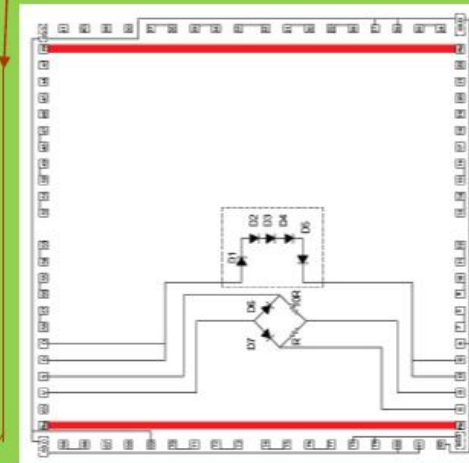
Unit



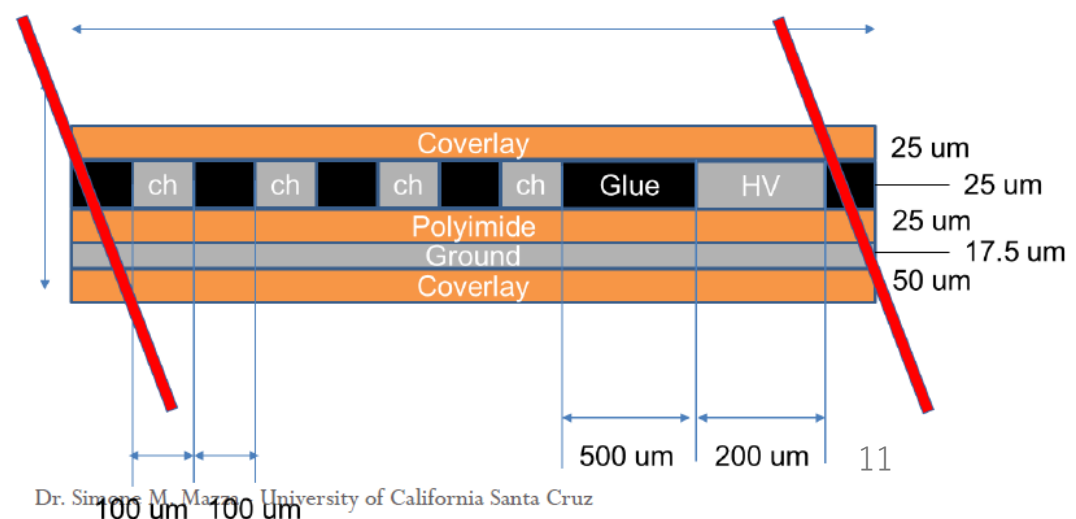
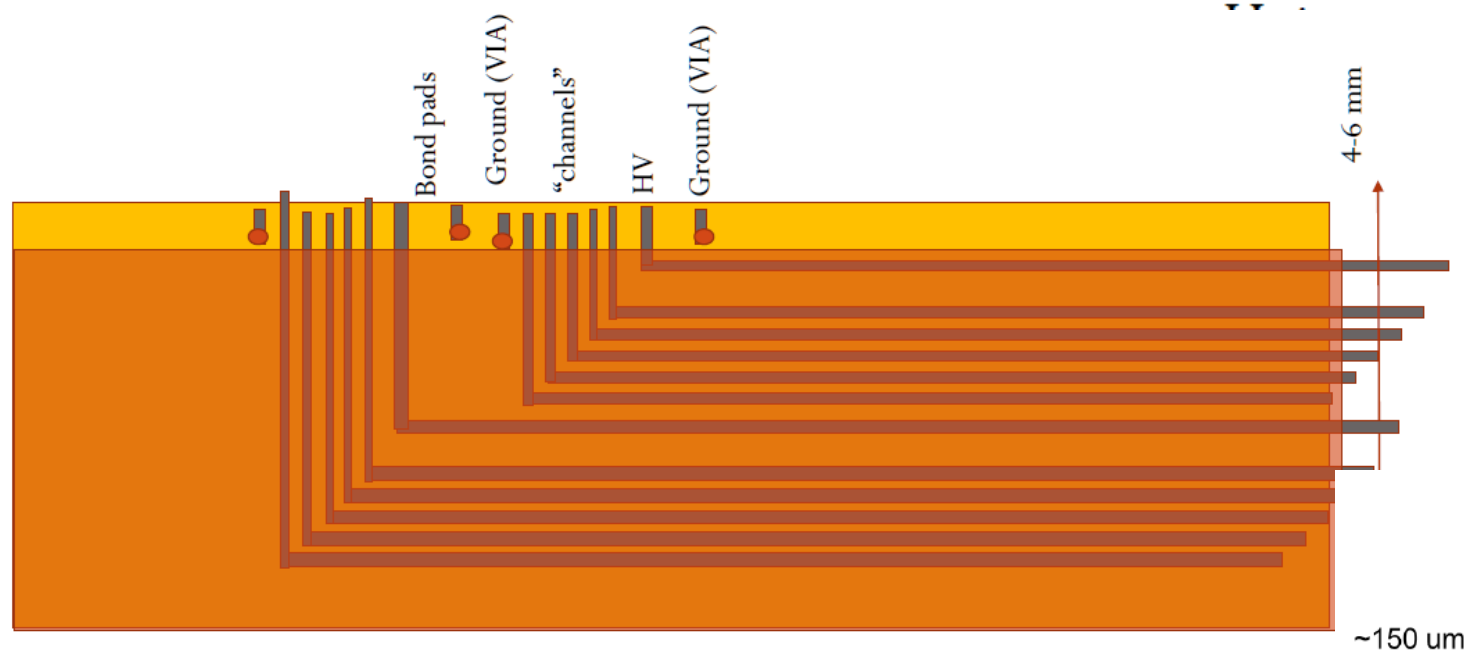
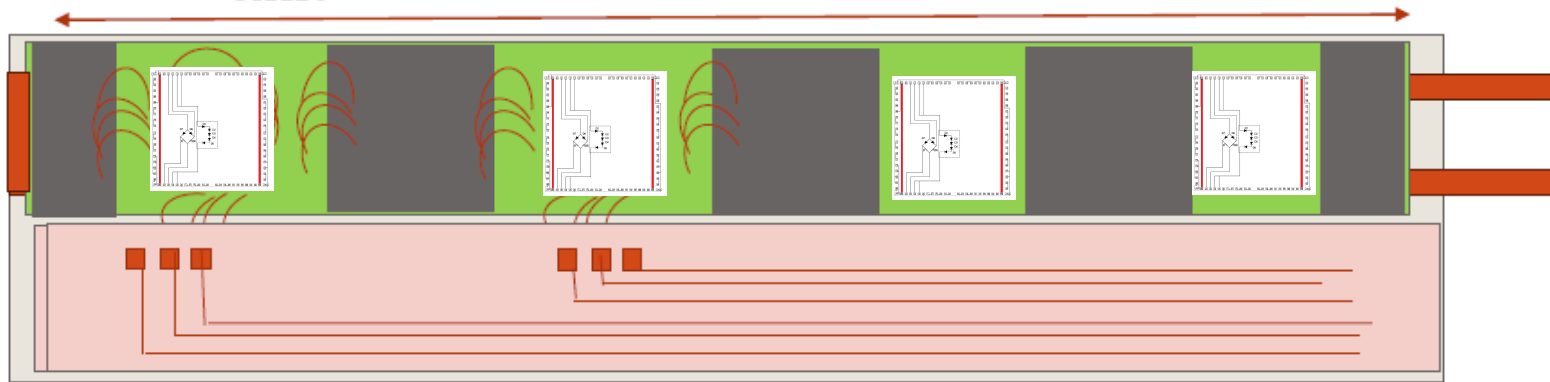
e

Traces with bond pads at both ends

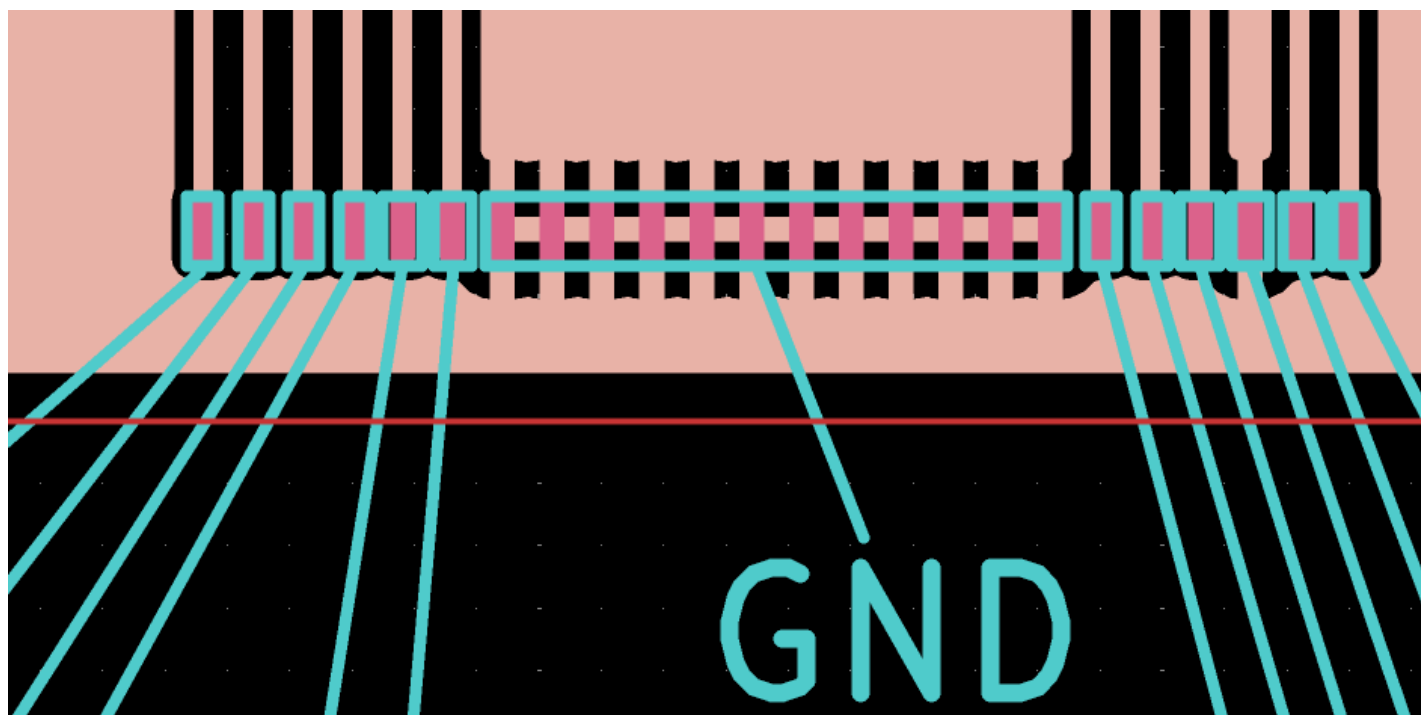
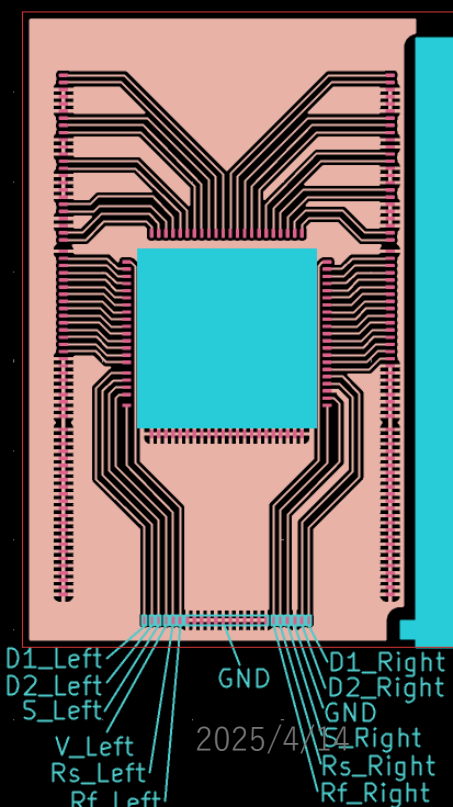
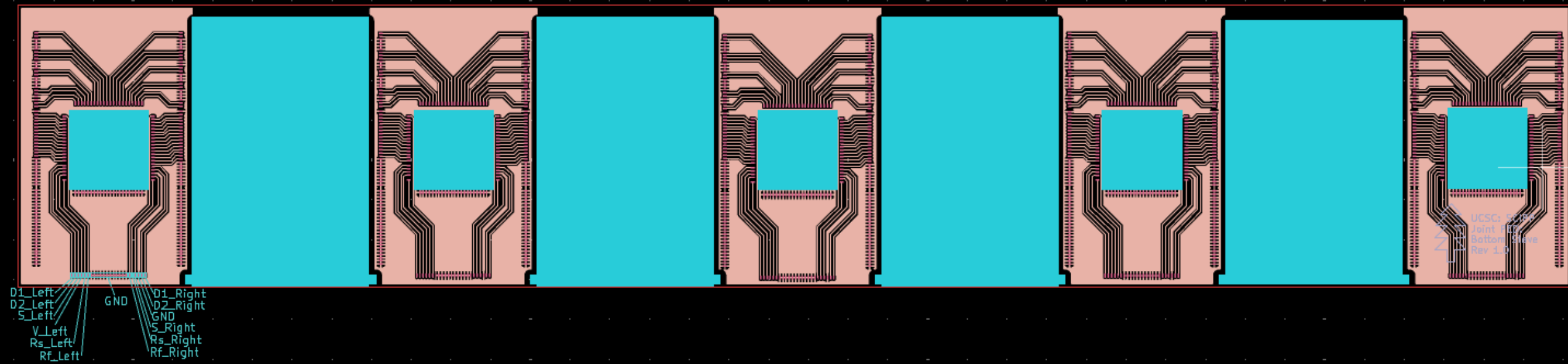
This is for heater on the other side, under wirebonds?



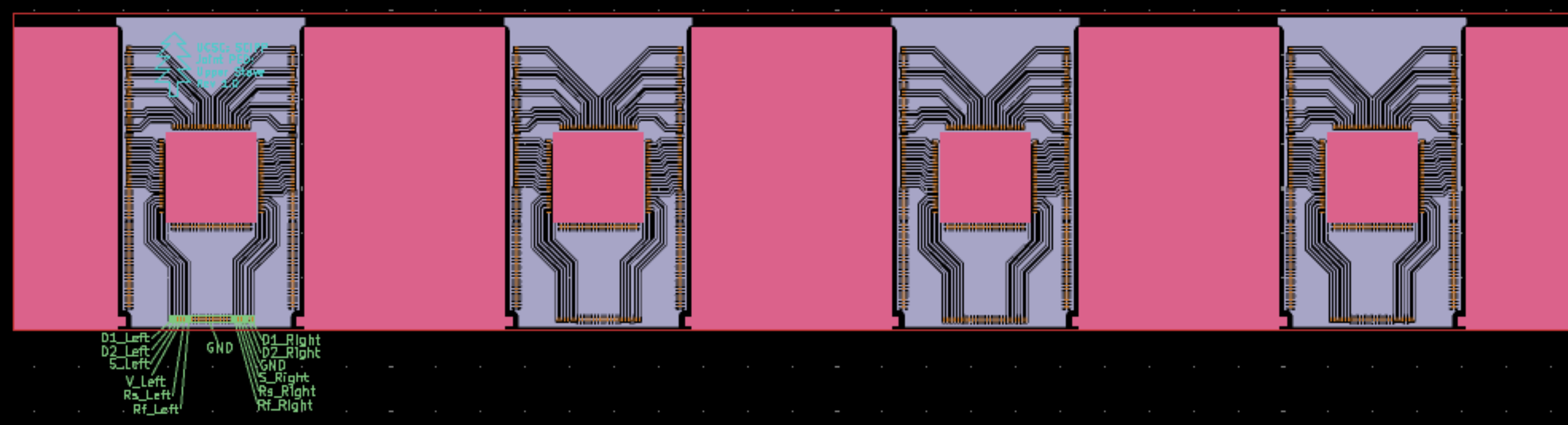
Unit



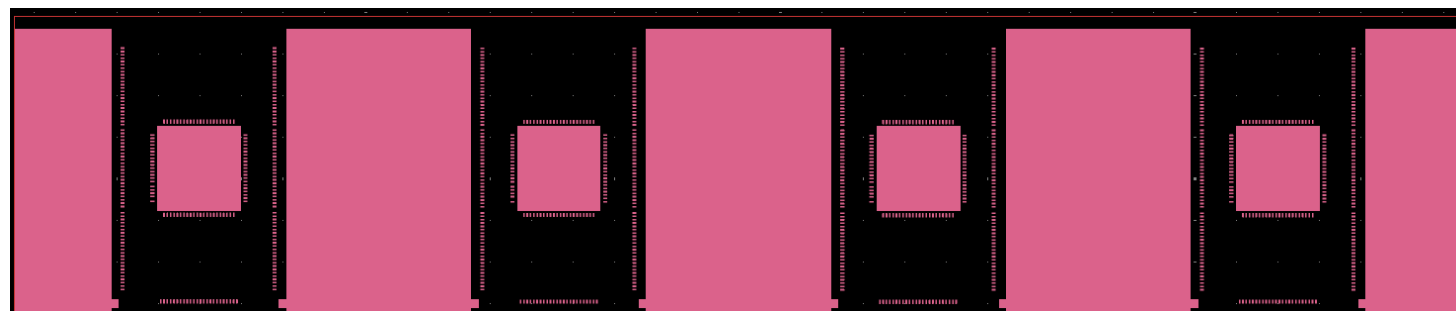
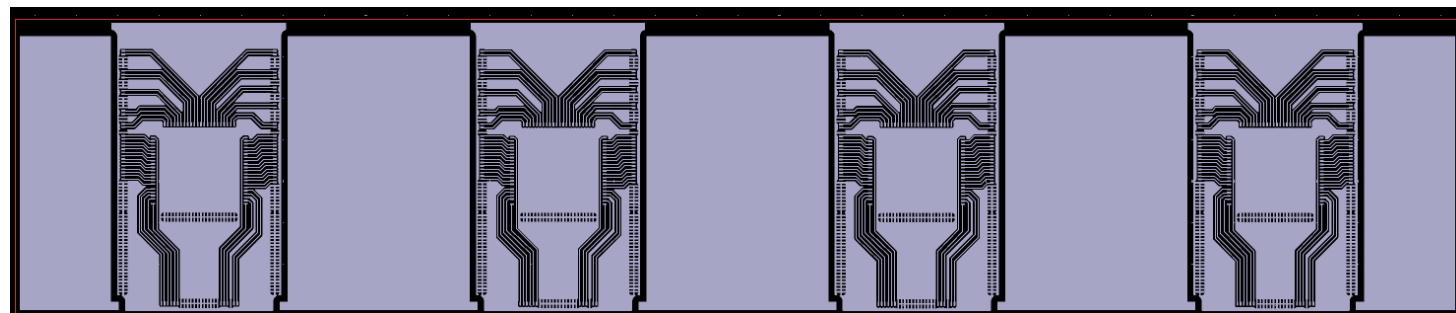
2025/4/14



- ガーバーデータあります。



• 裏面



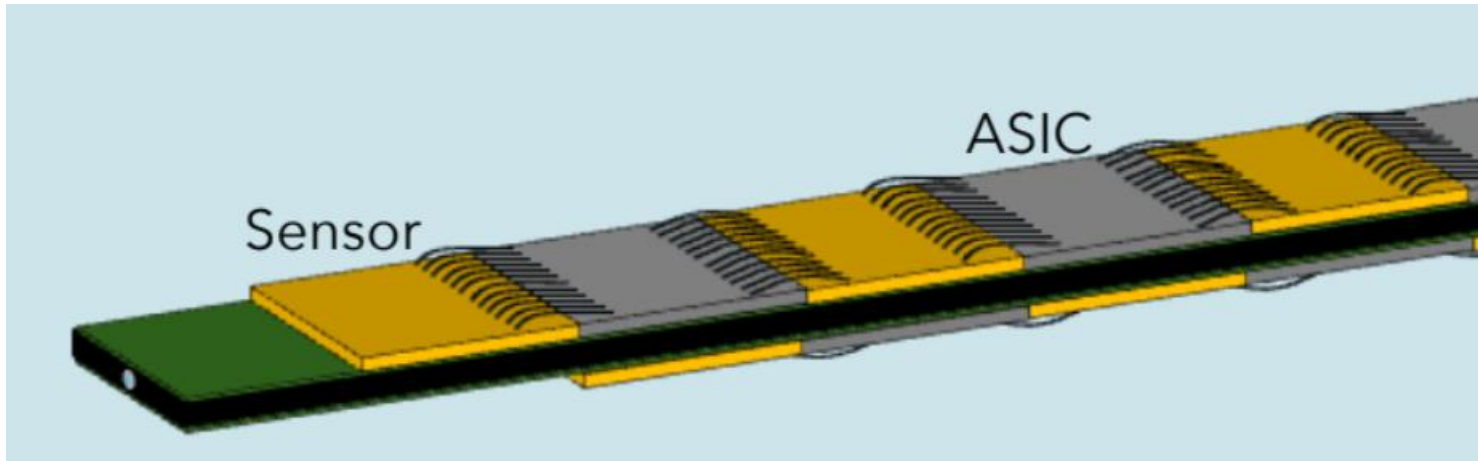
スケジュール

- 次のCDのレポートに載せたい
- 製造まで数か月(6月頃?)
 - 蜂谷も予定を聞かれた(4月以降は可と返答)
- FPC製造の不明点
 - 具体的はパッドの位置
 - 反対の端の扱い(コネクタ?)

相談したいこと

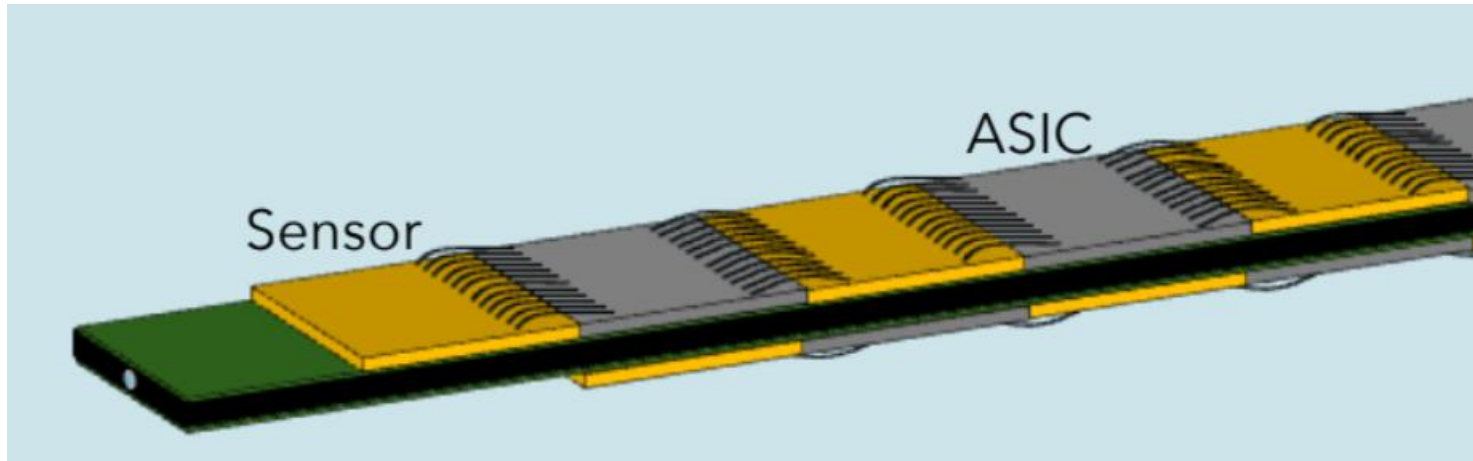
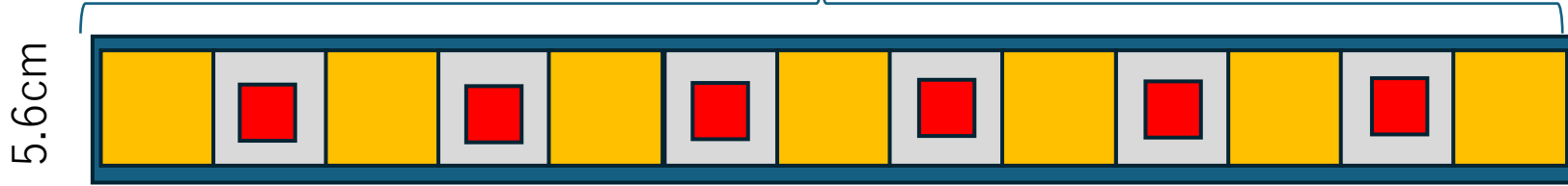
- 排熱テスト用試作機のFPCの設計と製造
 - 1～2か月。
 - 簡易で安く作りたい。
- BTOFラダー用FPC
 - そもそもできるのか？
 - 短いものをつなぐ方法を検討したい。

表裏にFPCを配置する例



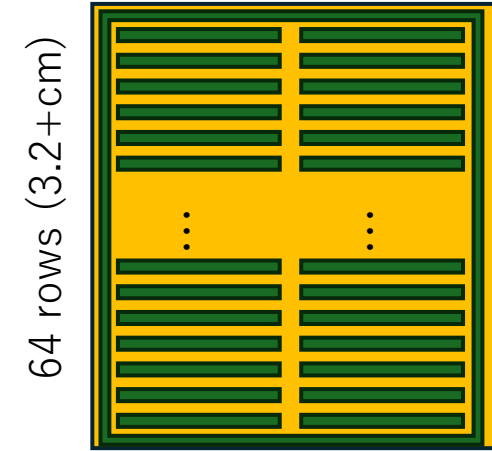
- Belle-IIのダブルサイドストリップ検出器
 - 折り紙接続が参考になるかも。

BTOFのハーフラダー

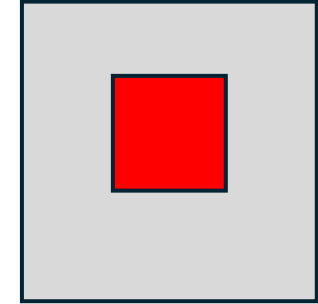


- 構造材を挟んで、表面と裏面にセンサー + ASICを配置
 - FPCは両面に必要
 - FPC : **135cm** + **コネクタ部**
 - **センサー** : **3.2cm x 2cm x 34個 (33個)**
 - **ASIC(未定)** : **既存のASICをBTOF用に改良予定**
 - **配線数** : **~200 (34FPC)** (INTTは124本)

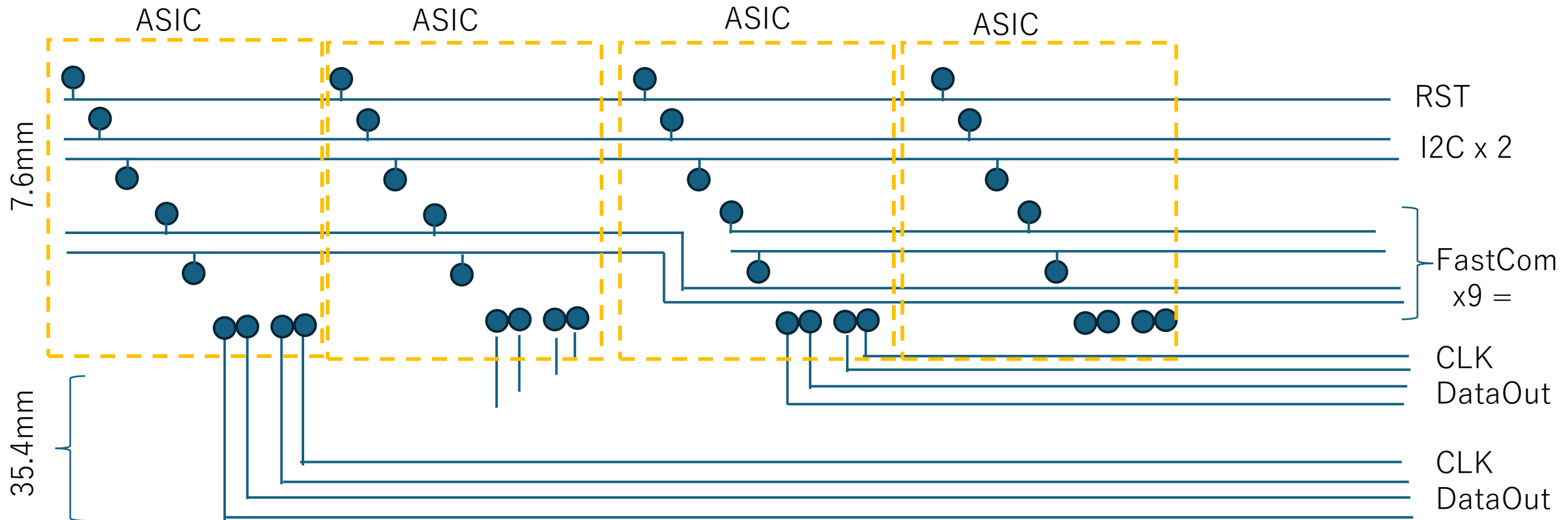
センサー (FPC)
2 cols(2+cm)



インターポーザ (FPC)



信号層を単層にする検討



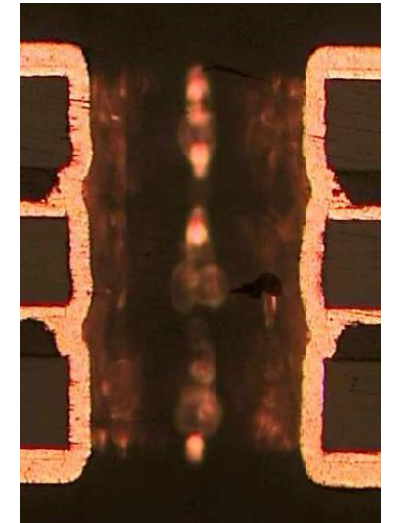
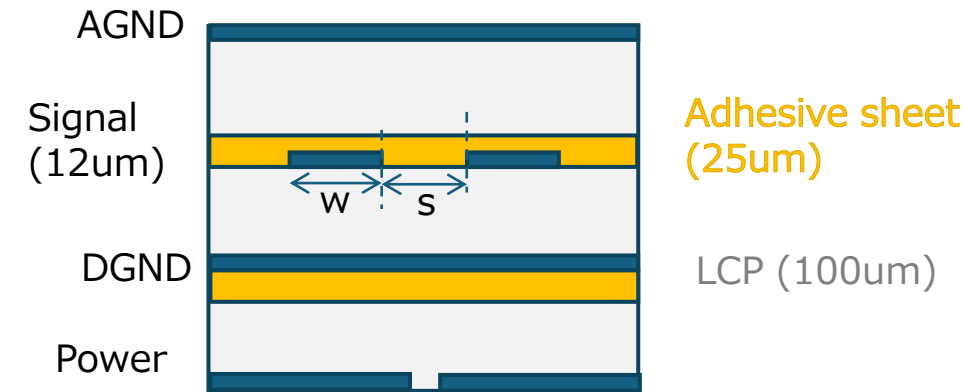
- バスエクステンダのデザインをもとに検討
 - Line (130um) + space (130um) + Land (for thru hole) = $\phi 300\text{um} \sim 600\text{um}$
 - Thru hole width : $\sim 8.8\text{mm}$ ($0.6\text{mm} \times 7 + 0.52\text{mm} \times 8 + 0.6\text{mm} = 4.2 + 4 + 0.6$)
 - Line area width: $34 \times 4 \times 260\text{um} = 35.4\text{mm}$ + アナログ配線
 - Land for powers and GND are also necessary
- ~44.2mm :
signal lines occupy < 5cm width

Long FPC from sPHENIX INTT

4 layers laminated by the adhesive sheet

- Cable design (prototype)

- Dimension (L x W): **130 x 5 cm²**
- 4 layers (signal , 2xGND, PWR): $X = 0.8\% X_0$
 - Cu : 12um thick per layer + 30 um Cu plating on surface
- Lines : **124 lines** (Line and space : 130 & 130 um)
- Z_{diff} : 100 Ω by strip line structure
 - Signal layer is sandwiched by GND layers
- Liquid Crystal Polymer (LCP) as substrate
 - Less signal loss due to low di-electric constant & $\tan(\delta)$
 - Thick LCP available for Z_{diff} : 100um



Signal lines based on ETROC2

- Size : 21x23mm² (Box shape) since 2D for the pixels
 - Bump bonding for pixel (CMS)

- Npads : 124 w/ wire bond

- CMS Digital lines: 13 lines
 - Tx: 2x DataOut (DS)
 - Rx: **CLK40 (DS)**
 - Rx: **FastCom (DS)**
 - Rx: **I2C (2 lines, SCK, SDA)**
 - Rx: **RSTn (1 line)**
 - Rx: I2C addr (5bits)
- Analog : 1 line (Vtemp)

ETROC for BTOF FPC

- BTOF FPC ~5 or 6 lines
- 1x DataOut (DS) = 2 lines
- **p2p = 2 lines**
- **bus w/ 4 chips (not p2p) = 2 / 4 lines**
- **bus w/ 17 chips = 2 / 17 lines**
- **bus for all chips = 1 / 34**
- 5 or 6 bits (depending on FPC conf.)
- **1 line**

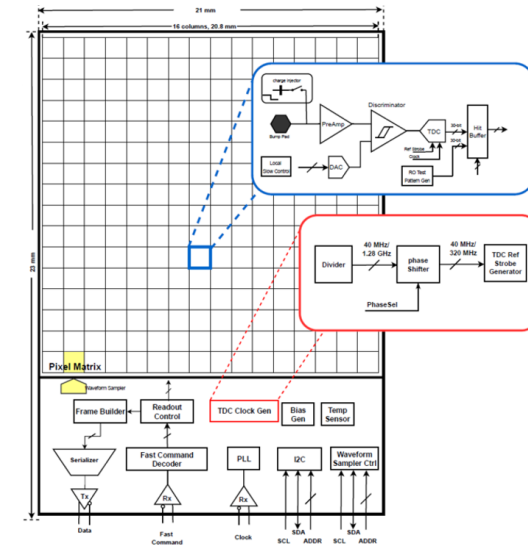
- 135 cm FPC = **33 or 34** ASICs/FPC (x2 FPC x 2cm/sens)

- **33 or 34** sensors are necessary

- If 34 ASIC's are in a FPC, $34 \times \{4 + 2/4 + 2/17 + 1/34 + 1\} = 194$ lines in total

- INTT: 124 lines w/ 3.5cm width (1.5 times more than INTT,)

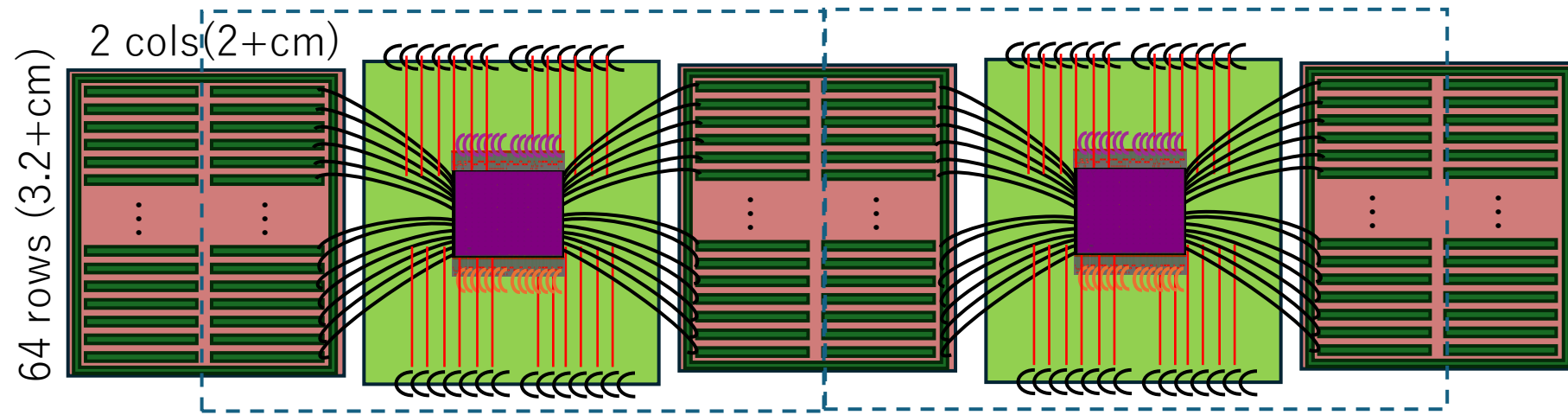
- If use INTT technology, Thickness is **~0.8 % X0 / FPC** **We use 2 FPC for a ladder ~ 1.6%**



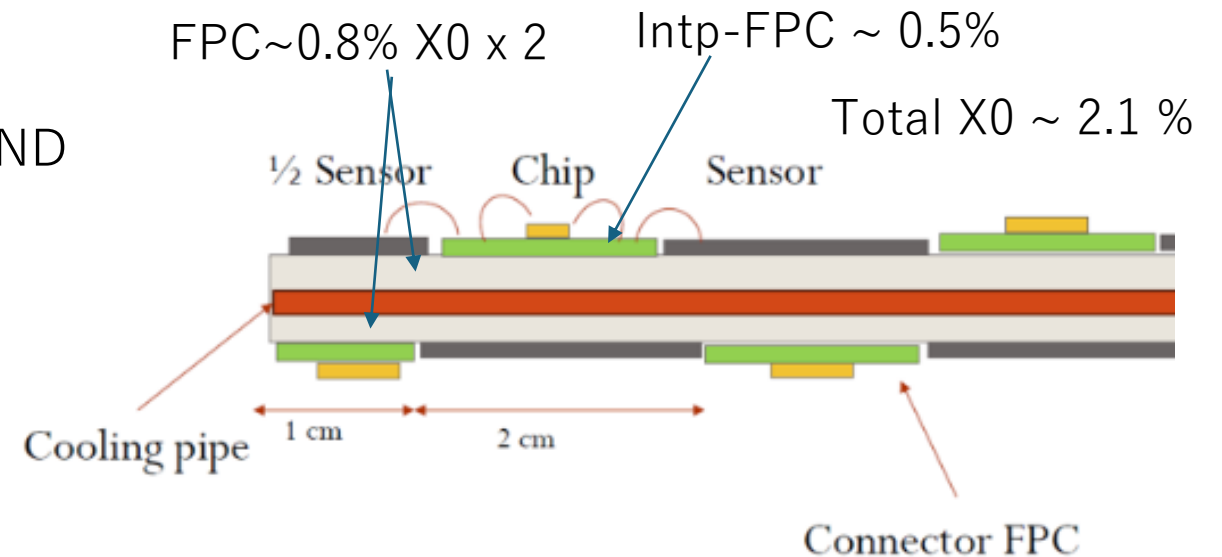
<https://etl-rb.docs.cern.ch/Specifications/etroc-test-card/#Specifications>

Sensor and ASIC Layout w/ interposer

ETROC (box)

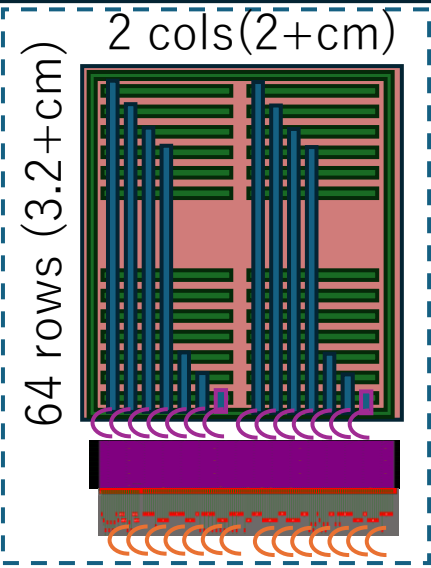


- Interposer FPC (green)
 - Routing signal lines from ASIC to FPC
 - Multiple (2~3) layers needed for DIO, power, GND
 - Additional thickness $>0.5\% X_0 \rightarrow \text{Total} \sim 2.1\% X_0$
 - Length of lines could be different
 - may get the time resolution worse
- Sensors & ASICs are connected
 - Difficult to make a (simple) module structure

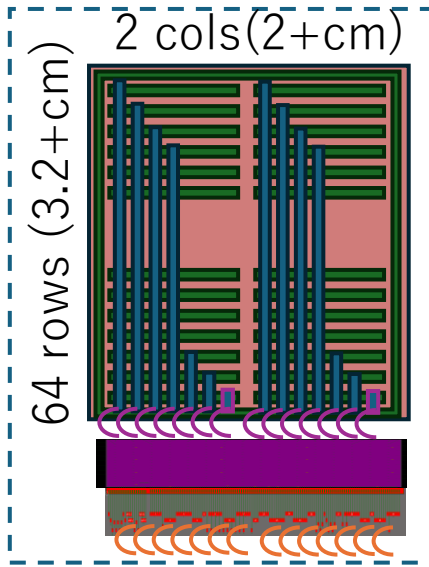


Option : Bottom layout of Sensor and ASIC

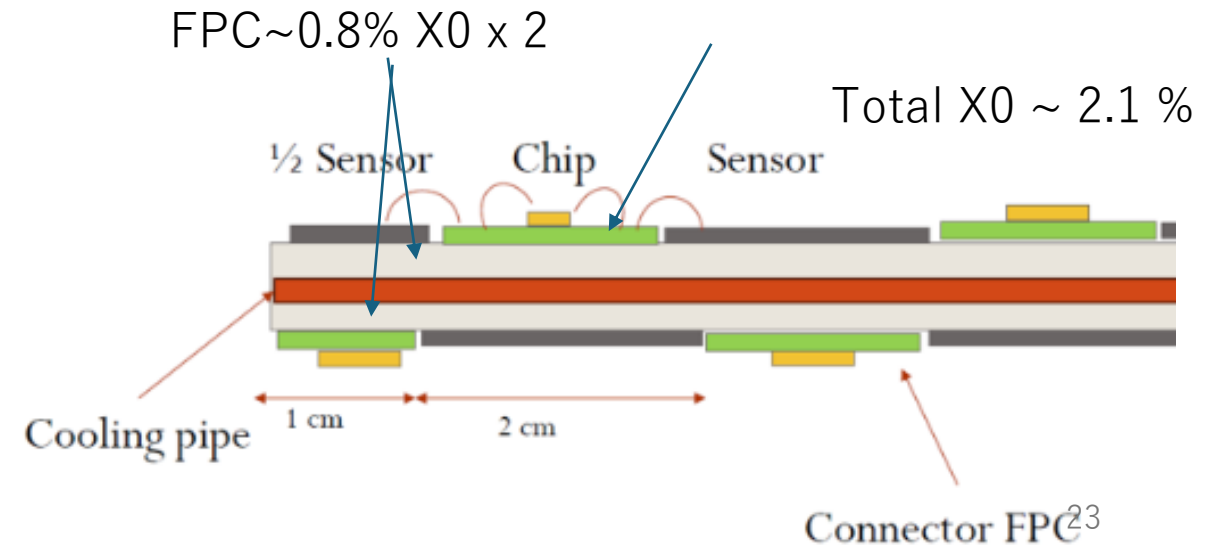
ASIC bottom placement



ASIC bottom placement



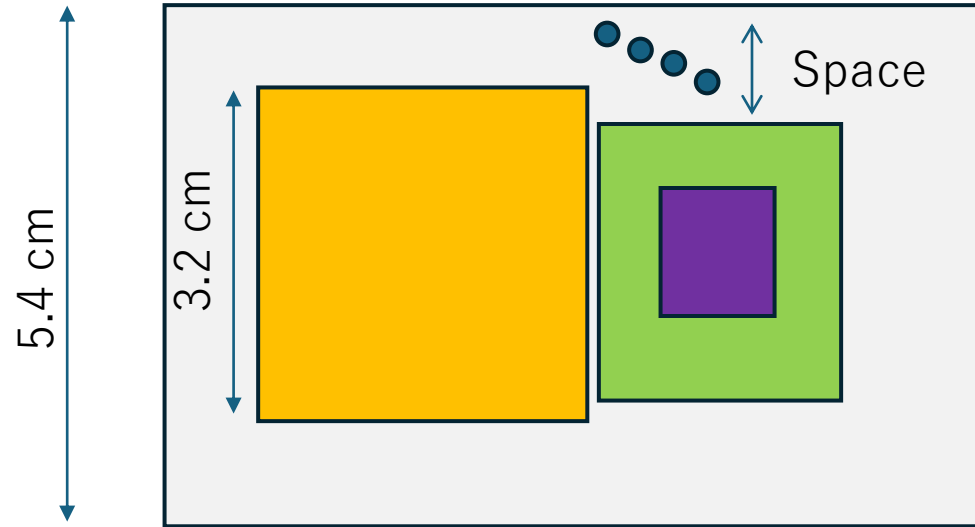
- ASIC at Bottom
 - Easy to make a module
 - Different lengths of double metal
 - Signal might be distorted
 - Simpler wire bonding
- If interposer, routing the lines get easier



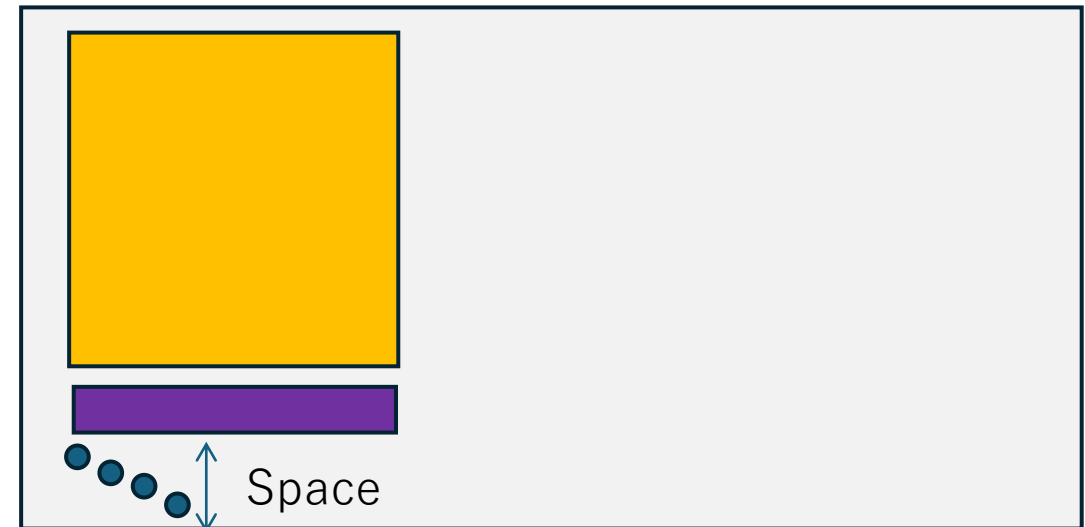
Space btw FPC and ASIC needed for wire bonding

Sensor + ASIC side by side

Thru-holes



Sensor + ASIC in top and bottom



- How much space is necessary to come out the signal lines from inner signal layer

Short FPC option

- Ladder : 135cm long with 34 sensors and 34 ASICs



- Minimize the additional connection
- Assembling this very long module is difficult
 - Yield rate will be issue during the production
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- 50cm FPC can be made with minimum risk in production
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Simone's slide in Nov. 2024

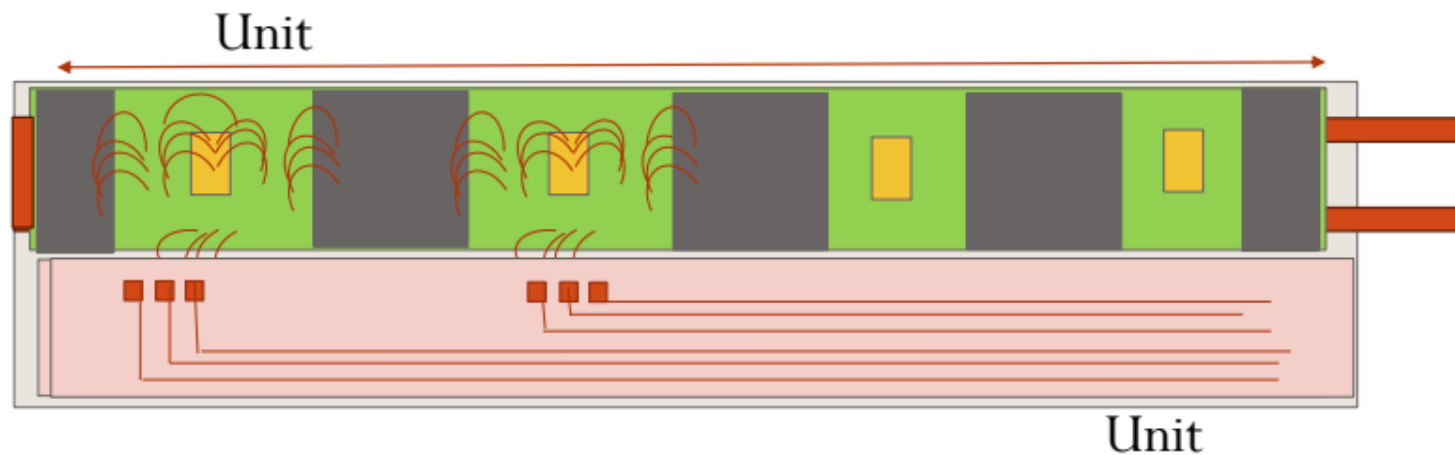
FPC idea

- FPCs are spTAB bonded to be extended so it's flush
- Flex are stacked and glued on the stave one on top of the
- Side view

The diagram illustrates the FPC idea. The top view shows a series of red squares (sensors) and green squares (ASICs) connected by lines, with a red line indicating the spTAB bonding. The side view shows the FPCs stacked on top of each other, with a red line indicating the bonding.

Double-sided stave

- Issue with small units: doubles the number of ASIC
 - If we do large units with half-sensors at the edges the number of ASICs would stay the same and it can be assembled 'stand-alone'
 - Demonstrator can be one unit length $\sim 16\text{cm}$



- Same number of ASIC but introduces small 'gaps' ($\sim 1\text{mm}$) between units
- Other stave side will have an ASIC in that position

