ePIC TOF Detector Design Documentation

Project: ***ePIC Forward Time-of-Flight (FTOF)***

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Contacts(s): M. Benoit, W. Li, M. Matveev, T. Ljubicic

Detector Envelope:

Latest detector envelope can be found at: link

The FTOF dimensions are:

- **Length**: 8 cm (from 185 cm to 193 cm in z from the interaction point)
- **Inner radius**: 10.5 cm
- **Outer radius**: 60 cm
- **Total area**: 1.096 m²

Sensor and ASICs:

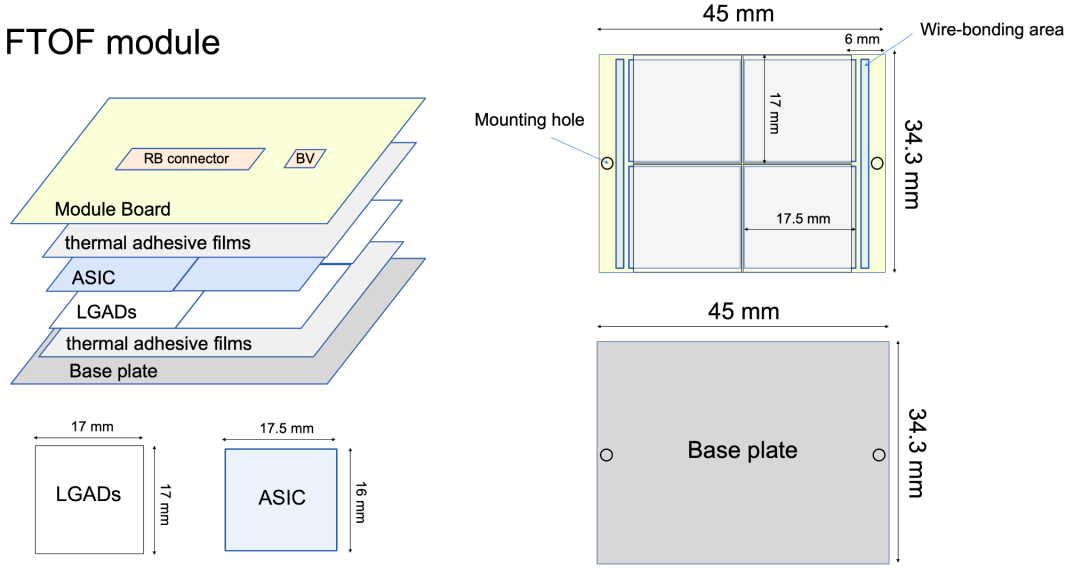
Sensor Specifications

- **Type:** Pixel AC-LGADs
- **Pixel Pitch:** 500 microns

- **Metal Electrode Size:** 50 microns
- **Active Area Thickness:** 20 microns (optimized for timing resolution)
- **Full-Size Sensor:** 1.7 × 1.7 cm²
    - 1.6 × 1.6 cm² with a 32 × 32 matrix of 0.5 × 0.5 mm² pixels
    - Additional 0.1 cm for guard ring (TBC)

ASIC Readout Chip

- **Type:** EICROC (same pitch as sensor)
- **Matrix:** 32 × 32
- **Capacitance Sensitivity:** 2 fC
- **Power Consumption:** 1.5 mW per channel
- **Jitter Target:** 20 ps
- **Full-Size Chip:** 1.75 × 1.6 cm²
    - 0.15 cm for series readout edge (TBC)



Module:

Each module consists of four full-size AC-LGAD sensors and EICROC chips, which are bump-bonded together. The conceptual design of the module is shown in the figure below. The module consists of the following components:

- **Module PCB Board:**

    - Dimension: ~ 0.6 mm in thickness, 45 x 34.3 mm^2 in area
    - A connector to the readout board for data transmission and a bias voltage connector for sensor biasing. Additionally, a wire-bonding area is available on the edge of the module board for connection with EICROCs.
    - Two mounting holes per module PCB
- **Thermal Adhesive Films:** Ensures stable thermal contact between components.
- **LGADs+EICROC Assemblies:** The core of the module where LGADs and ASICs are coupled.
- **Aluminum Nitride Base Plate:**
    - Dimension: ~ 0.5 mm in thickness, 45 x 34.3 mm^2 in area
    - Mechanical support and aiding in thermal management.
    - Two mounting holes per base plate

In the design shown below, the LGAD sensor is positioned at the bottom, closest to the cooling plate and mechanical structure for better temperature stability. The ASIC chip is placed on the top, even though it is the most power-consuming component. The order of ASIC and LGAD placement is still under R&D investigation. Each module includes two mounting holes for mechanical integration.

Service Hybrids and Powering Scheme

Service hybrids consist of two main components:

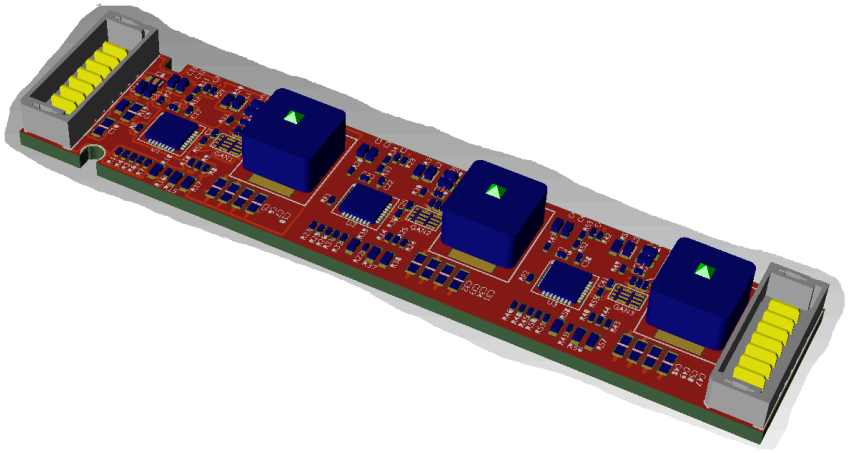
1. **Readout Board (RB)**: Each RB includes:
    a. **lpGBT** for high-speed data transmission.
    b. **VTRx+** optical transceiver.
    c. **MUX64 multiplexer** for monitoring.

Three types of RBs are envisioned: **RB3, RB6, and RB7**, serving **3, 6, and 7 modules**, respectively.

2. **Power Board (PB)**: Each PB consists of **three CERN bPOL48V DC-DC converters** to provide the necessary voltages for powering the RB and EICROC

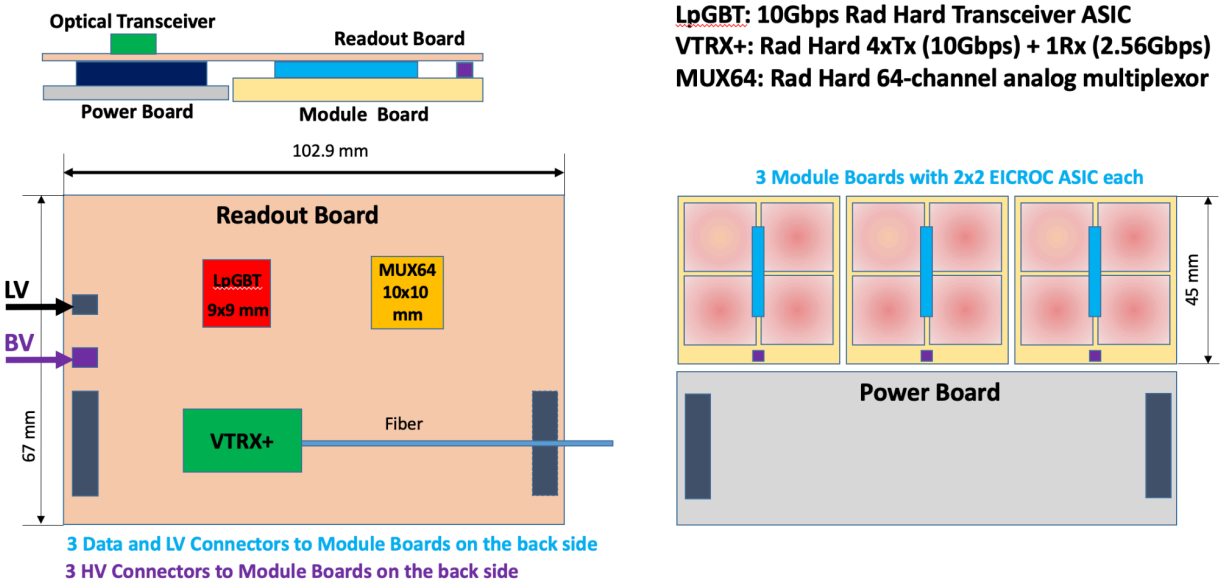
chips. The PB connects to the RB through board-to-board connectors. The following configurations are being considered:

a. **PB3**: Powers an RB3 setup (3 modules).
b. **PB6 and PB7**: Each 6-module and 7-module SH configuration will use **two PBs**.
c. **Alternative Option:** Instead of using multiple PB3s, separate PB6 and PB7 designs may be developed for better integration.

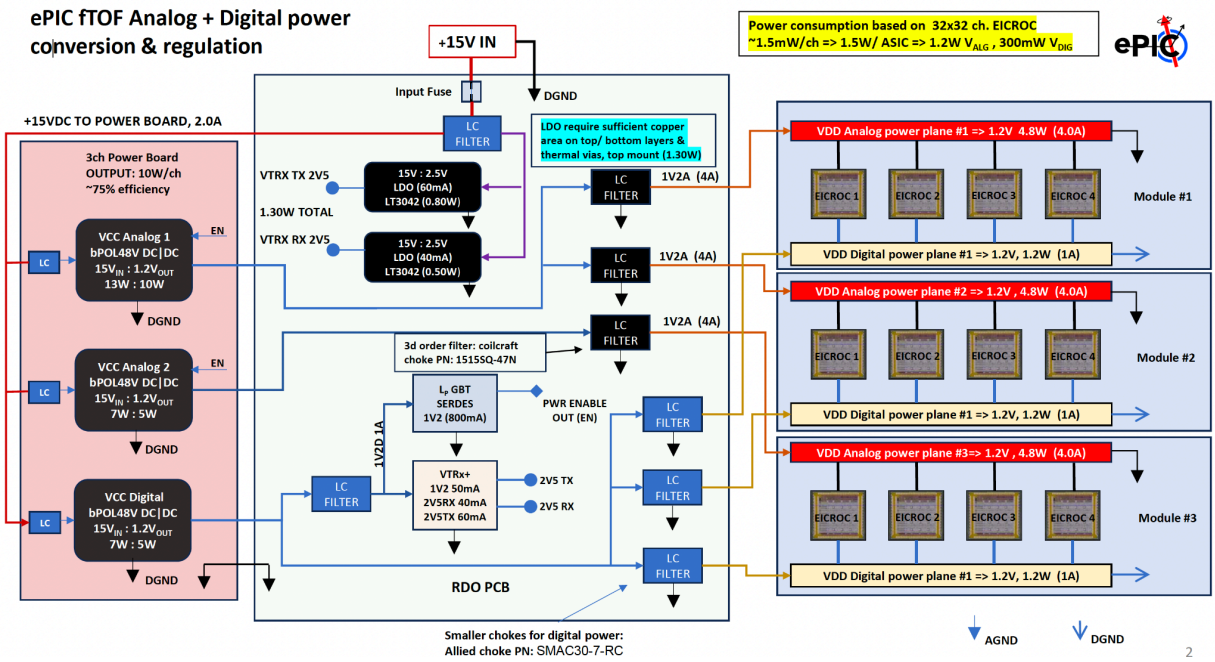


The figure below shows the design and dimensions of RB3 and PB3. The **PB is positioned at the bottom**, in direct contact with the cooling plate and mechanical structure, as it requires efficient cooling. The **RB is mounted on top** of the PB and module.

ETL FTOF Readout Board Prototype

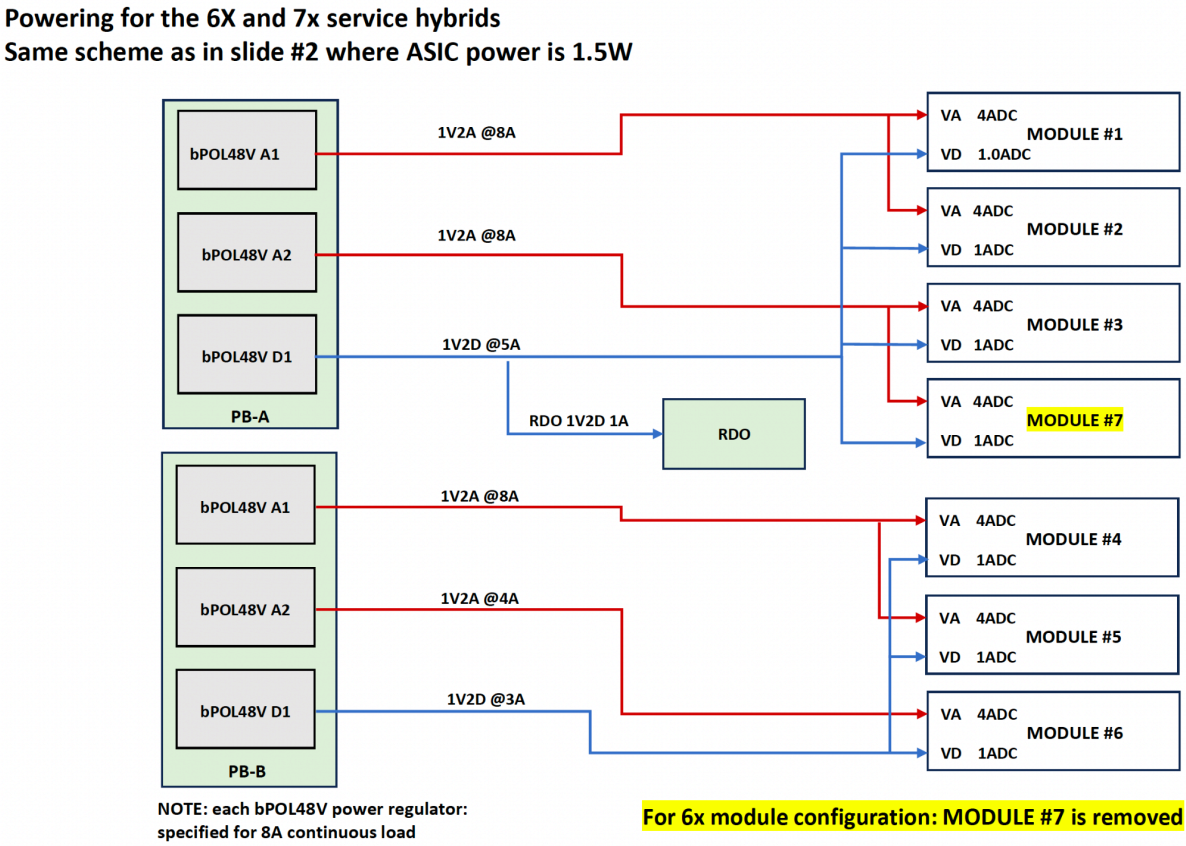


The detailed powering scheme of PB3, RB3 and 3 modules (or 12 EICROCs) is demonstrated in this picture (based on link). The total input power is 27W and output power is 20W, assuming ~75% efficiency. Two bPOL48Vs will output 1.2V and be dedicated to provide analogy powers to EICROCs, while the third bPOL48V will also output 1.2V and provide digital powers to EICROCs, as well as 1.2V to power lpGBT and VTRx+. The 2.5V needed to power VTRx+ will be provided through a linear convert on the RB



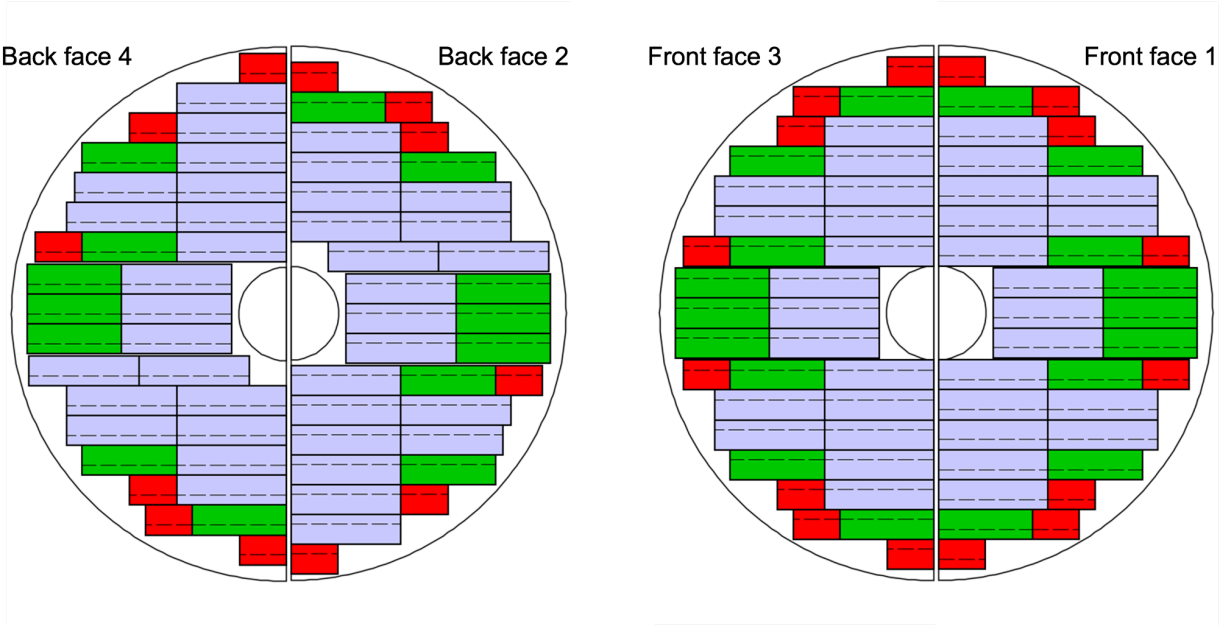
Schematics of the design of RB3v1 and PB3v1 serving 12 ASICs or 3 modules.

The powering schemes of PB6 and PB7 are demonstrated in the figure below:



Power scheme for RB6 and RB7, serving 6 and 7 modules

Detector Layout

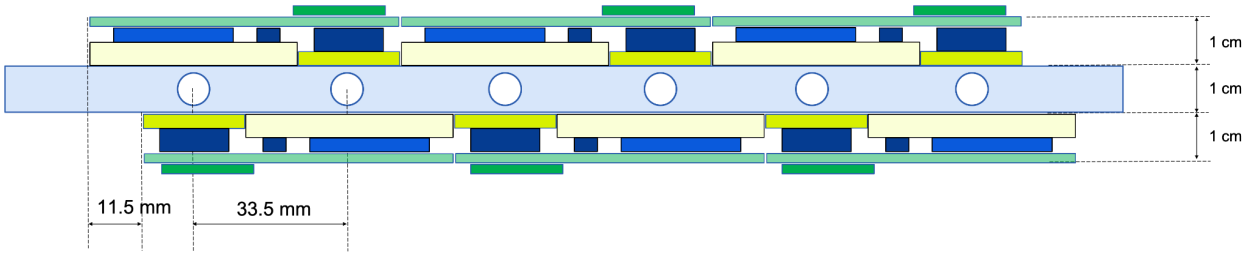


With these considerations in mind, we can populate the disk with the following numbers of each type of service hybrid as shown in Table 1.

Type	FACE 1 & 3	FACE 2 & 4	Total
3 module SH	8	6	28
6 module SH	9	8	34
7 module SH	17	18	70
Modules	197	192	**778**
Sensors	788	768	**3112**

Number of Service Hybrids (SH) and modules of the detector.

Material budget



To estimate the material budget, we consider the follow composition:

- Sensor: 300 microns (0.3%X0)
- ASICs: 400 microns (0.4%X0)
- RB and PB PCB board: 2 mm kapton (0.7%X0)
- Module PCB board: 0.6 mm kapton (0.2%X0)
- Aluminium nitride (AIN) base plate: 0.5mm (1.1%X0)
- Cooling and support: 5%X0 (TBC)

Total material budget is estimated to be: 7.7% X0

Power budget

This section summarizes the current estimate of the power budget. Please see the table below for a summary. Detailed basis of estimates are as follow:

- ASICs: 1.5mW/channel is assumed for EICROC as a conservative estimate (w/ 1mW/channel as the optimistic target). Each ASIC consists of 1,024 channels so each EICROC consumes 1.5 W. This power is distributed into analog (80%) and digital power (20%). For a total of 3112 ASICs, the total ASIC power consumption is about 4668 W.
- Sensor: leakage current of unirradiated sensors is < 20 nA/channel before breakdown (link). For a full-size sensor, the leakage current is less than 20 microA. Bias voltage before breakdown is about 100 V, leading to a power consumption per sensor of about 2mW. For a total of 3112 sensors, the total power consumption is about 6.2W.
- Power boards: in the current design of PB3, we assume 75% power efficiency with 27W input power and 20W output. Therefore, this leads to 7W heat

dissipation per PB3. Similarly, heat dissipation for PB6 and PB7 is 13W and 15W respectively. Based on the number of PB3/PB6/PB7 in the layout section, we can estimate the total heat dissipation for PB3, PB6 and PB7 to be 196W, 442W, and 1050W, respectively.

- Readout boards: on the readout board, we estimate 0.96W for lpGBT and 1.3W for VTRx+. This leads to a total of 303.6 W power consumption for a total of 132 readout boards.

Type	Quantity	Unit power consumption (W)	Total power consumption (W)
ASICs	3112	1.5	**4668**
Sensors	3112	0.002	**6.2**
PB3	28	7	196
PB6	34	13	442
PB7	70	15	1050
RB3	28	2.3	64.4
RB6	34	2.3	78.2
RB7	70	2.3	161
Service hybrids (RB+PB) total			**1991.6**
Grand total			**6666**

Power budget table

Power system (HV, LV) and data acquisition system (DAQ)

As we do not foresee the need of applying different voltages to different modules on the same SH, each SH will be served by one HV cable and one LV cable (there probably needs to be a return cable as well shared together by HV and LV as ETL). Cables will be connected through patch panels mounted on the rim of the FTOF disk. Each SH will have one data optical fiber cable. No patch panels on the FTOF disk for data fibers are currently planned.

Power supplies and backend DAQ to be completed later

Components	Total
HV cables	132
LV cables	132
Data fiber cables	132

Table 3. Number of cables

Common components needed

With the proposed layout above, the total number of ASIC components (mostly CERN ASICs) needed are summarized below. We assume 30% spare is needed.

Components	3 module	6 module	7 module	Total	Total w/ spare (30%)
lpGBT	1	1	1	132	172
LDO	2	2	2	264	344
MUX64	1	1	1	132	172
VTRx+ (5.5 cm pigtail)	1	1	1	132	172
bPOL48V	3	6	6	708	921

Table 1. Readout and power boards ASICs needs