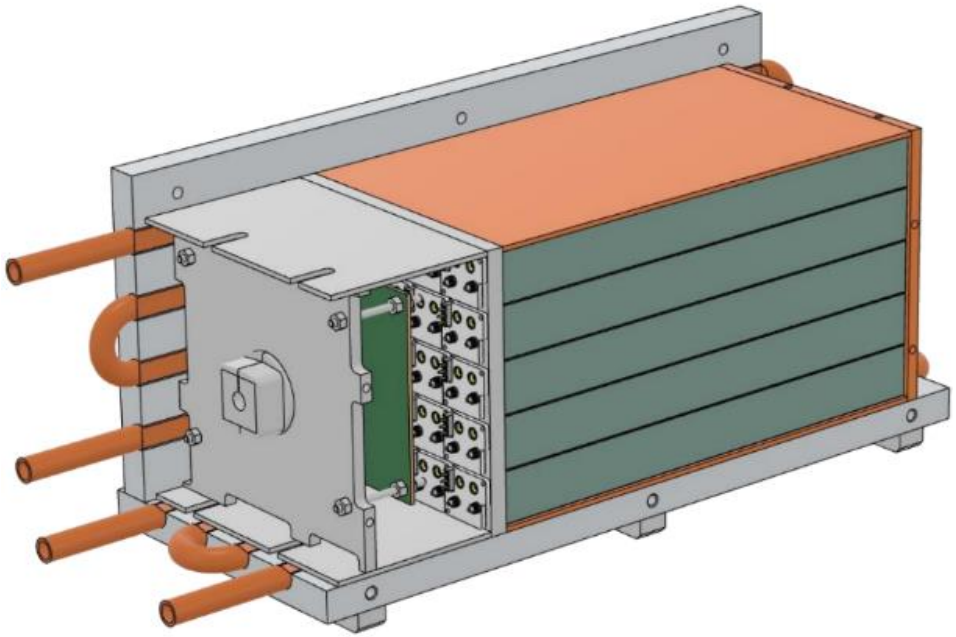


Backward ECal Test Beam

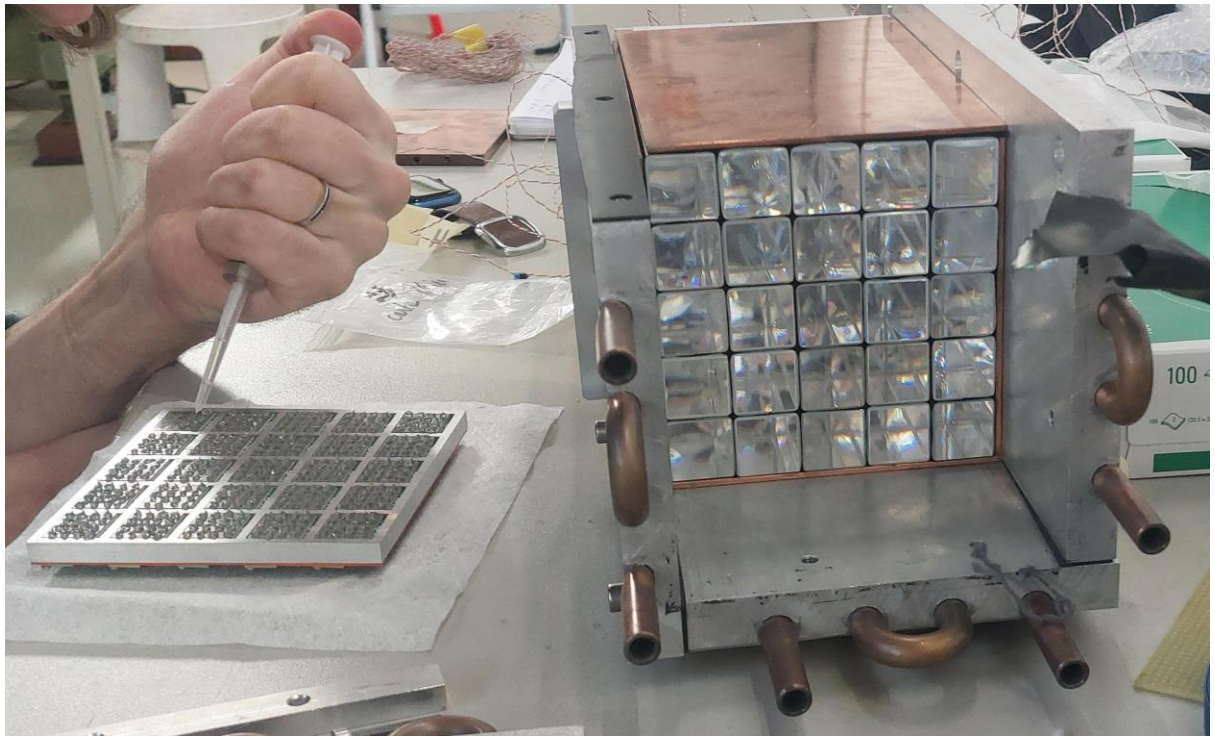
DESY, Feb 17 - Mar 2 (2025)

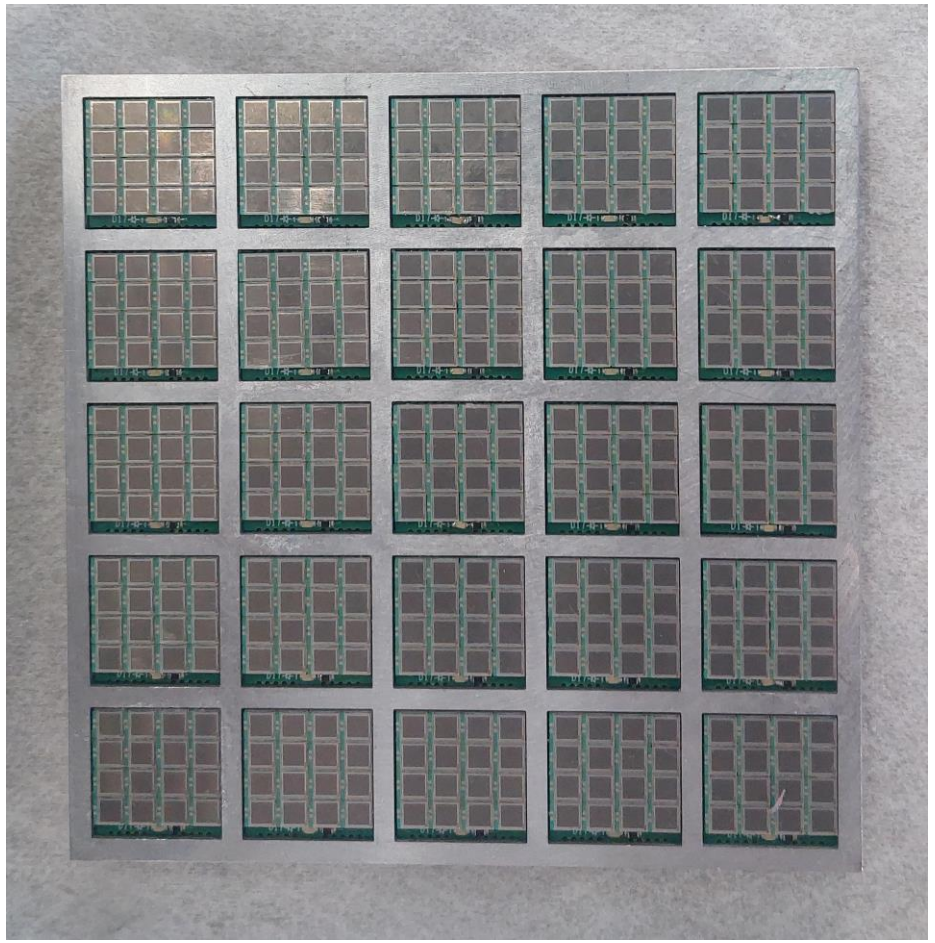
***Other DESY beam test:** March 28- April 7 (under analysis)
Upcoming *requested* dates (at DESY): Sep 29 - Oct 13 + Dec 1-15 (2025)

5x5 PWO prototype with 16 SiPMs per crystal

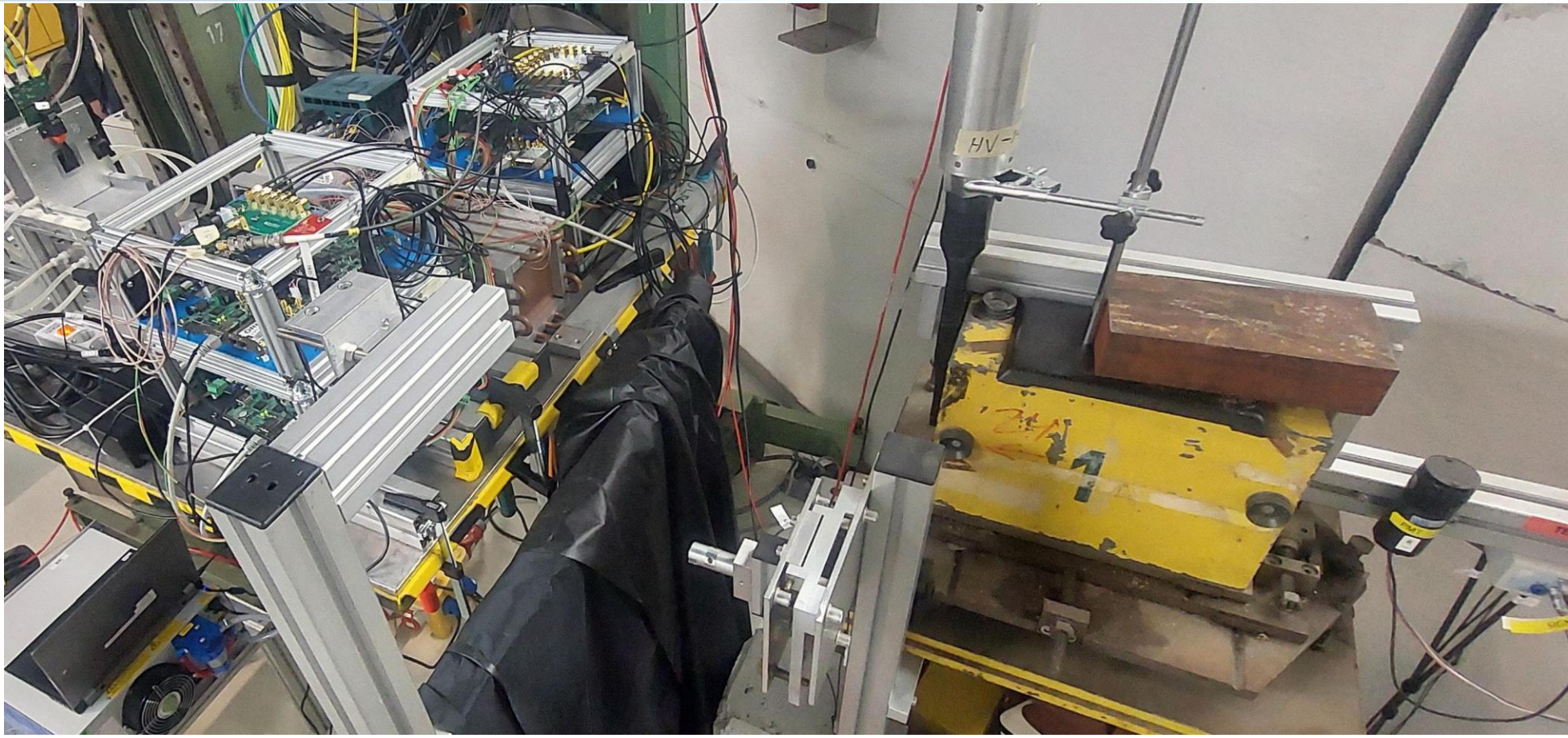
SiPMs: Hamamatsu S14160-3015PS
(3x3 mm^2; 15μm pixel size)

- 25 PWO crystals from CRYTUR
- SiPM readout
- Cooling and temp control



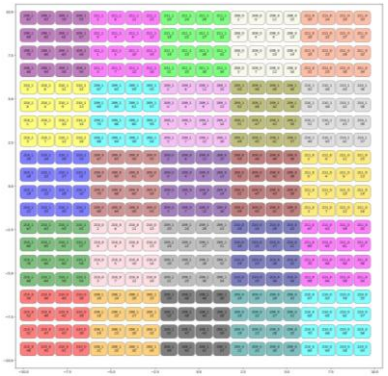


Setup at T24 in DESY test beam facility



- 1 – 5 GeV electron beam through a 2x2 mm^2 collimator
- Triggered by 2 scintillators
- Typical DAQ rates: ~50-100 Hz
- Prototype on a X-Y table with 0.1 mm position accuracy

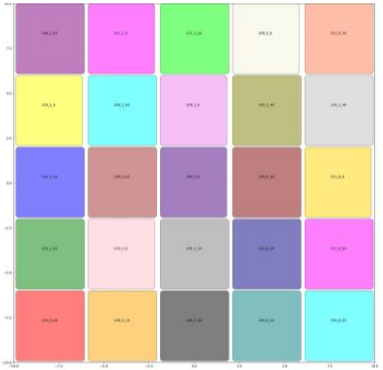
Readout options tested



- Each SiPM individually
- 400 channels
- 530 pF per channel

- SiPMs grouped by 4 in a crystal
- 100 channels
- 2120 pF per channel

- All 16 SiPM in a crystal read in parallel
- 25 channels
- 8480 pF per channel



- All 16 SiPM in a crystal read in parallel
- 25 channels
- 8480 pF per channel

+ Readout with H2GCROC3b chip

+ preamp board &
CAEN V1725S 14-bit 250MS/s digitizers

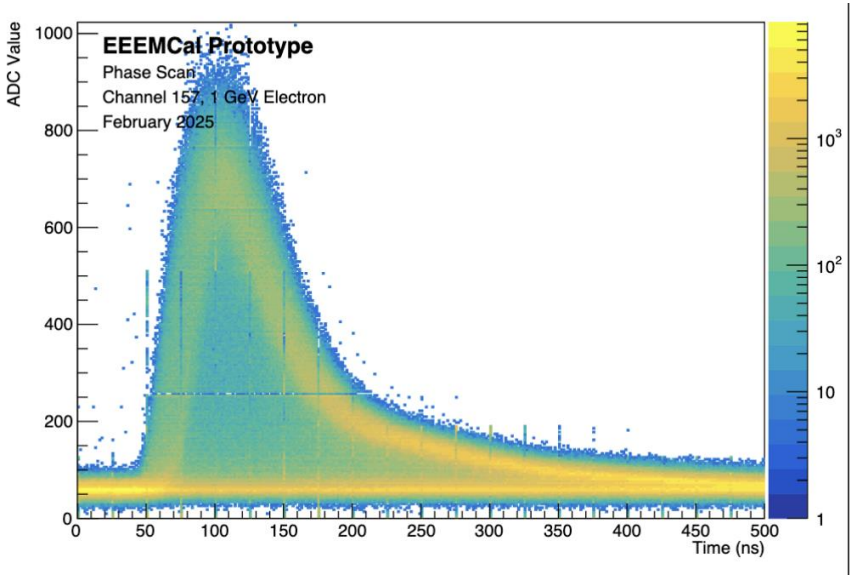
Beam test run plan

- Gain matching runs: runs centered at each of the 25 crystals
- Energy scans: beam at the central crystals and energy ranging from 1 to 5 GeV
- Position scans: beam across crystals at 4 mm steps

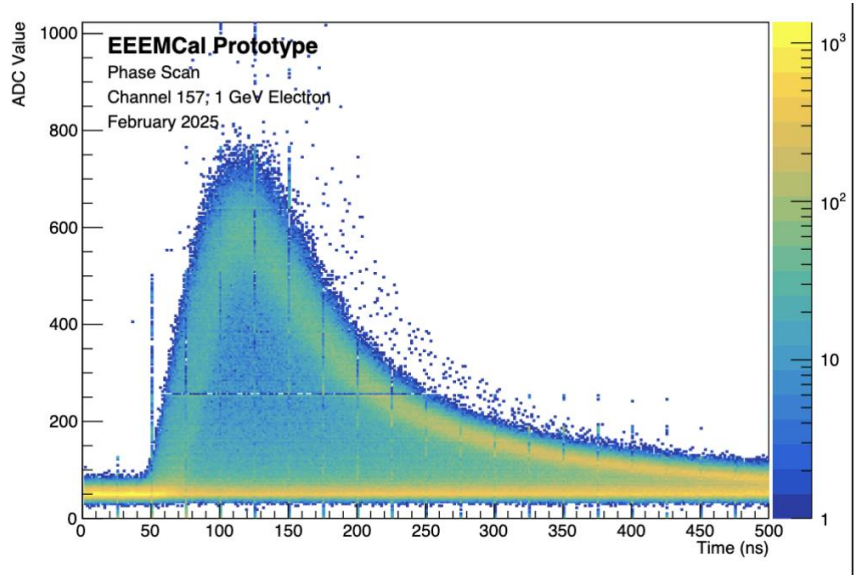
- Typically ran ~2 days for each of the readout configurations (after some debugging and commissioning)
- Analysis ongoing
- Results expected in ~ 6 weeks.

SiPM signal shapes

16-independent readout



4x4 readout



16-parallel readout

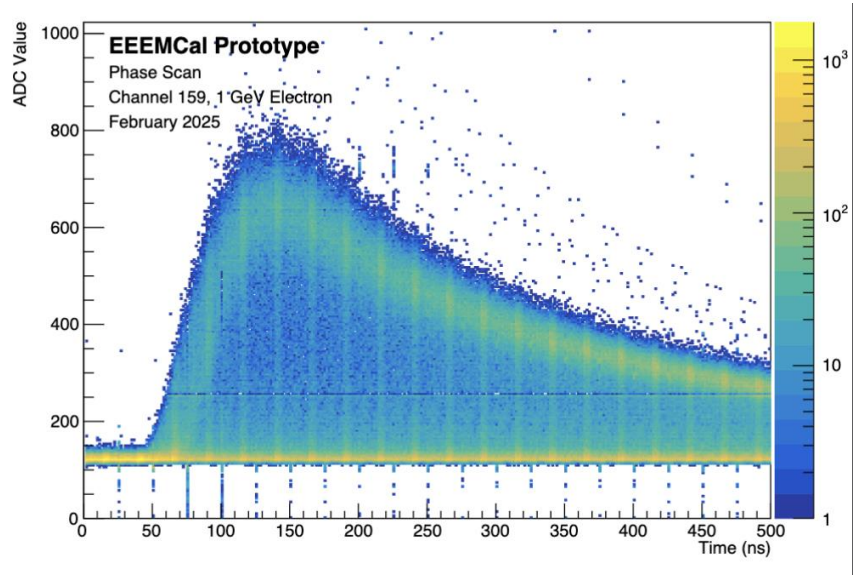
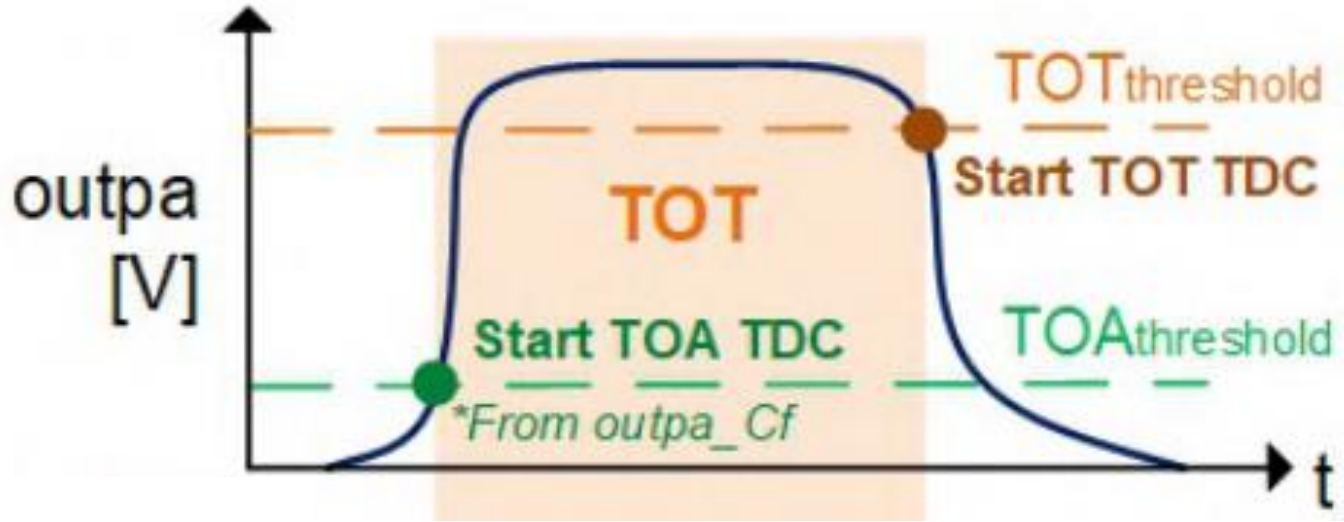


Figure 22: Waveform measured in a phase scan for each of the different daughther boards: all independent (left), 4×4 (center) and all parallel (right). The value of Rf is 1100 (6.7 KOhm). The current conveyor gain is 0.3 (left), 0.1 (center) and 0.05 (right).

ADC vs TOT

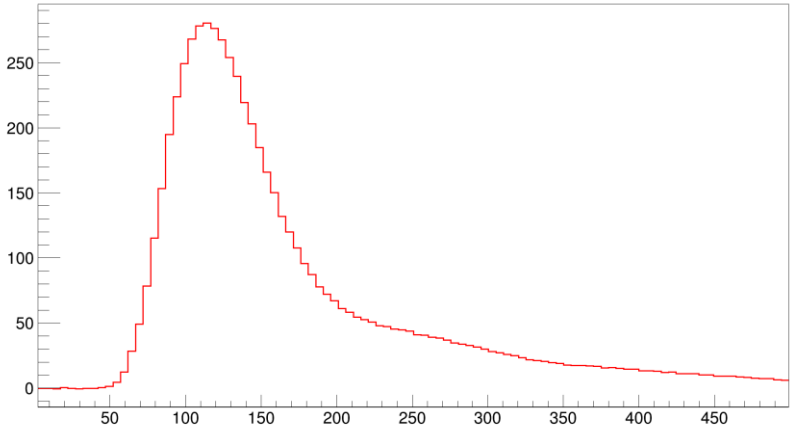
Energy measurement by a combination of a:

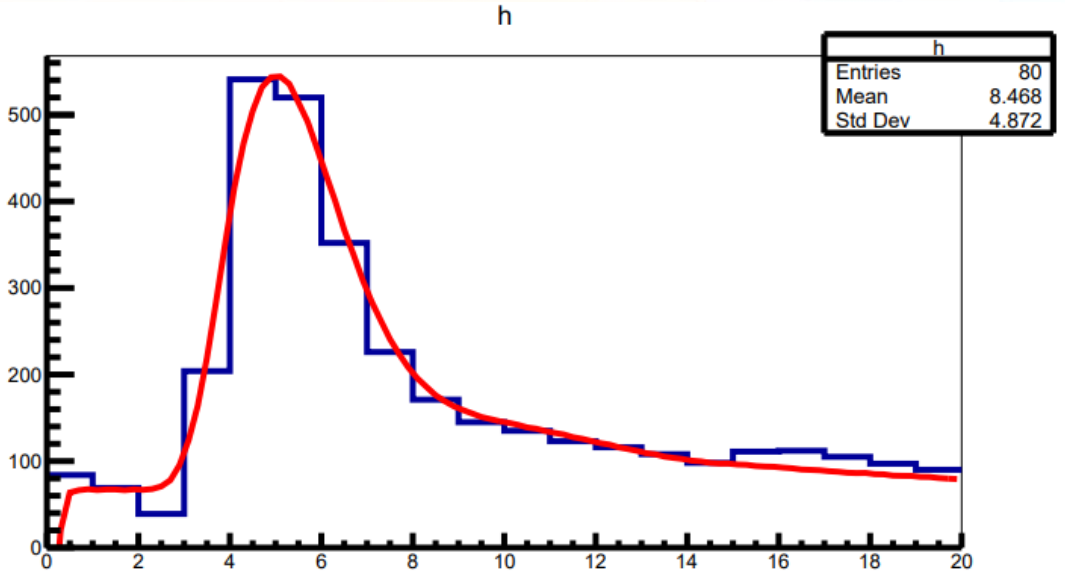
- 10-bit ADC (for small signals) and a
- 12-bit TDC (for large signals)

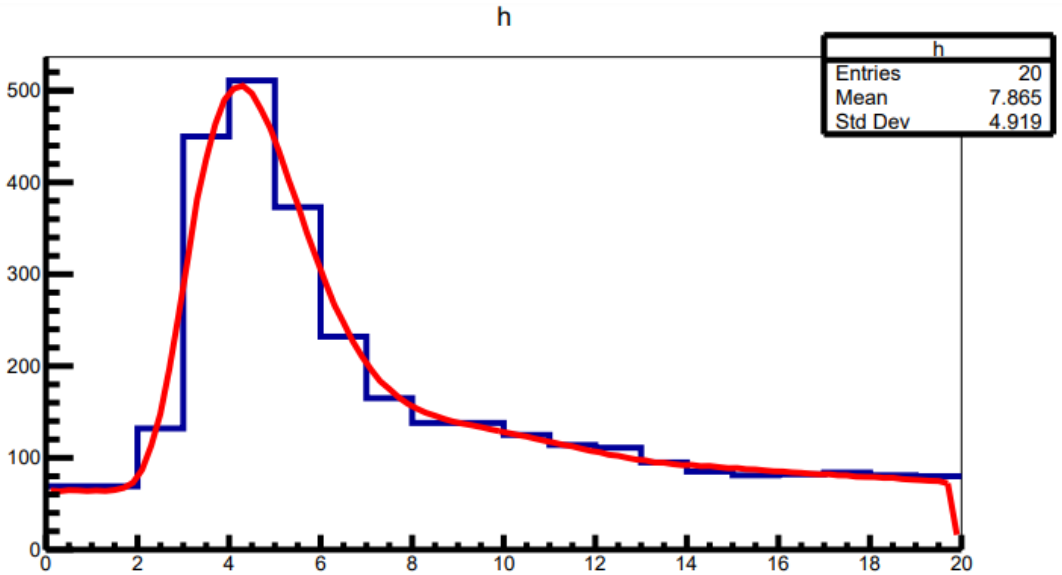


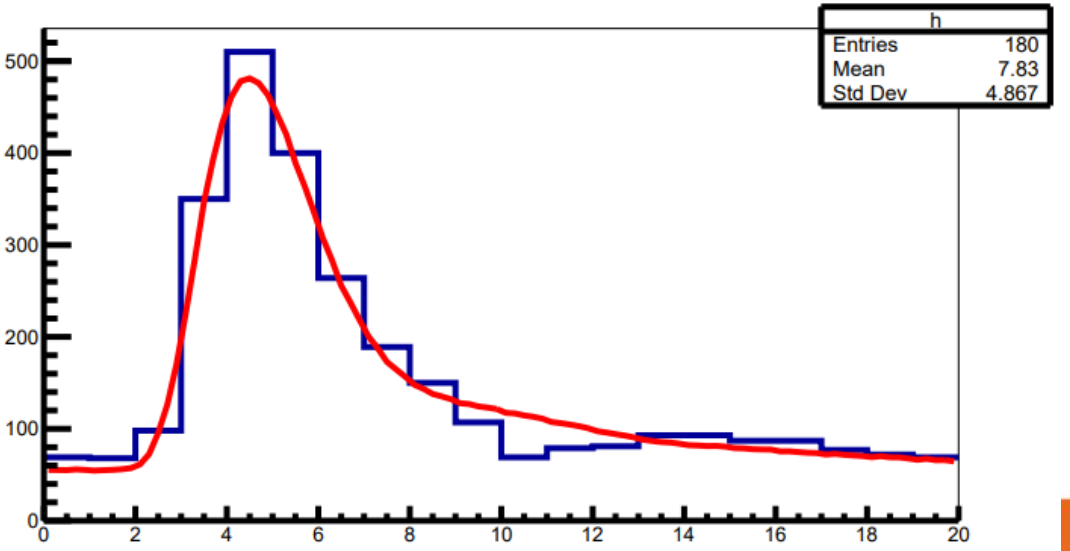
Waveform fits

Reference shape for the fits



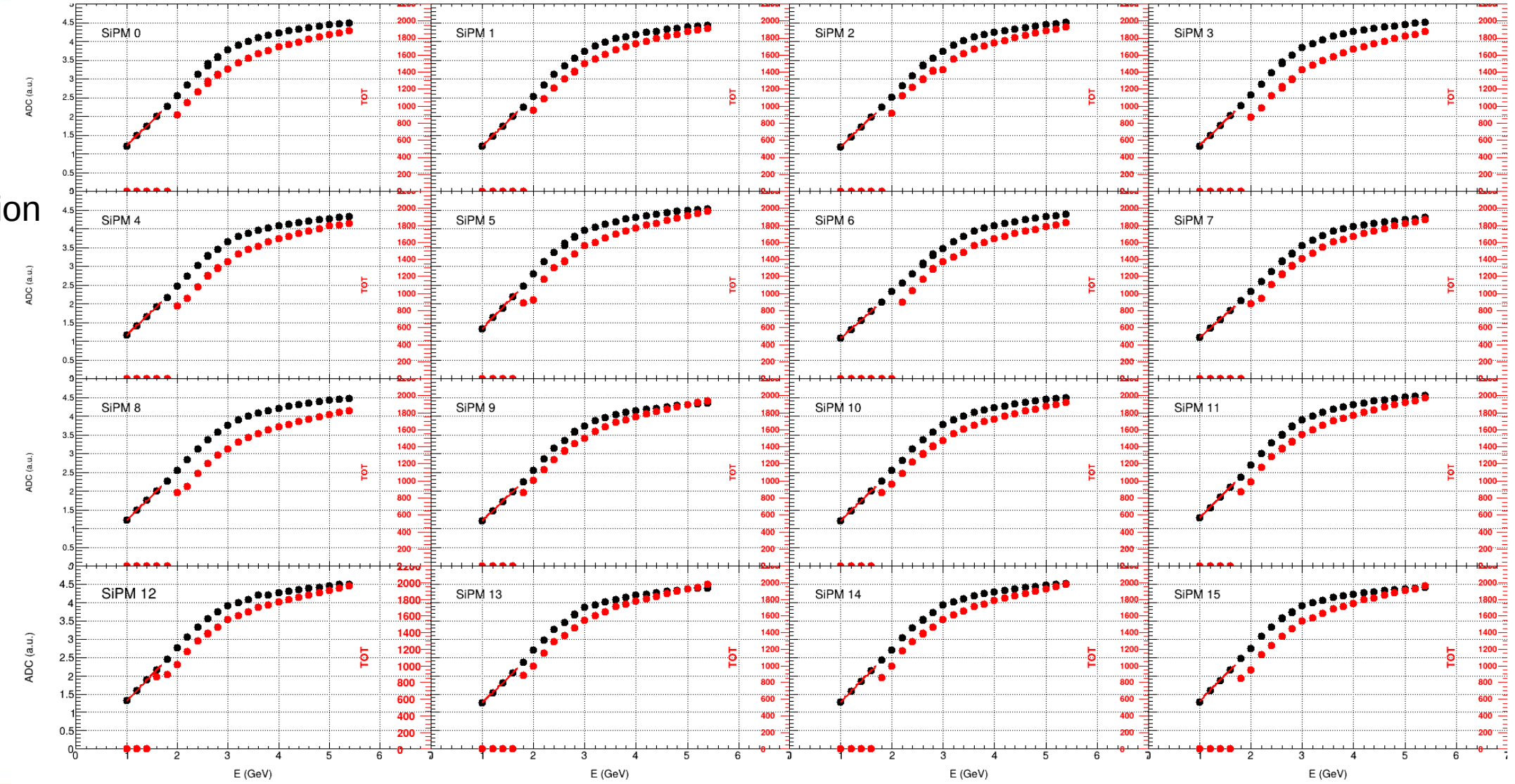




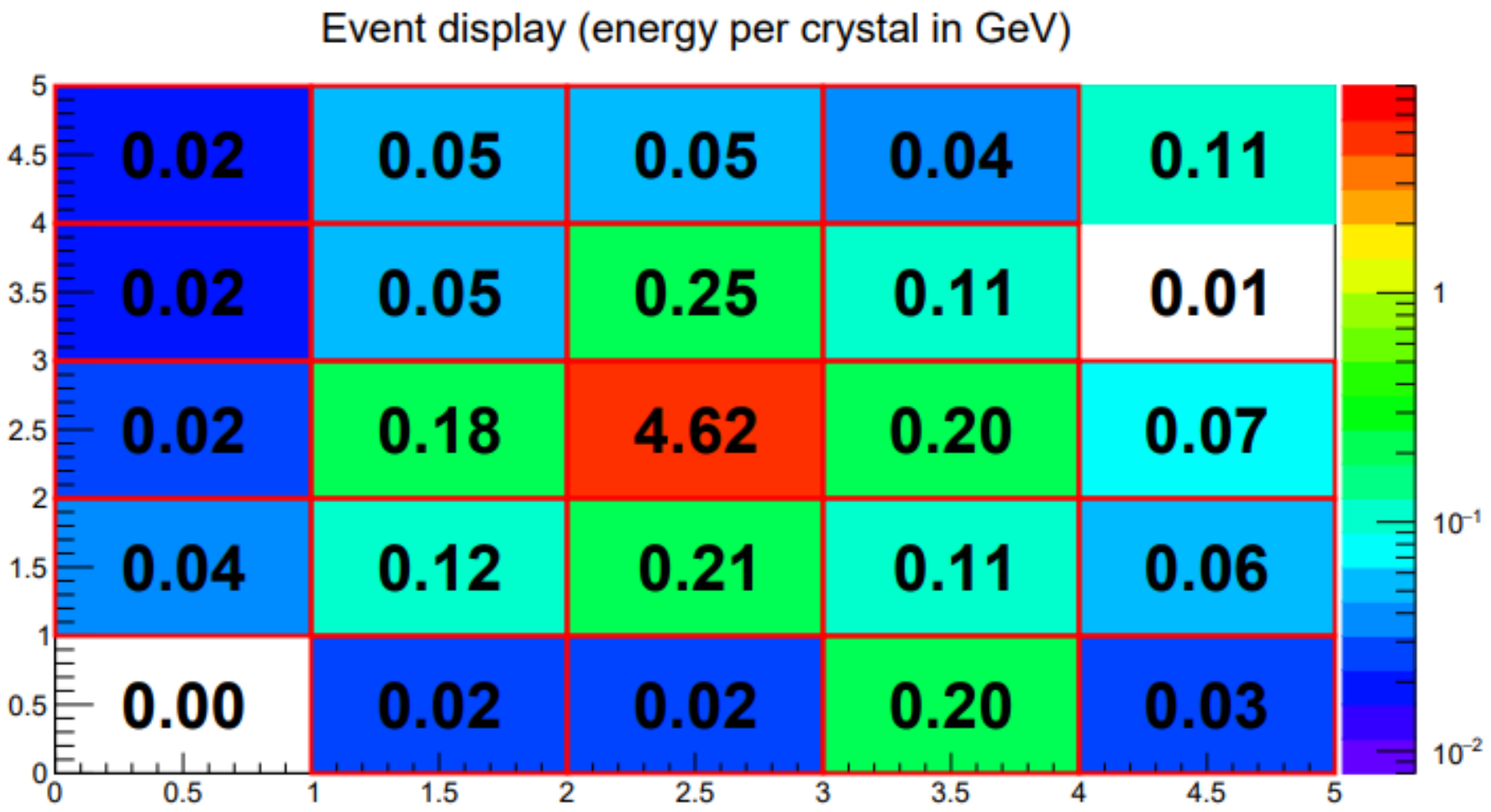


Energy scan: ADC and TOT

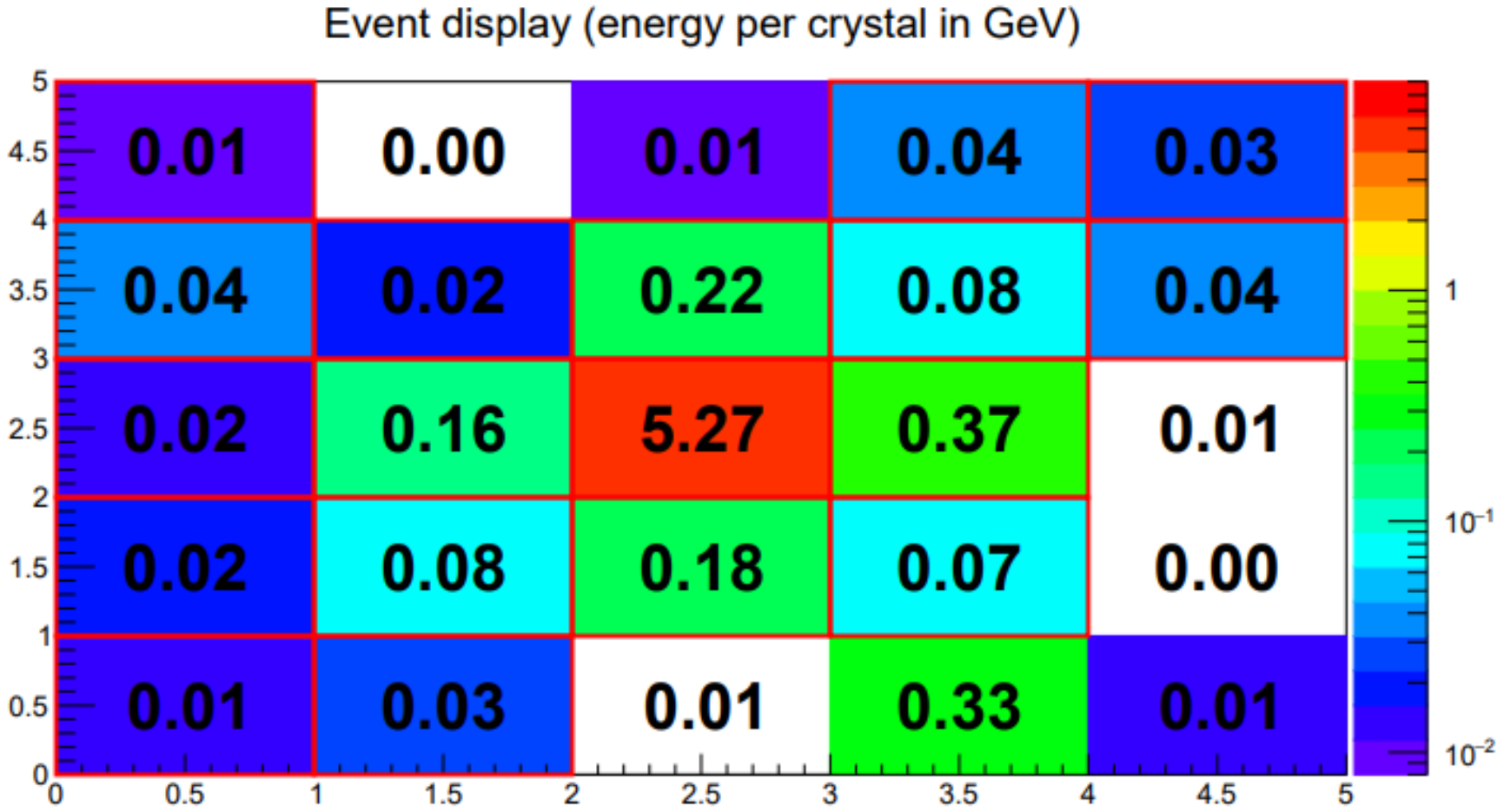
- ADC is linear before saturation
- TOT needs correction for non-linearity



Sample event at 5 GeV



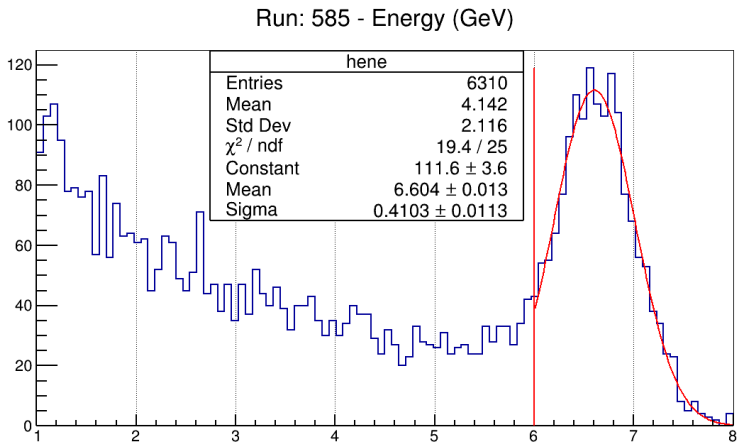
Another event at 5 GeV

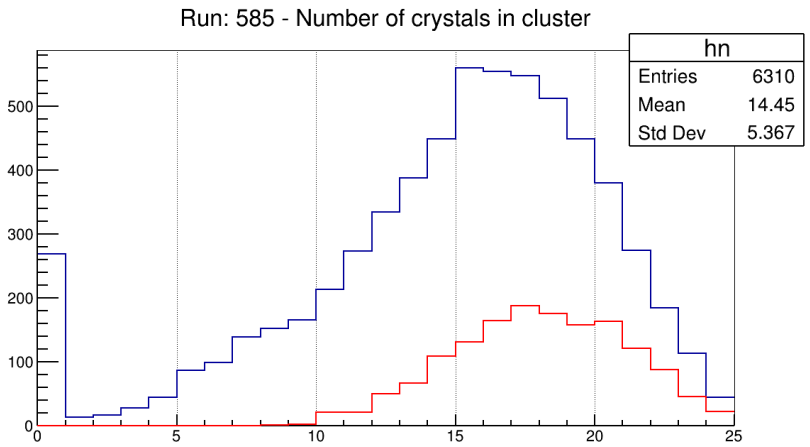


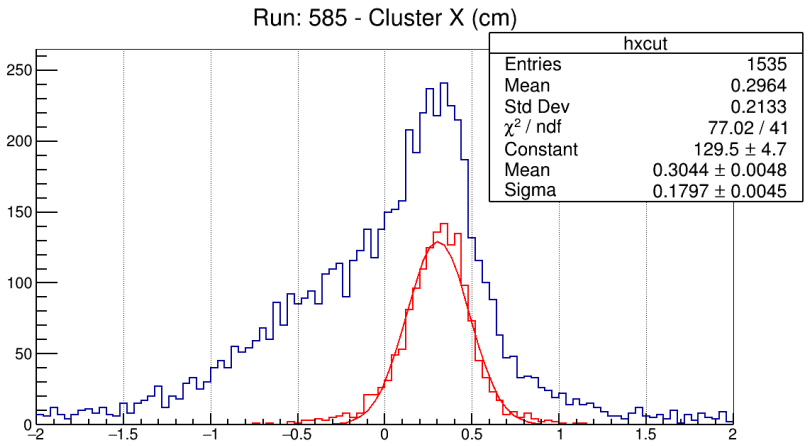
5 GeV run

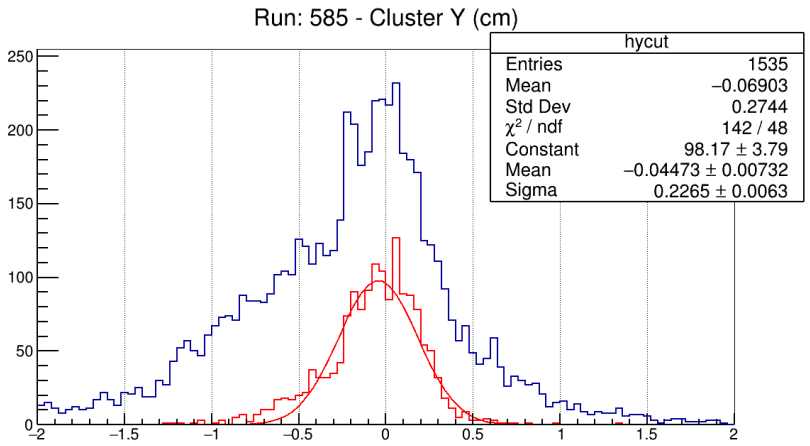
6.2% energy resolution

Still far from goal: ~2%

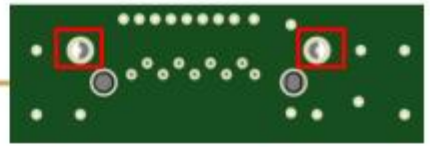






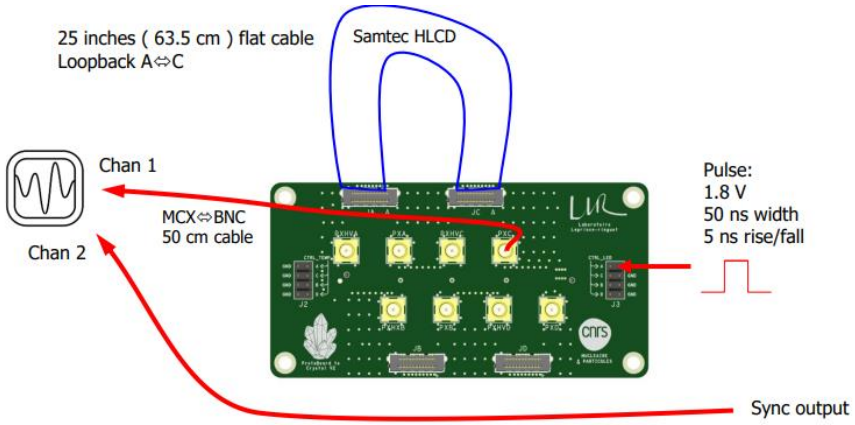


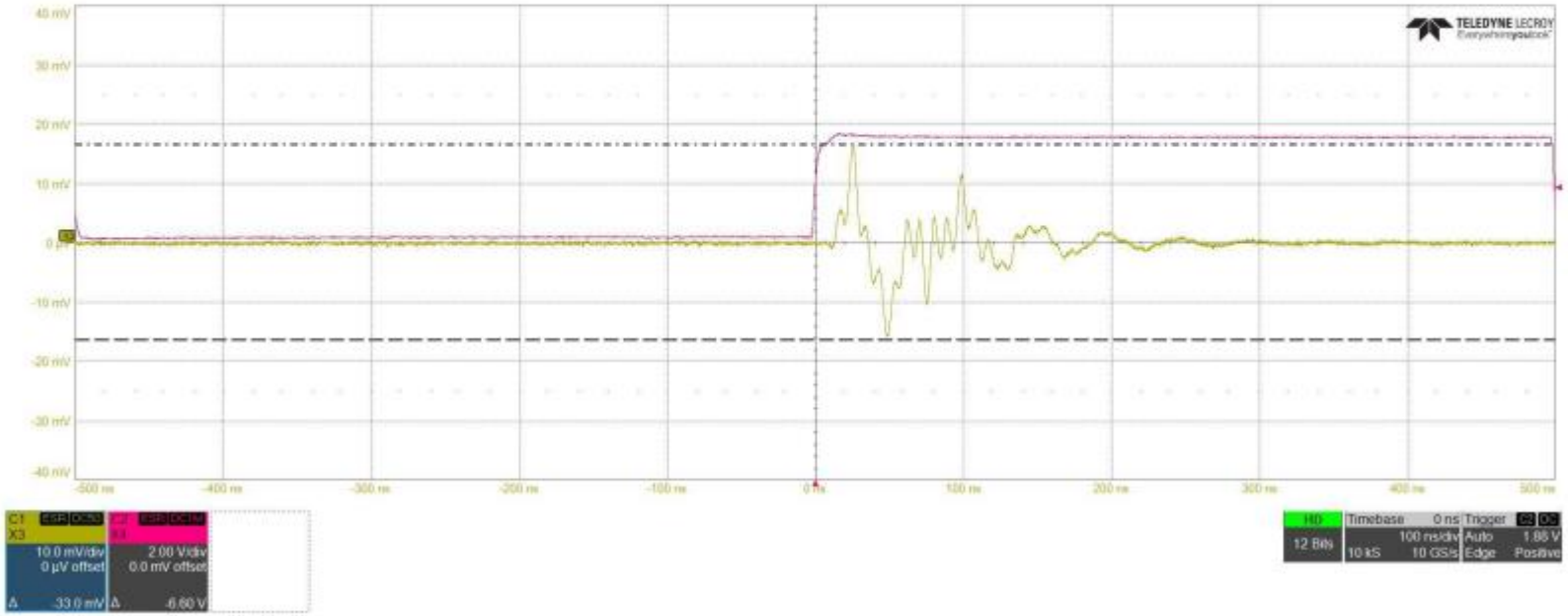
Initial Scheme (cf p.5)



No GND connection of the flat cable connectors pins (floating shields)

=> The amplitude of the spikes significantly varies when moving the cable. Here, "best" case (~33mV pp)



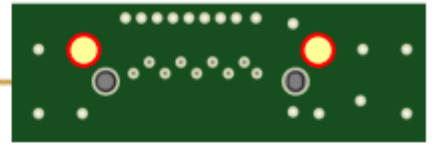


Signal Trigger

O. Le Dortz / LLR

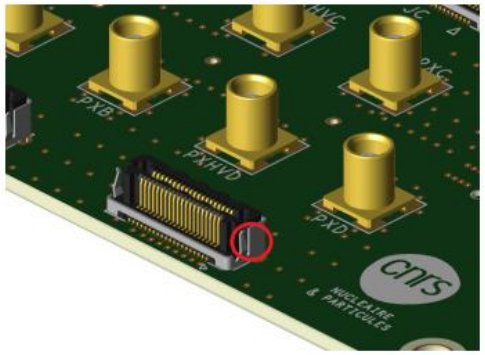
25 April 2025

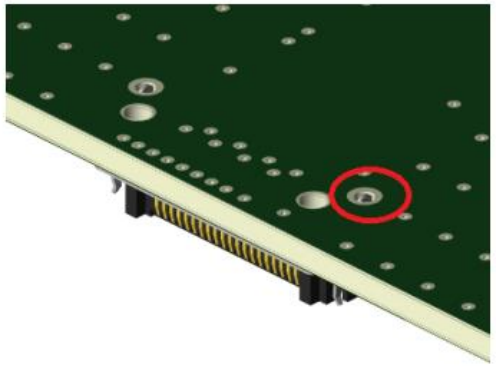
After shield pins soldering

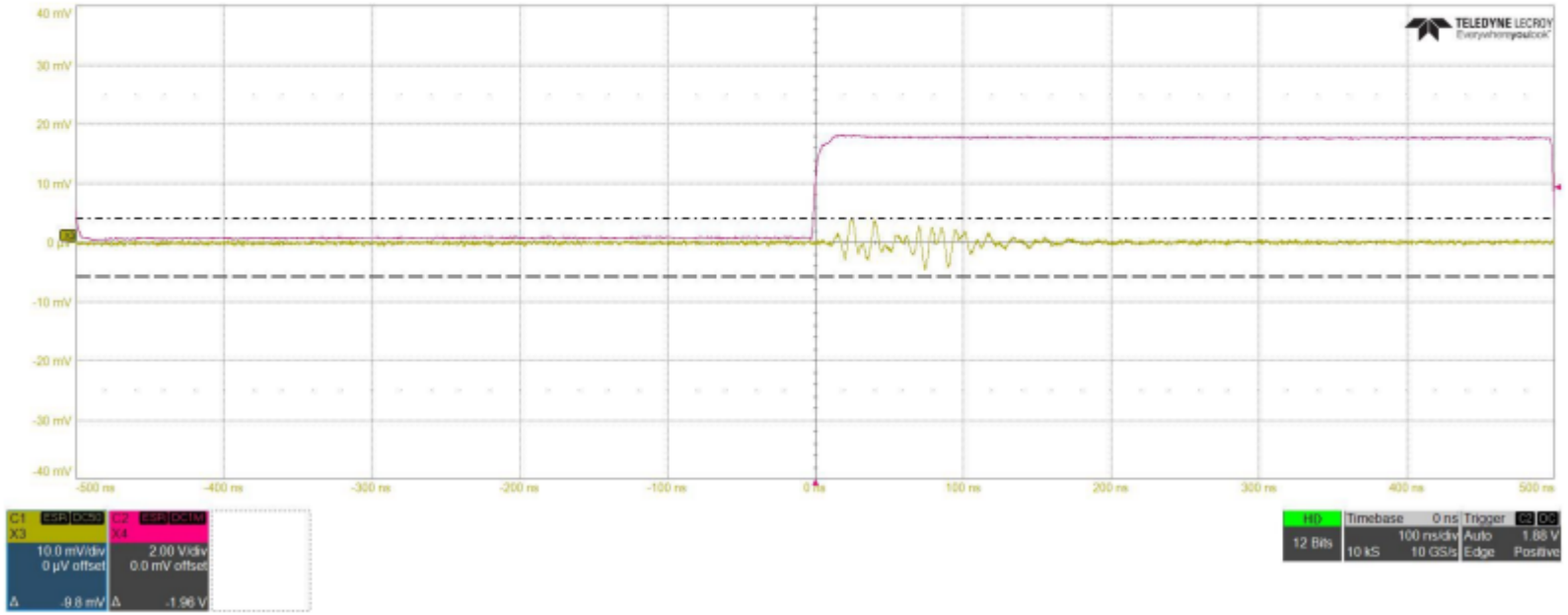


Noticeable reduction of the spikes amplitude (~10mV pp)

Conclusion: soldering the 2 GND pins on each connector **recommended** (if not already done)!







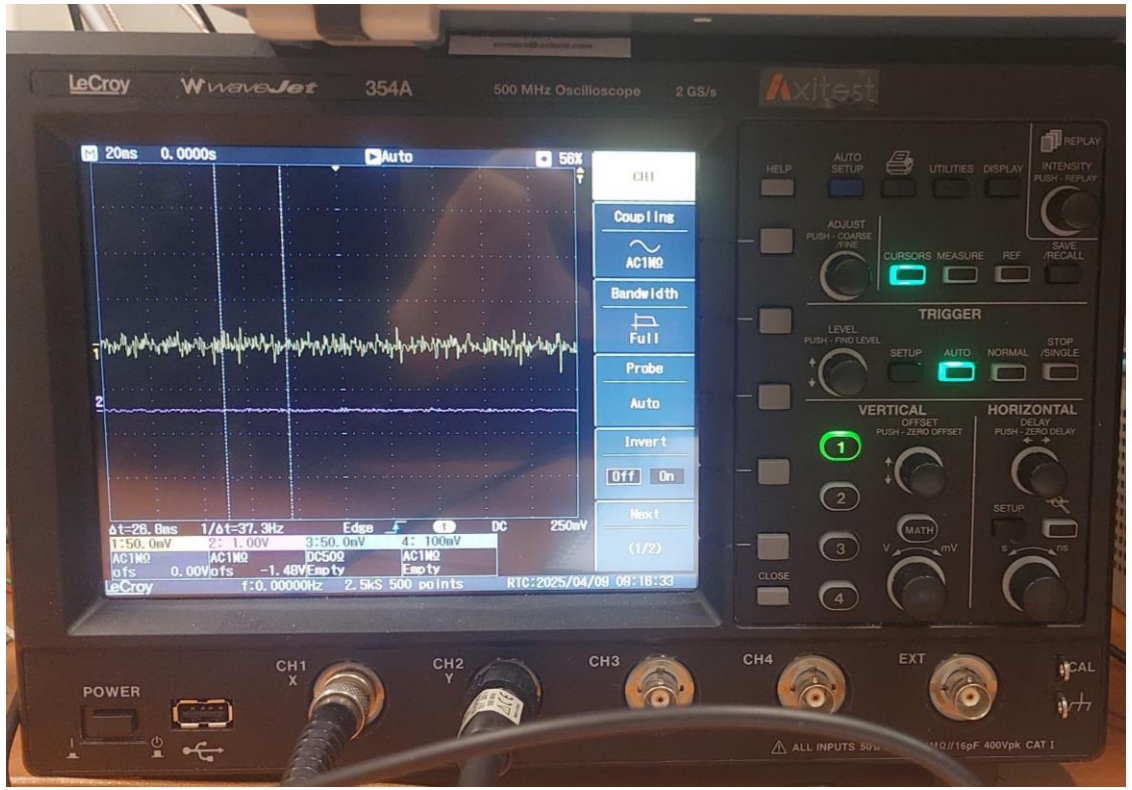
Signal Trigger

O. Le Dortz / LLR

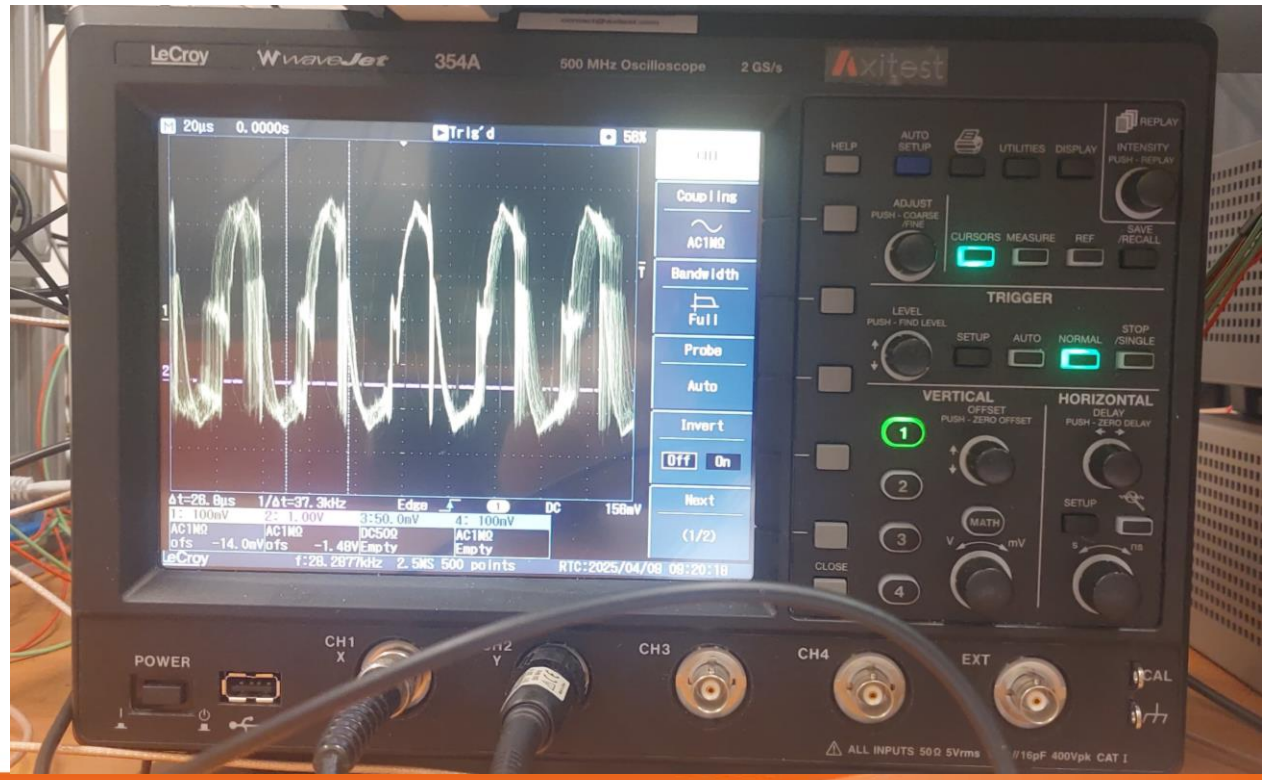
25 April 2025

Stability of the bias voltage supply

- HGCROC boards (aka protoboards) connected, a large oscillation in the power supply is observed (400 mV peak-to-peak, ~37kHz)
- This affects all SiPMs, as the power supply is common
- This *should* not happen in the discrete readout at DESY



HGCROC boards disconnected



Summary and outlook

- Analysis still ongoing
  - Channel-by-channel ref shapes
  - Better calibration of individual channels
  - Mask (and correct for) bad/dead channels

- Investigation on different sources of background and fluctuations

(Power supply, HGCROC boards, light leaks…)

The team

J. Bettane[1], E. Cline[8,9], J. Crafts[10], V. Chaumat[1], M. Czeller[4], C. Delafosse[1], P. Dinaucourt[6], C. Domingues Goncalves[1], F. Dulucq[6], P. Dumas Ziehlmann[6], R.H. Fatemi[14], J. Frantz[13], B. Geoffroy[1], A. Hoghmrtsyan[15], C. de La Taille[6], O. Le Dortz[5], N. Gabor[4], D.K. Hasell[8], T. Horn[10,16], M. Imre[1], L.D. Isenhower[12], S. Jia[7], B. Mathon[1], H. Mkrtchyan[15], A. Migayron[1], R.G. Milner[8], C. Muñoz Camacho[1], M. Nguyen[5], T. Nguyen Trung[1], N. Novitzky[3], S. Obraztsov[5], S. Olmo[1], T. Protzman[2], R. Reed[2], A. Shatat[5], D. Thienpont[6], G. Visser[11]