



INTT Overflow Flag Analysis

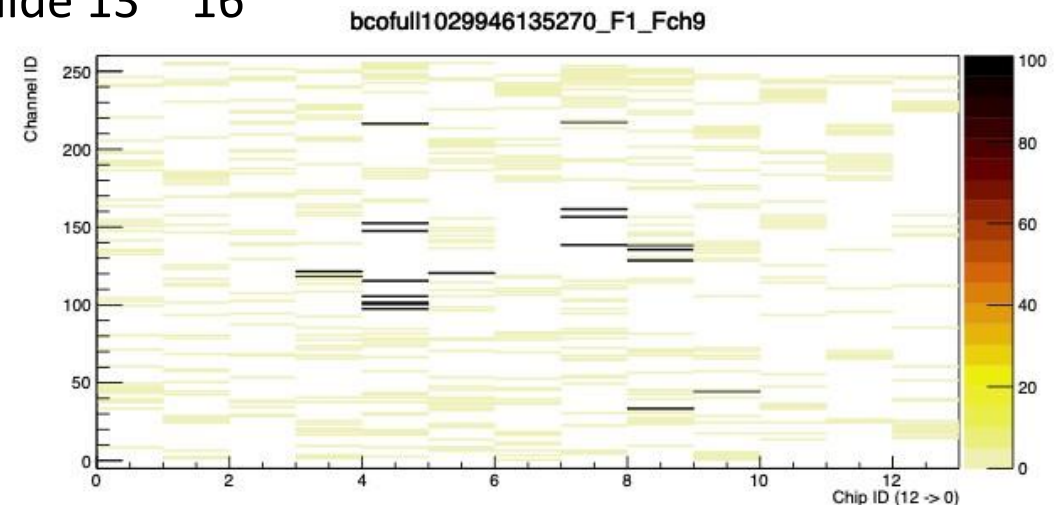
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Overview

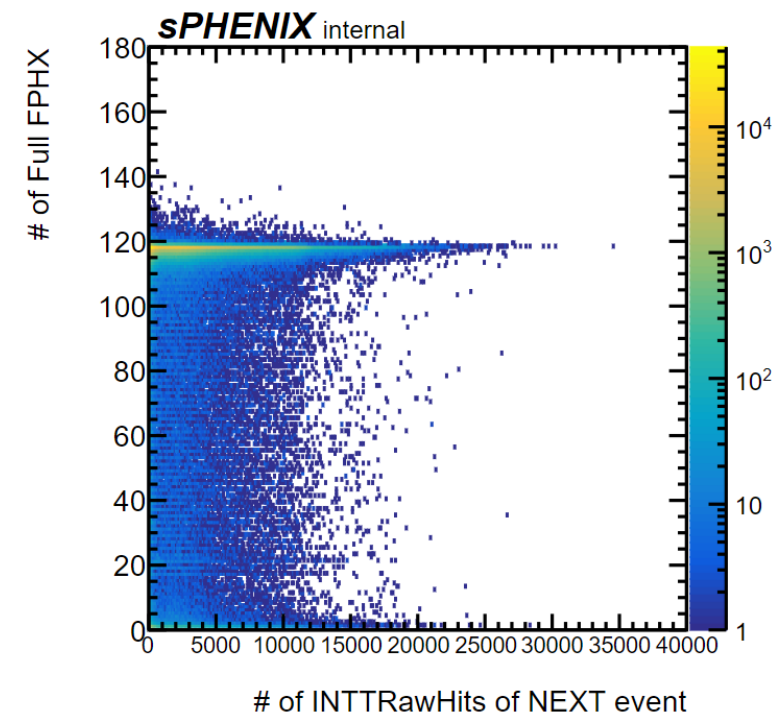
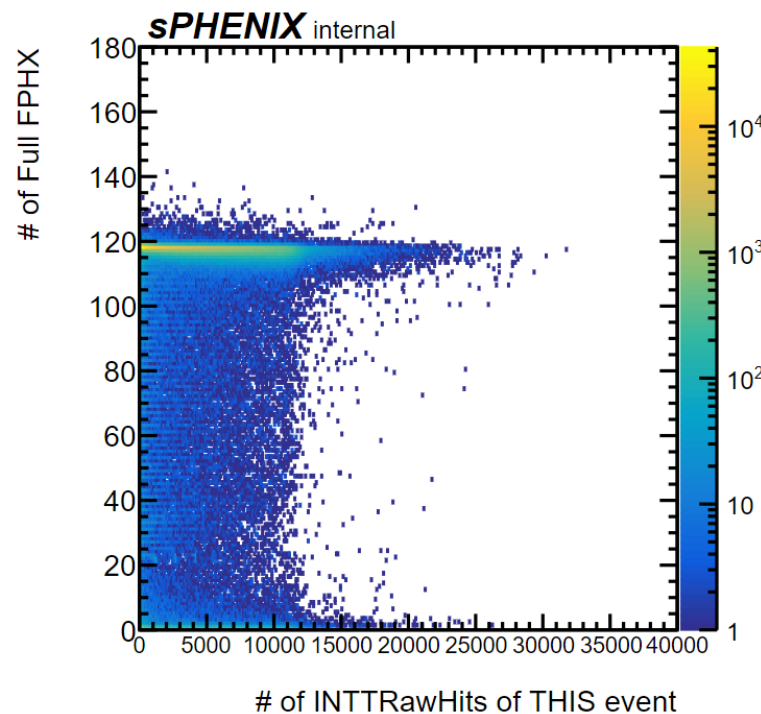
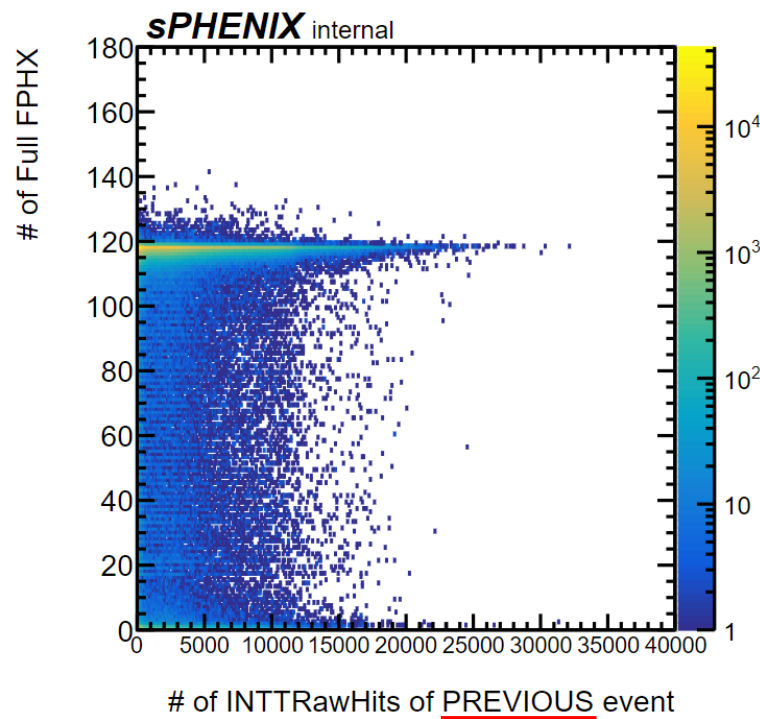
- There are overflow flags found in current INTT data as shown by Cheng-Wei
- We aim to understand which part of our detector it happened, how often it happened and under what conditions it happened
- The final goal is to understand whether it is an “issue” or not. If it is, what is the cause?
- Data of Run 54280 taken in 2024 Au+Au collisions is used (1.63M/10M analyzed)
 - Triggered readout mode, ncollision = 100, open_time: 60
 - Analysis based on INTTRawHit DST
 - For the results in slide 3 ~ 11, no bad channel removal applied
 - Comparisons w/ and w/o bad channel removal: slide 13 ~ 16
 - For all plots, no clone hit removal

(back entries: hits
with Full ROC fired)



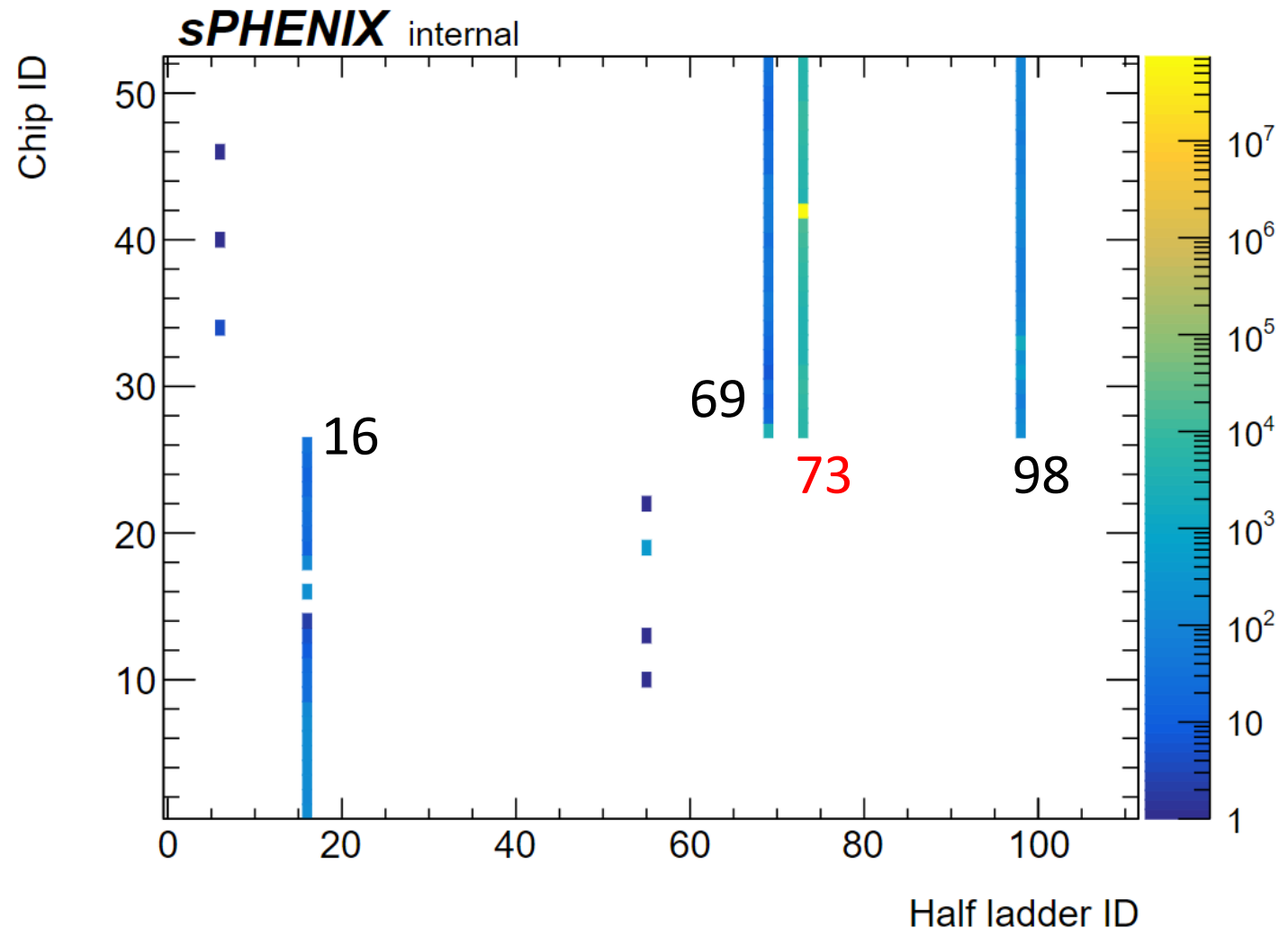
Chip Overflows vs. total hits

- (Events with no overflows are not included)
- If there is relationship between overflow and previous or next event total hits?
→ No obvious difference observed between these distributions



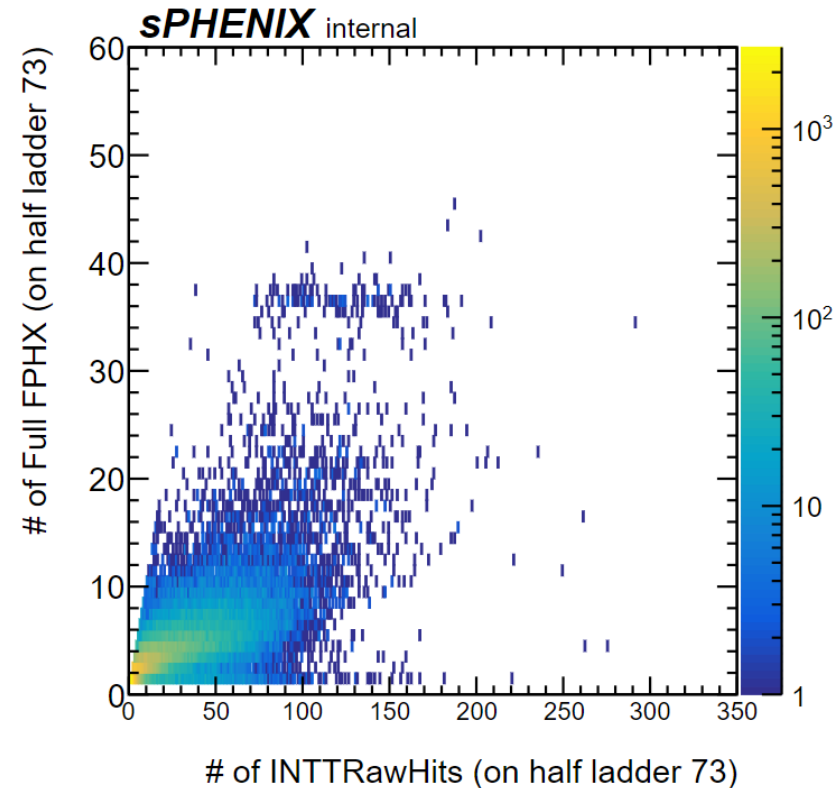
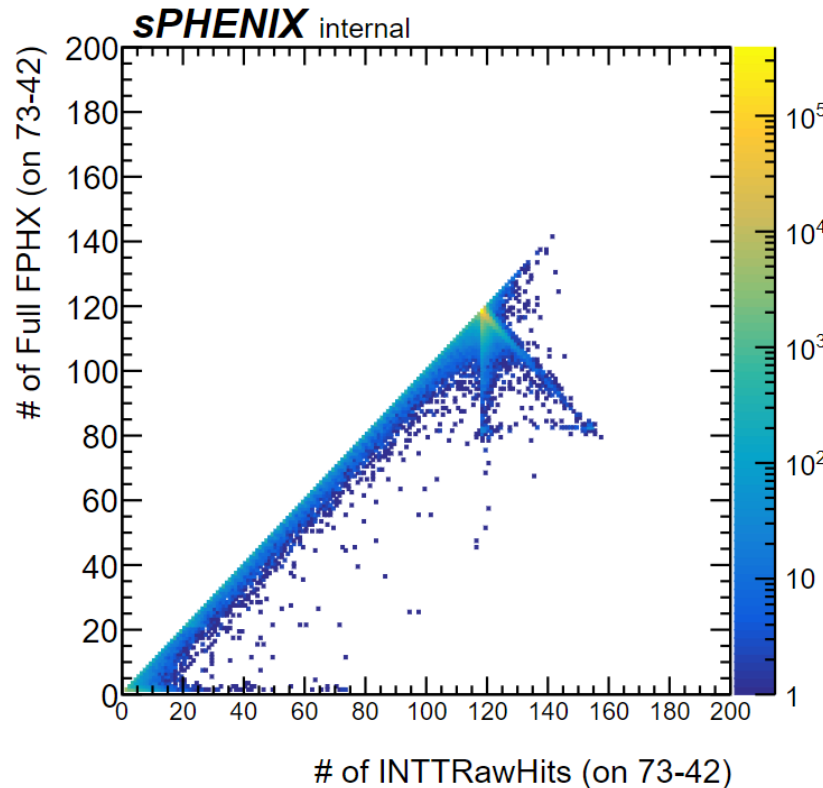
Chip Overflow hits distribution

- Half ladder ID = (packet ID – 3001) * 14 + fee ID
- The hottest chip: 73-42
- Chip independency violation:
 - In half-ladder 16, 69, 73, and 98, most of chips have hits with FullChip fired (kinda becoming half-ladder behavior)
 - Assuming chips are working independently, more scattered distribution expected



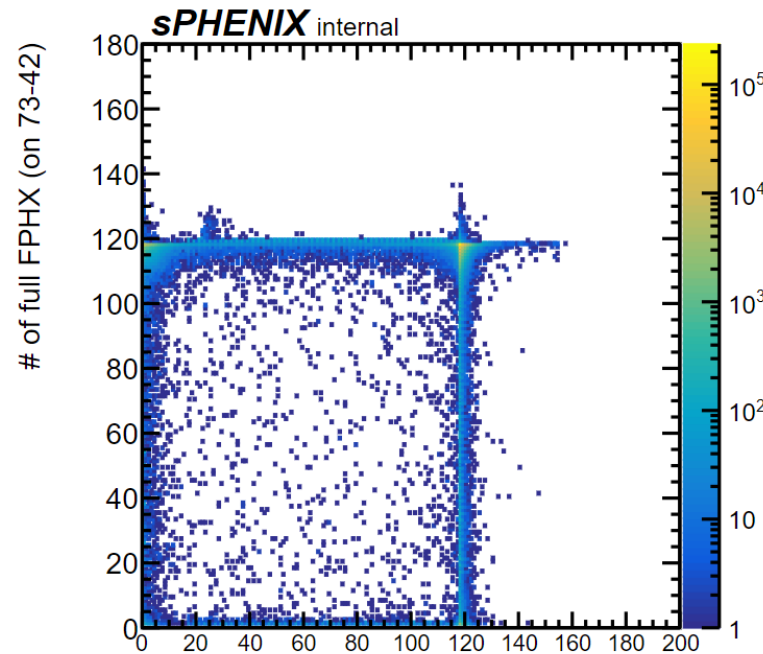
Chip Overflows vs. total hits (Half-ladder 73)

- (Events with no overflows are not included)
- **Shows a positive correlation at hot chips**
- Other three ladders are shown in backup

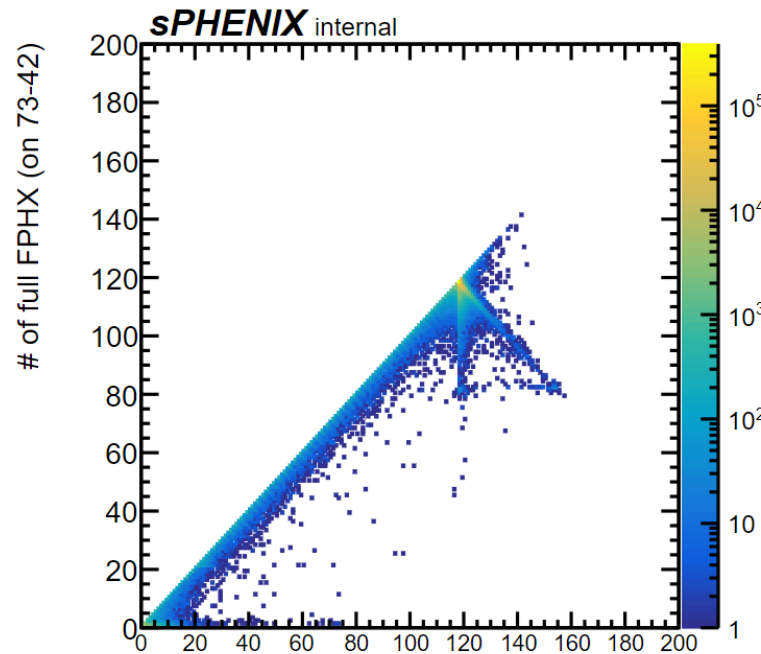


Chip Overflows vs. total hits

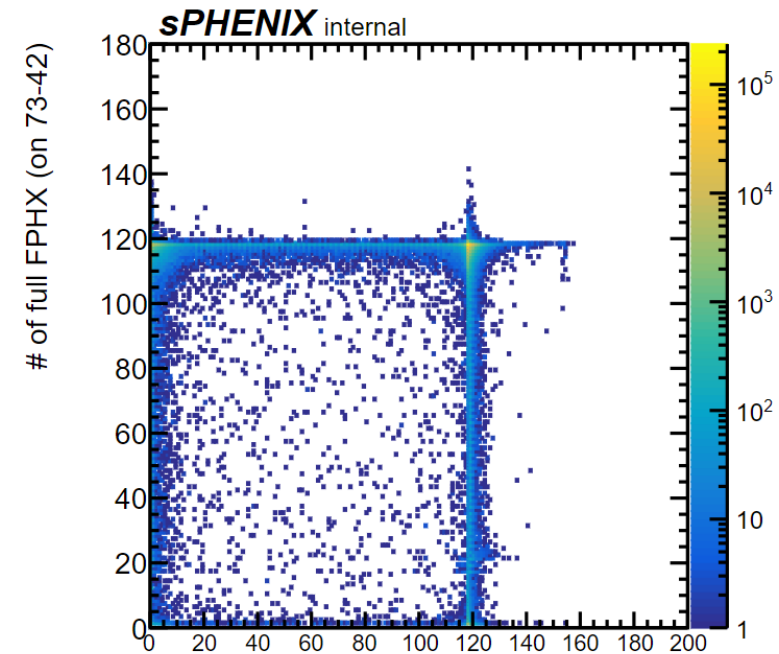
- (Events with no overflows are not included)
- On 73-42
- Have no relationship with previous and next event total hits



of INTTRawHits of PREVIOUS event (on 73-42)



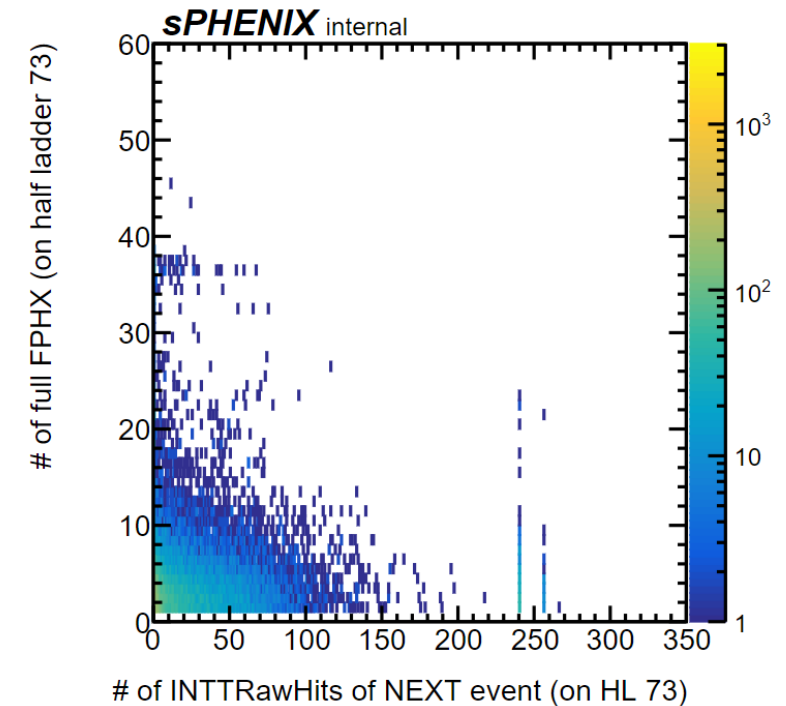
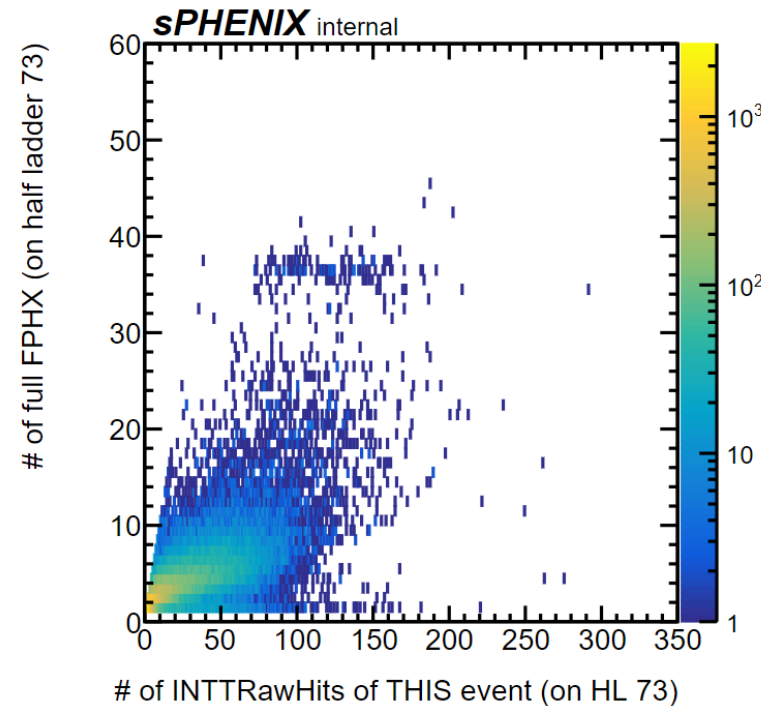
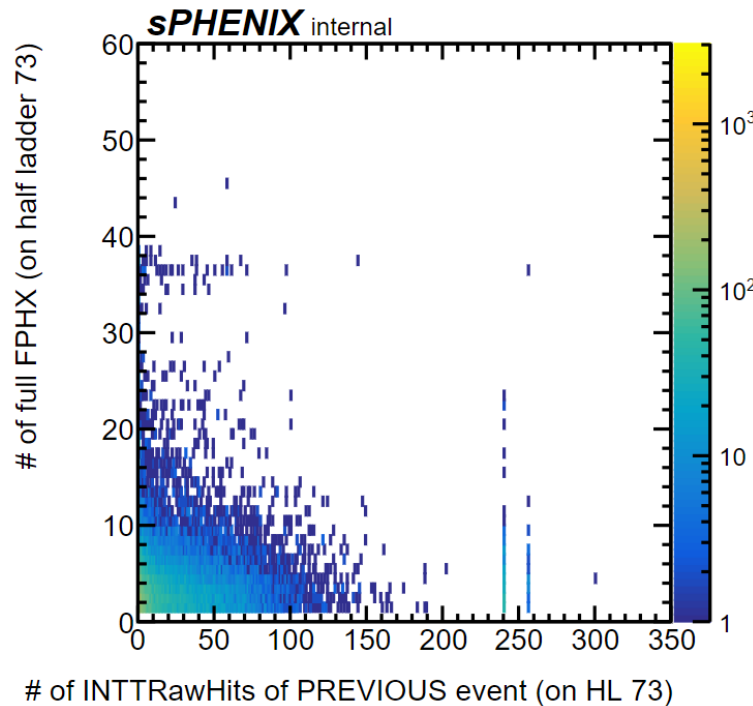
of INTTRawHits of THIS event (on 73-42)



of INTTRawHits of NEXT event (on 73-42)

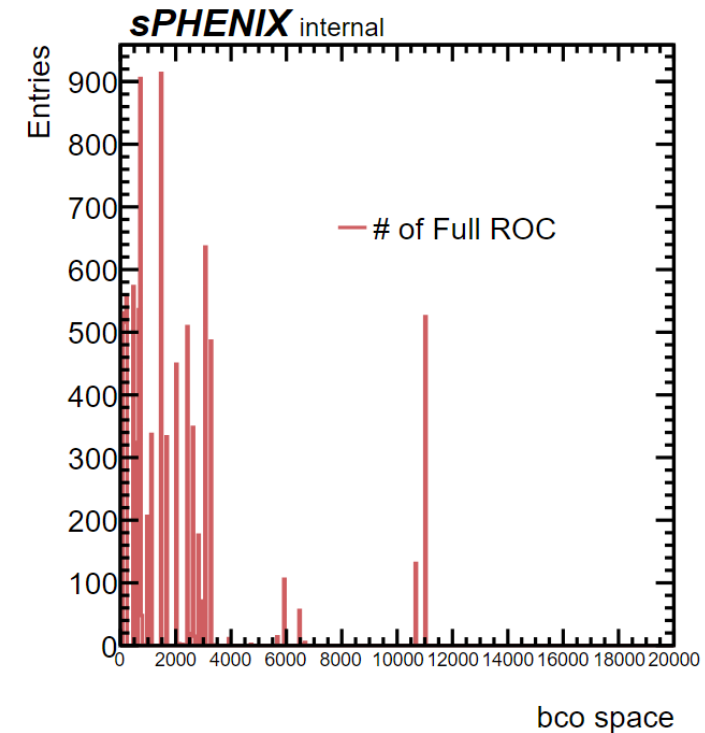
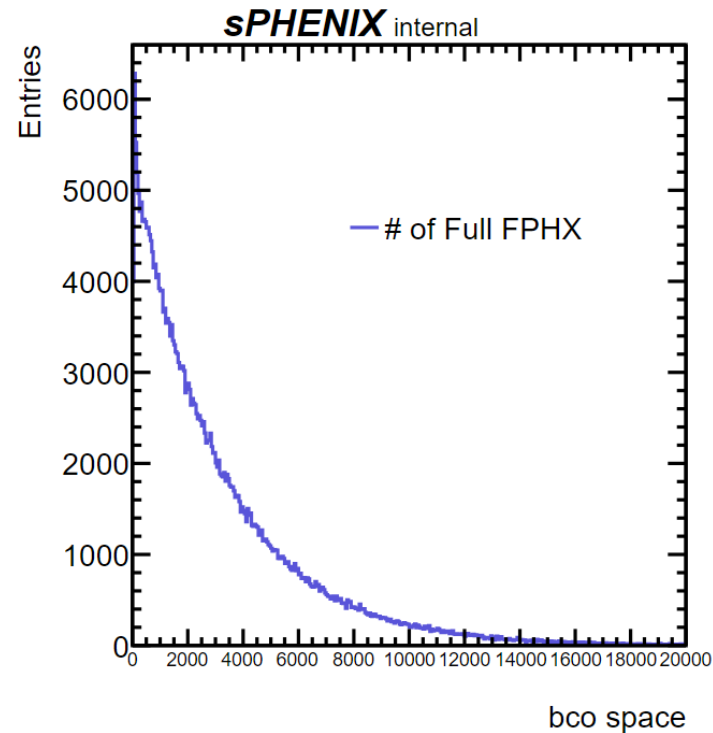
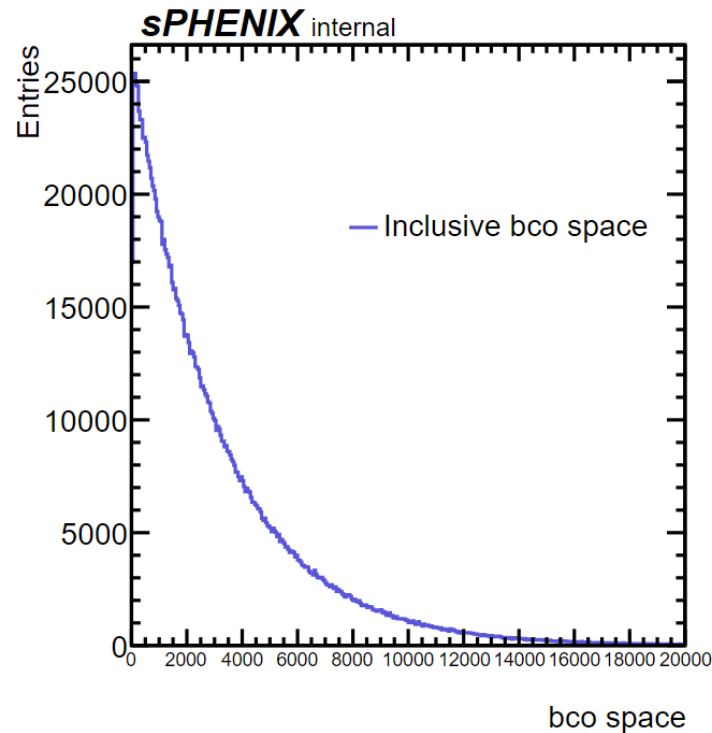
Chip Overflows vs. total hits

- On half-ladder (HL) 73 (without chip 73-42)
- Have no relationship with previous and next event total hits
→ Overflows may have nothing to do with previous and next event total hits



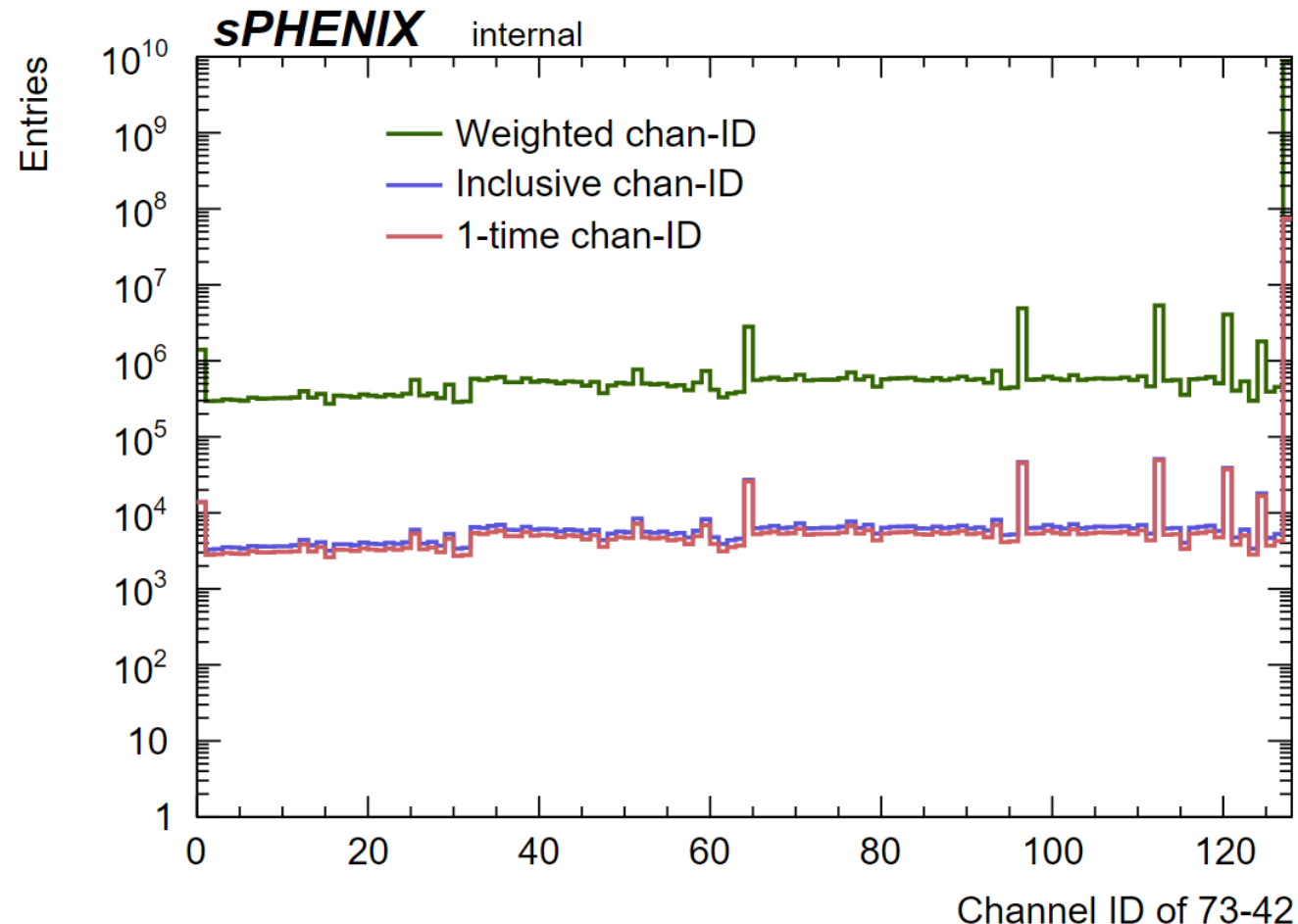
Chip Overflows vs. event bco space

- Event bco space = this event bco full – previous event bco full
- The # of full FPHX shows similar falling distribution with that of inclusive case
→ Overflows may have nothing to do with bco space



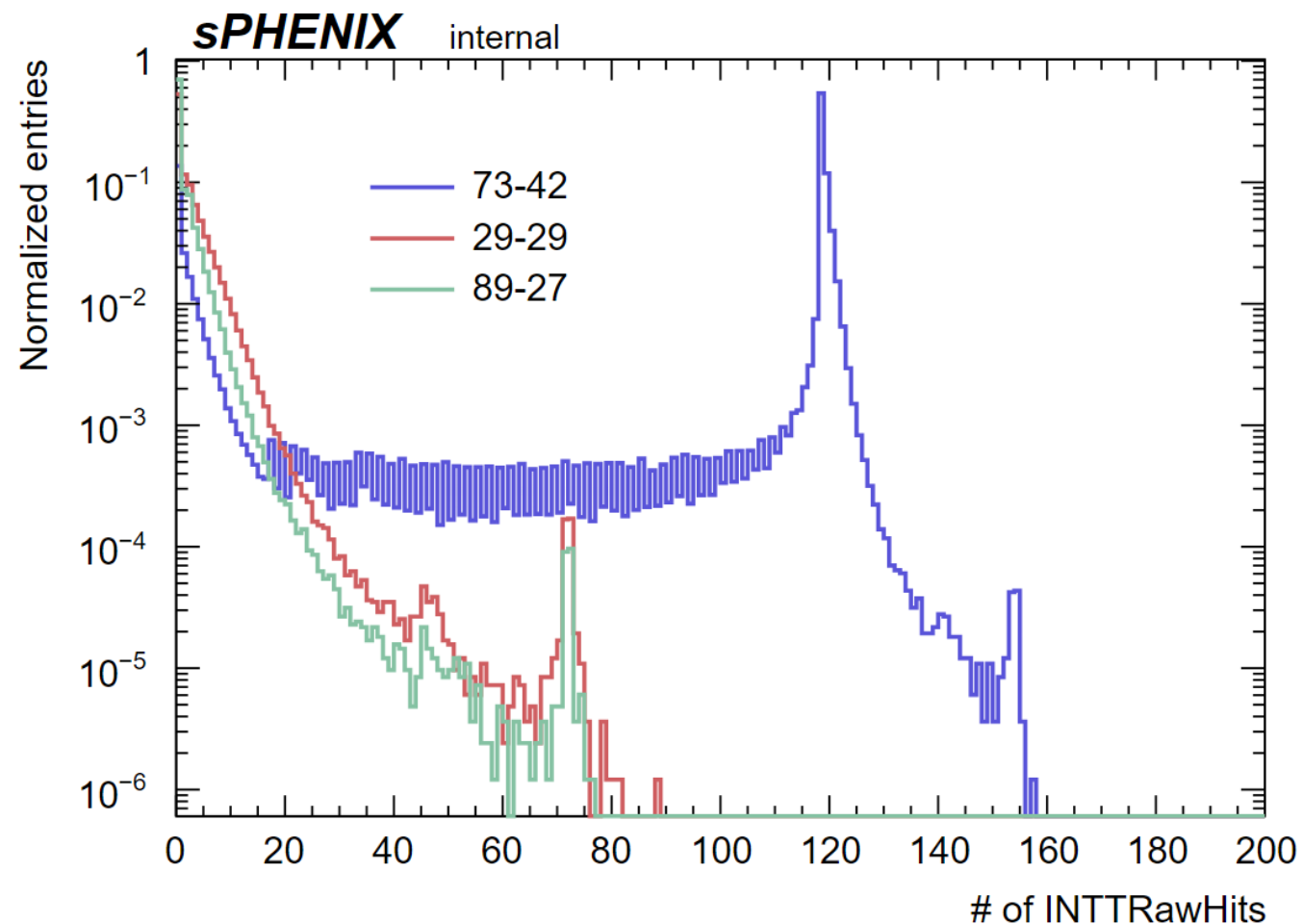
Channel ID distributions (on 73-42)

- **Weighted channel ID** = if an overflow flag found, fill in the whole channel ID distribution of this event & **weighted by # of full FPHX**
- **Inclusive channel ID** = fill in the whole channel ID distribution no matter what
- **1 time channel ID** = if an overflow flag found, fill in the whole channel ID distribution of this event & **1 event 1 times**
- No obvious difference between **Inclusive channel ID** and **1 time channel ID**. This means almost every time this chip gets hit, it overflows.



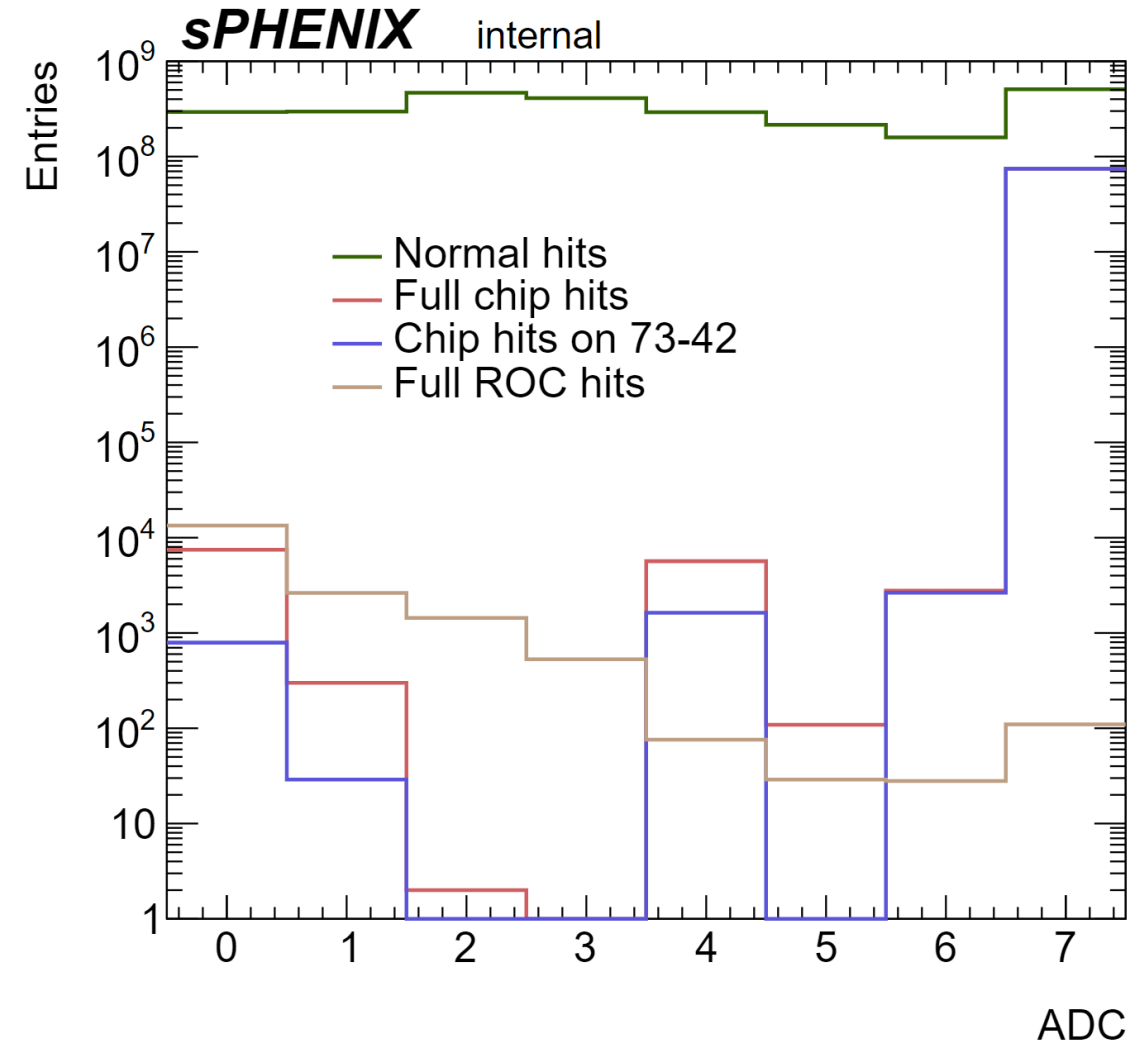
Number of hits distribution

- If we check the # of INTT raw hits of the chip 73-42, there is an unusual peak at 118 (unphysical)
- I randomly select two chips (29-29 & 89-27) which **never** happen overflow, their distributions **do not** show similar tendency
- For 73-42, # of hits > 128
 - Must have clone hits
 - Assuming the same hit process speed, additional (noise) hits may be generated in ROC level



ADC distribution

- The ADC distribution of **normal hits** (never happen overflow), **Full-chip hits which have happened overflow**, **full-chip hits on 73-42** and **full-ROC hits**
- The shapes of distributions filled by hits with FPHX overflow flag issued are very different from that of the normal hits

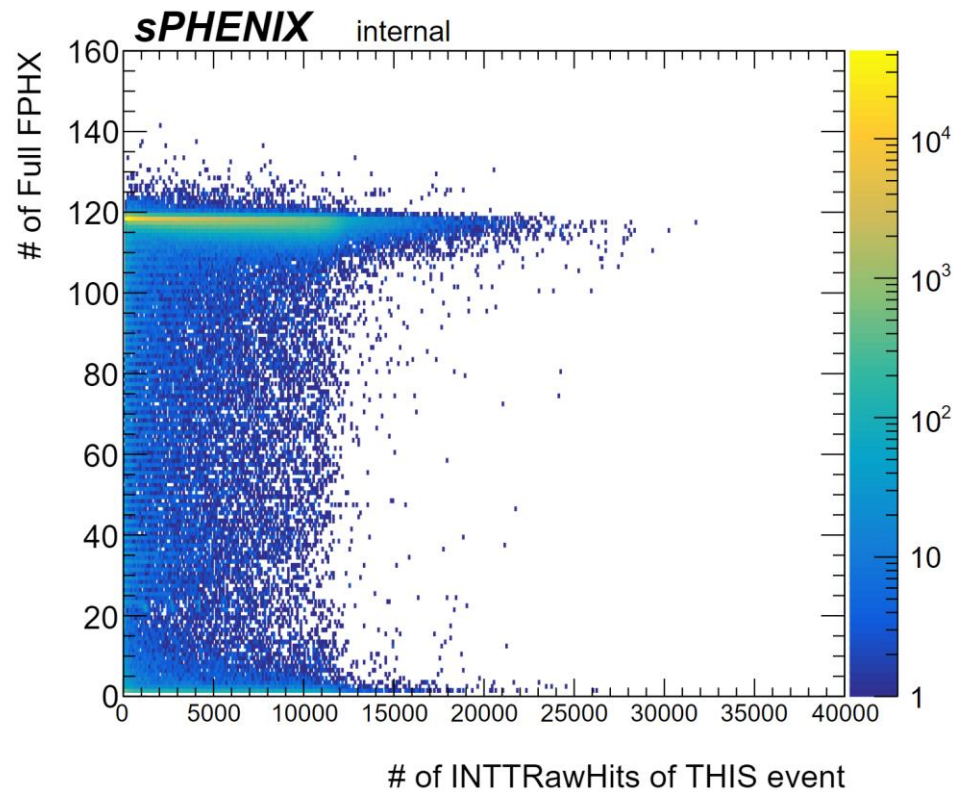


Apply bad channel mask

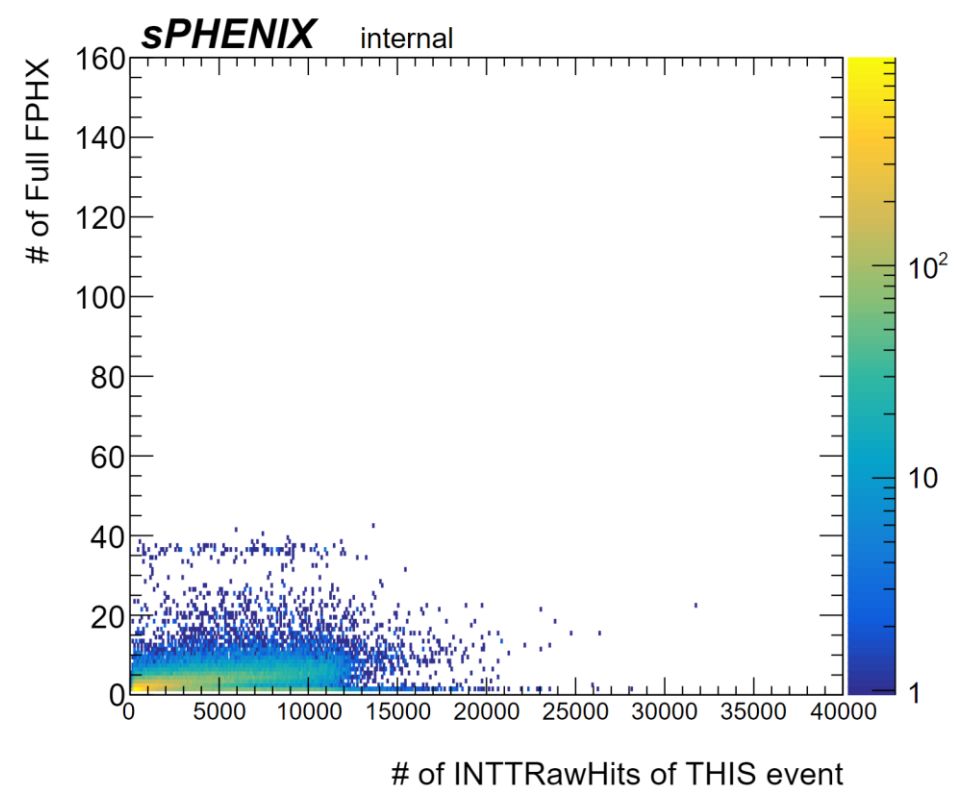
Chip Overflows vs. total hits

- # of full FPHX hits decrease!

w/o mask



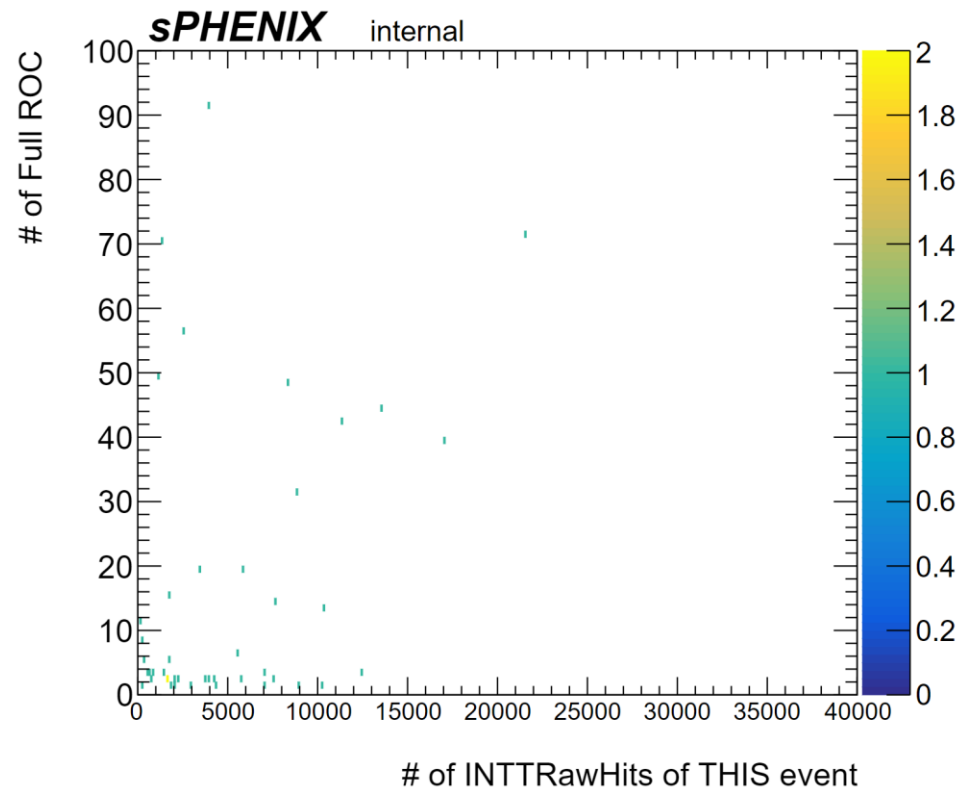
w/ mask



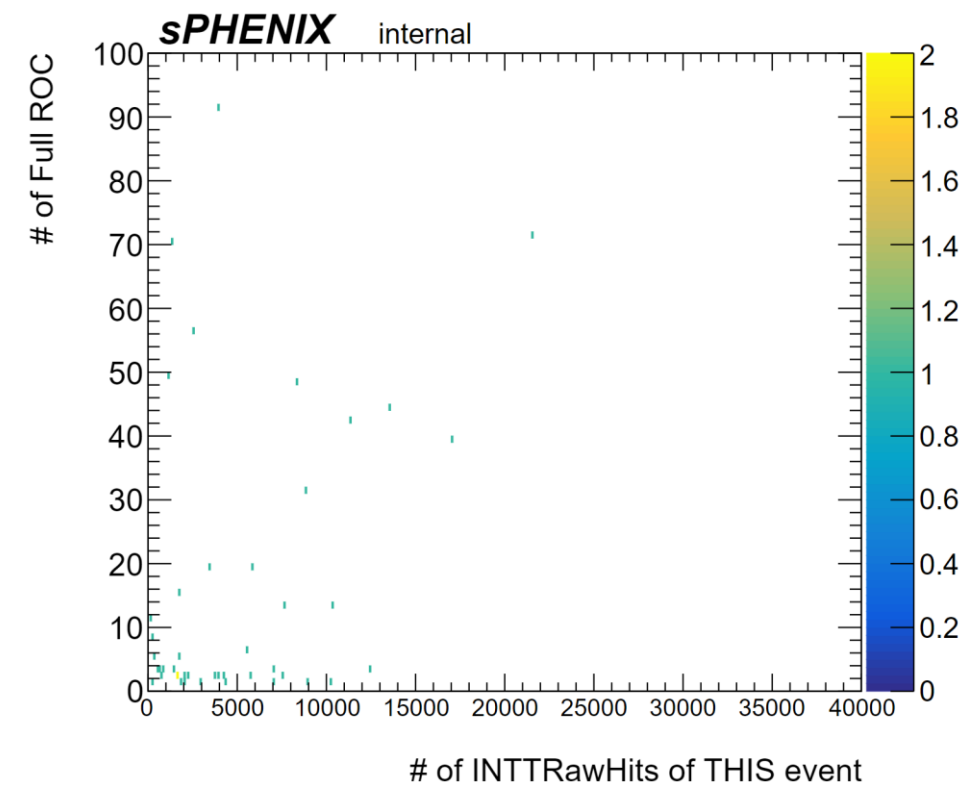
Overflows vs. total hits

- # of full ROC do not have obvious change

w/o mask

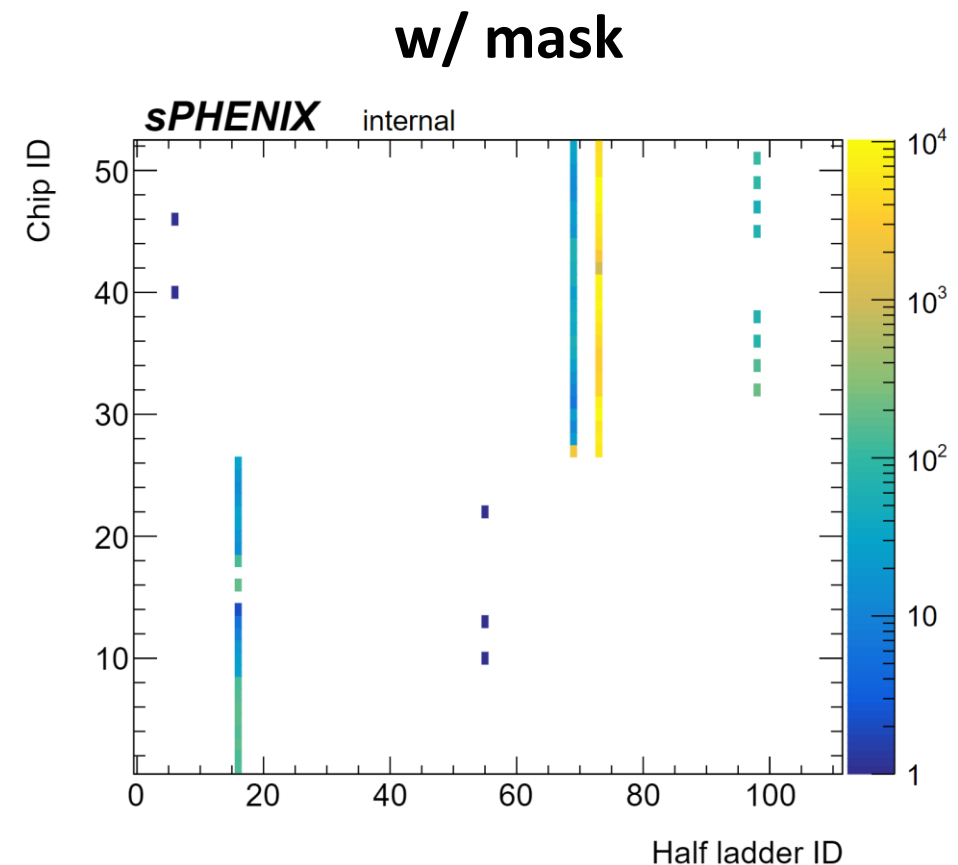
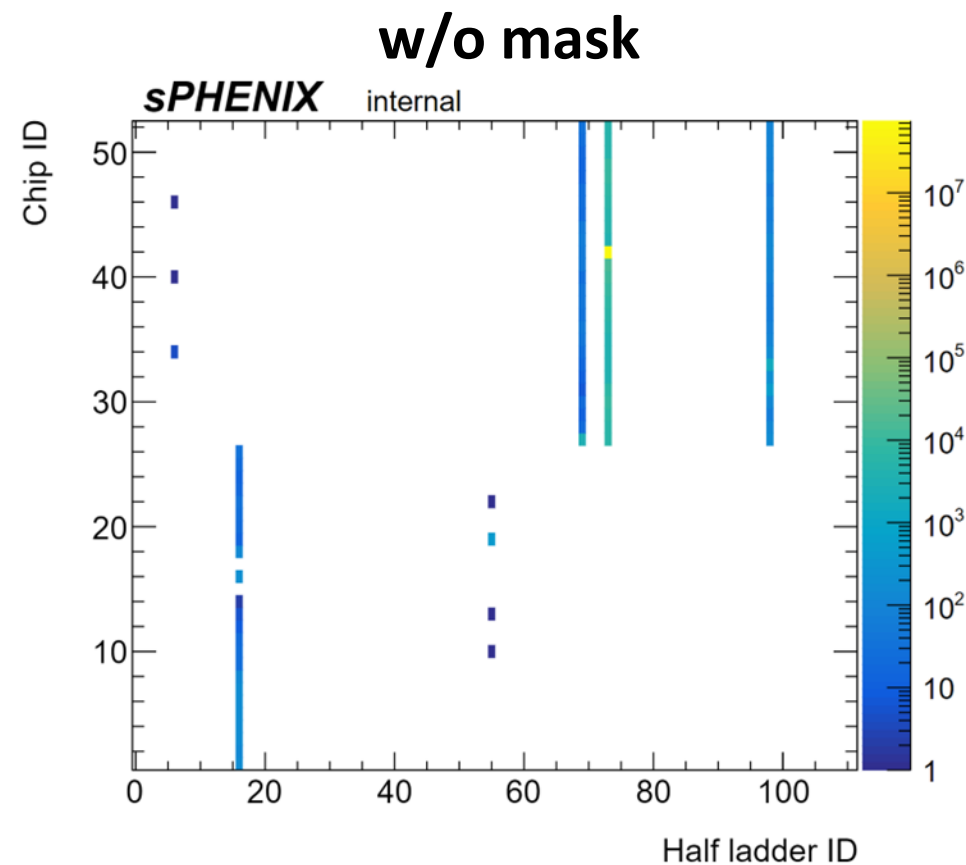


w/ mask



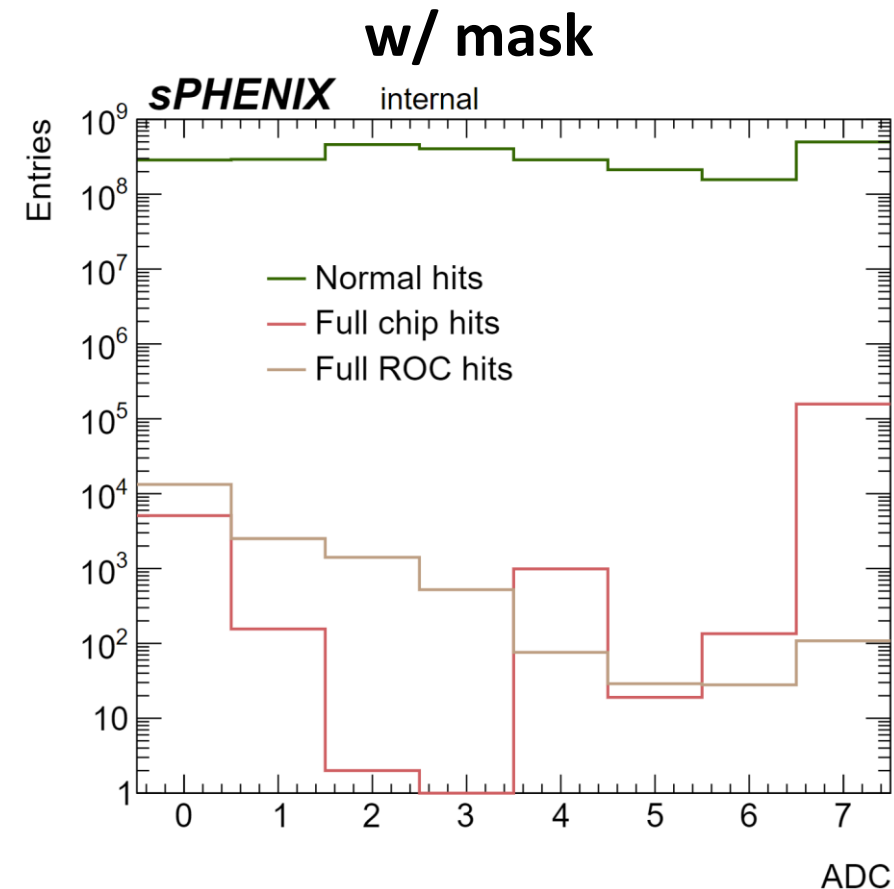
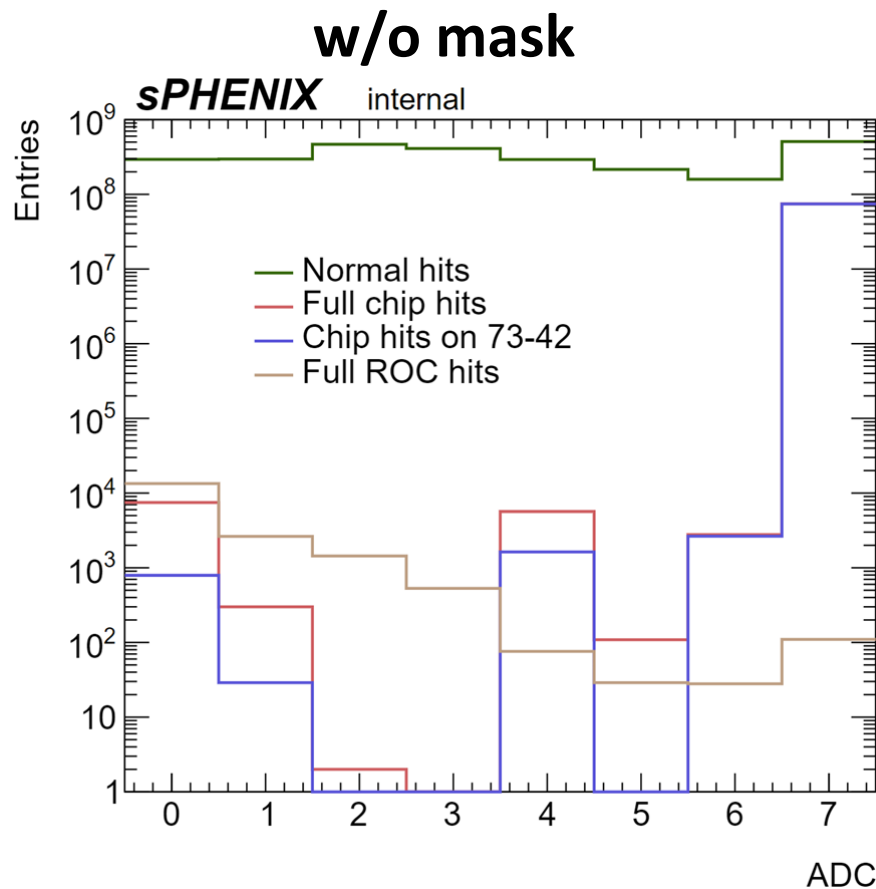
Chip ID and half-ladder ID

- Chip 73-42 is no longer the hottest one as most of its channels are masked



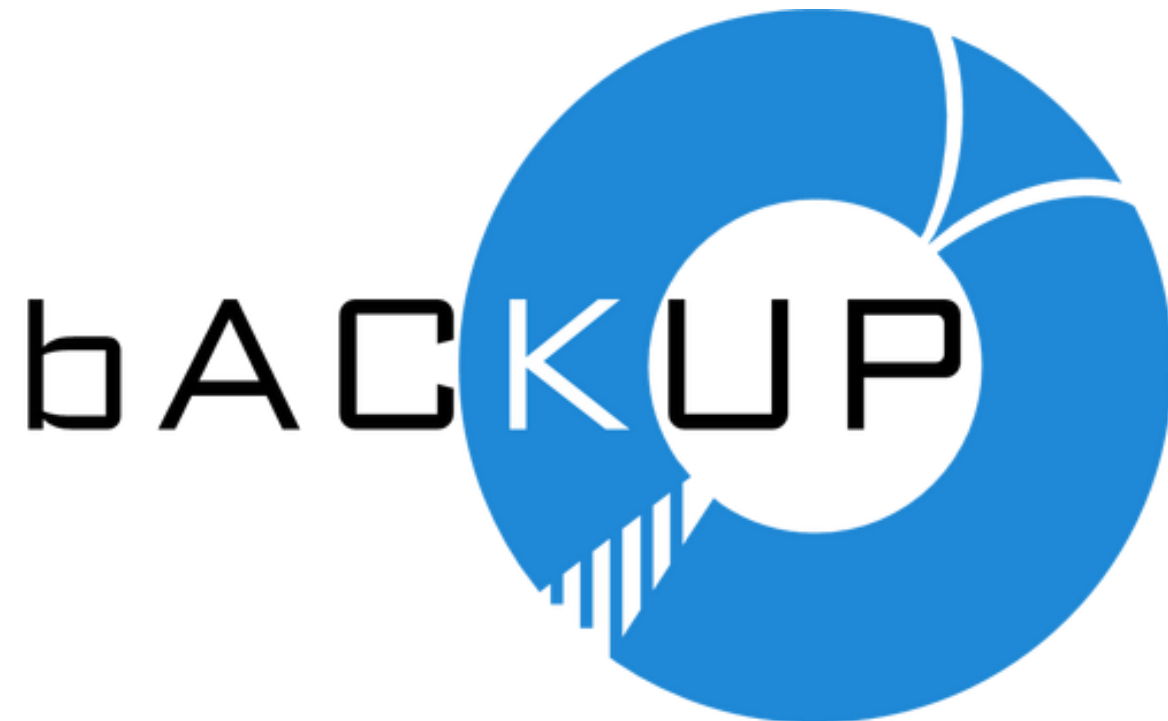
ADC distribution

- For the distribution of “Full chip hits”, the shape stays the same even after bad channel removal -> the indication of problematic hits?



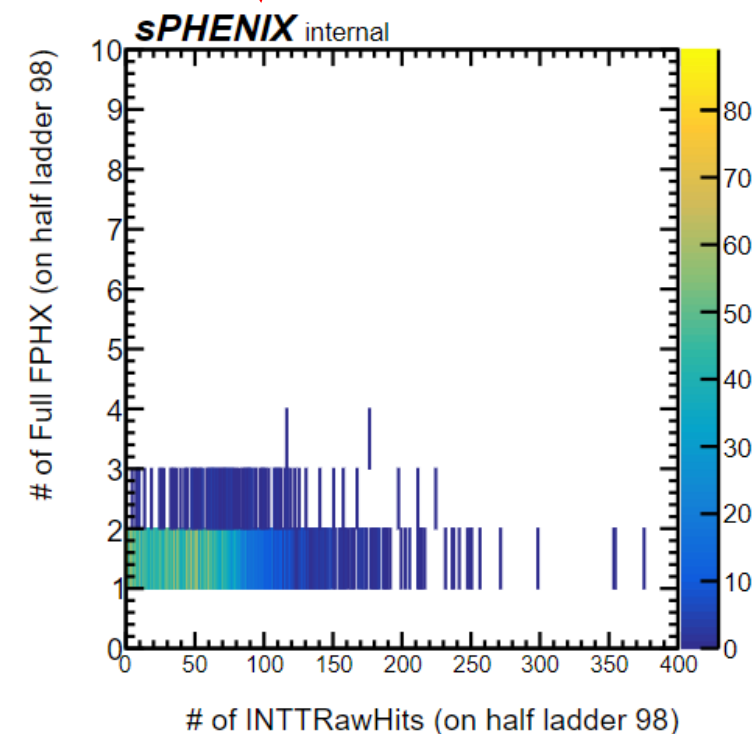
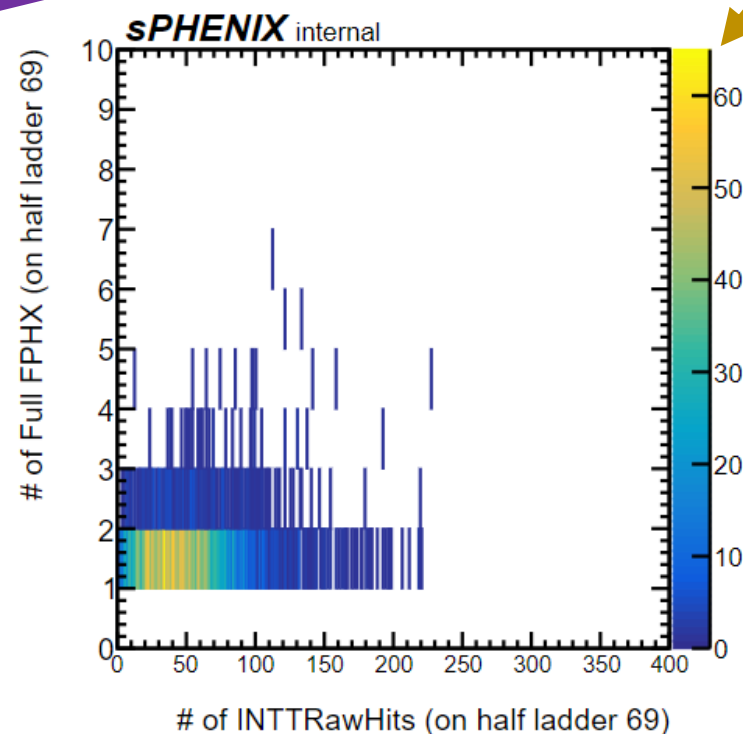
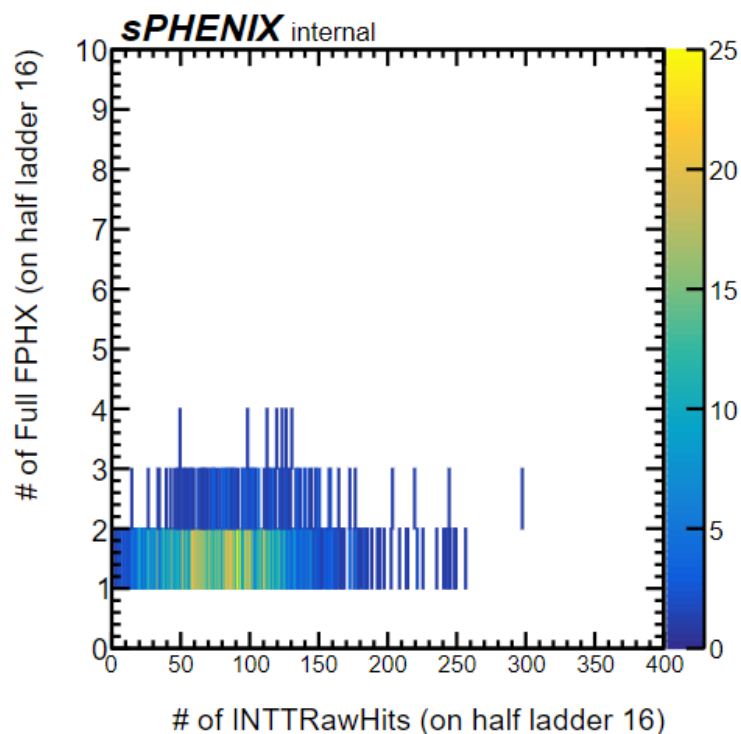
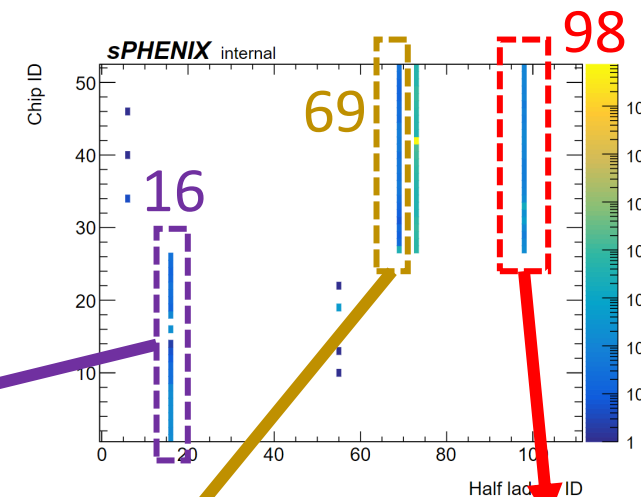
Summary

- The shapes of distributions filled by hits with FPHX overflow flag issued are very different from that of the normal hits -> maybe the indication of problematic hits
 - In the statistical wise: only 0.007% of hits has FullChip or FullROC issued
- In extreme case, chip 73-42 or half-ladder 73, overflow chip flags have positive correlation with total hits of this event
 - In chip 73-42, its number of hits distribution implying that the noise hits could possibly be generated in the ROC level, assuming the same hits process speed for chip
- The overflow chip and ROC flags seem to have nothing to do with hits of adjacent events and event bco space
- Hits with FPHX overflow distribution indicating that it's the half-ladder-level problem -> chip working independency principle violated
 - Distribution stays the same after bad channel removal
- Wrap: No clear evidence showing the meaning of overflow flags. The fraction of overflow hits is in the level of $7e-5$, should not be an issue

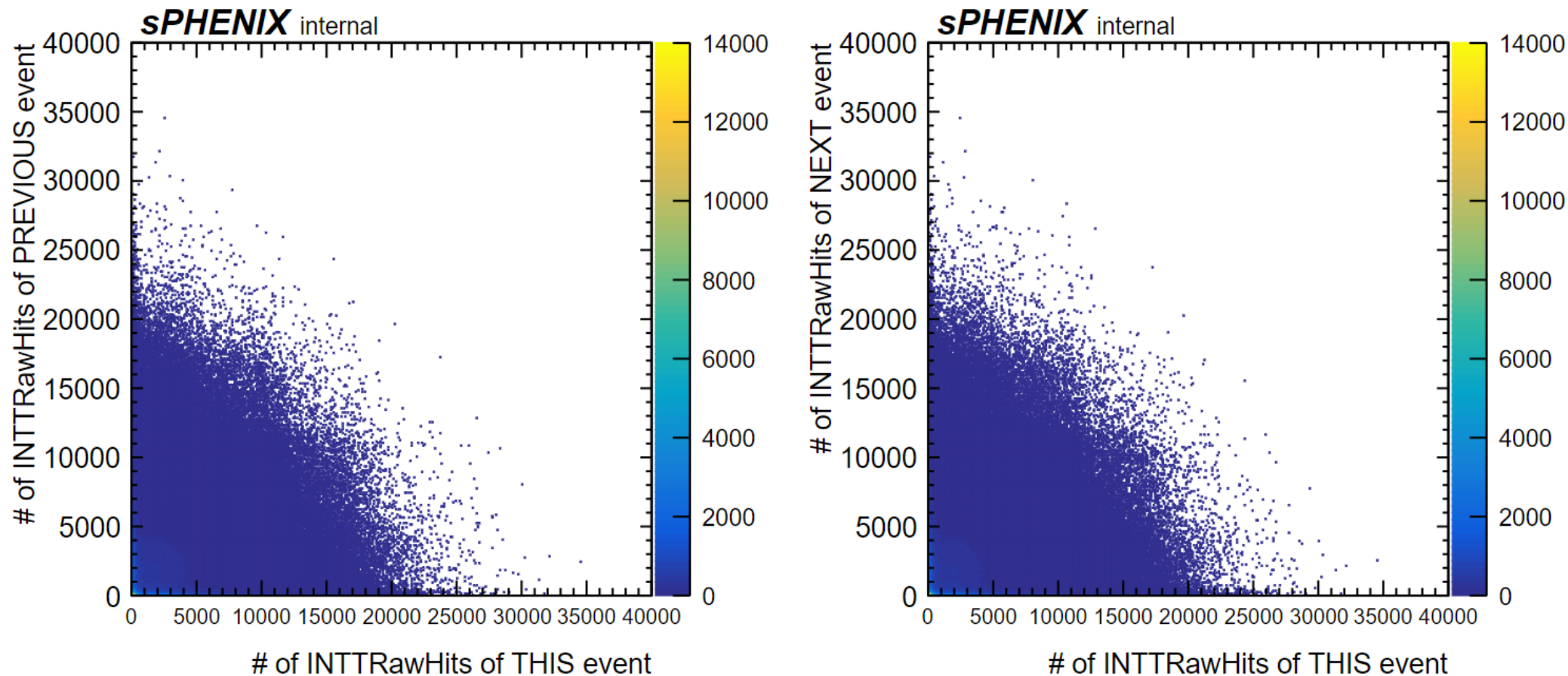


Overflows vs. total hits

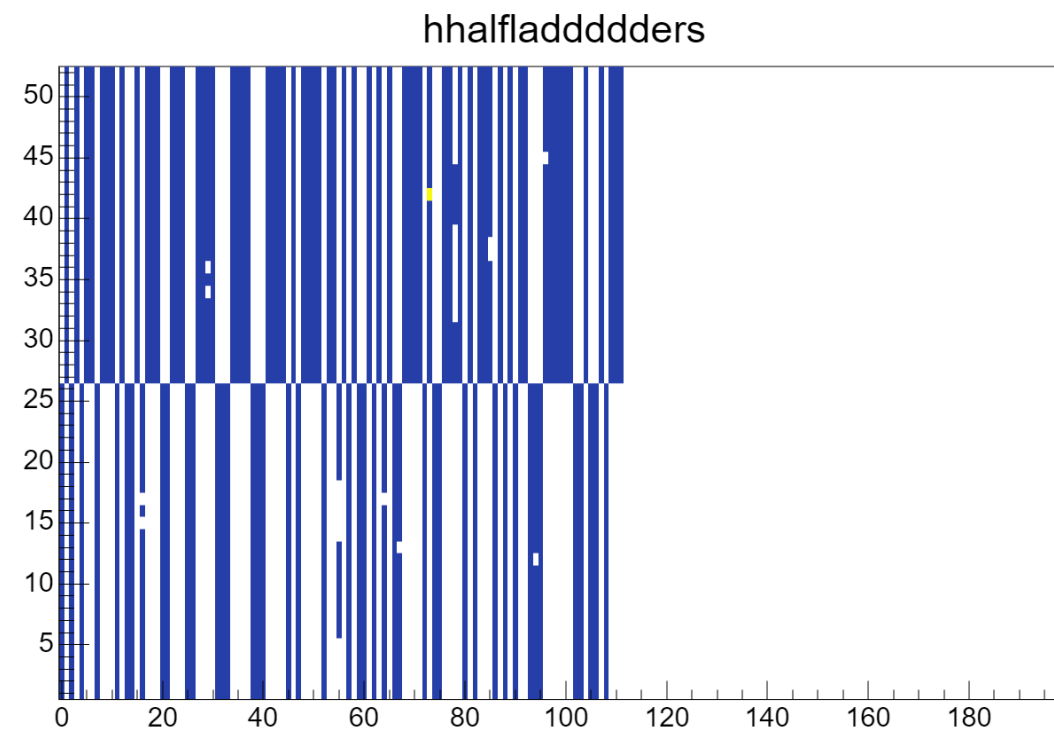
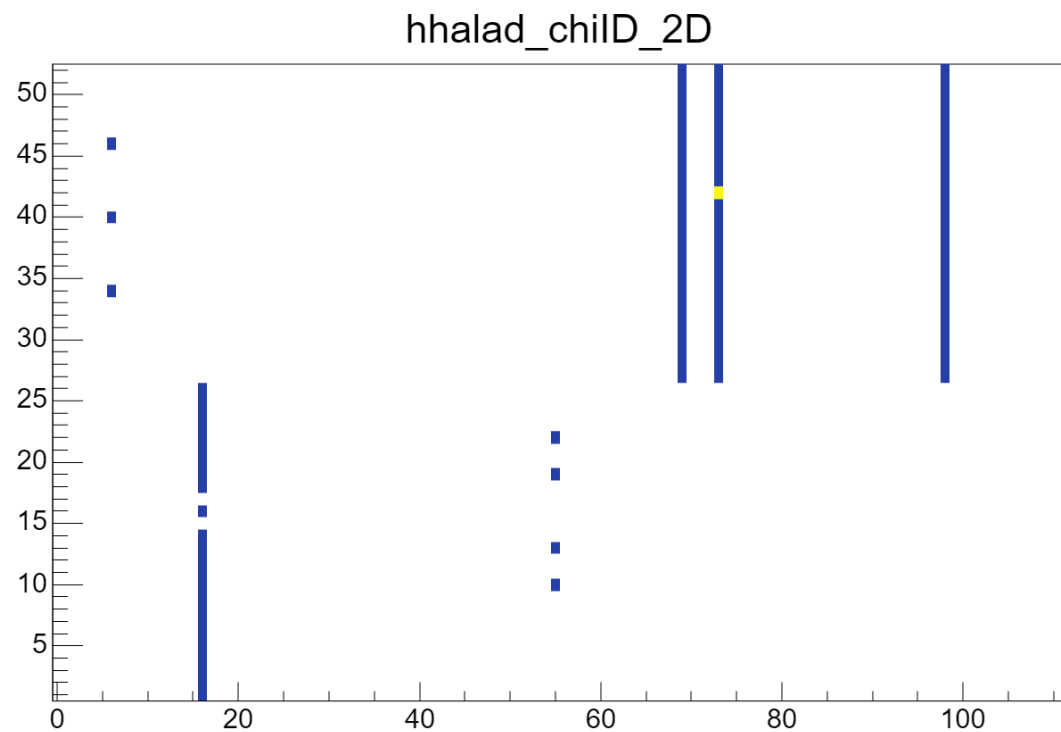
- Same plots on other half ladders
- No clear positive correlation



To check whether I get things right



How I select chips



Good channels

73_42_33
73_42_35
73_42_51
73_42_59
73_42_67
73_42_70
73_42_76
73_42_78
73_42_81
73_42_89
73_42_93

From Cheng-Wei

(In the first half of the slide, no bad channel removal applied. This is to see the electronic behaviors, including extreme cases)
(No clone hit removal as well)
(analysis based on INTTRawHit DST)

Chip independence issue...?

Chips on one half-ladder are expected to be independent b/w each other. Therefore this 2D distribution is then expected to be more like uniformly scattering. (In the other words, even if chip U1 has lots of overflow hits, it should be nothing to do with chip U2) However, If we just focus on half-ladder 16, 69, 73, and 98. Somehow all the chips in those half-ladders have some hits with overflow issued, which is against the expectation.

In Green and Red distributions, the bump at around NInttRawHits is expected, which is due to the chip saturation issue.

Number of INTTRawHits can be more than 128. It indicates that there must be clone hits in this chip. (clone hits: hits with same spatial position: FELIX, FELIX channel, chipID, channelID)

of INTTRawHits peaked at 118 -> unphysical, expected to be just noise hits predominately

Open_time is set to be 60, which results in cutoff at around 73 (the bumps in Green and Red Dists.) But the chip 73-42 can have hits beyond the cutoff limits (73 hits) -> The indication that those hits are not generated from chip (could possibly by ROC)