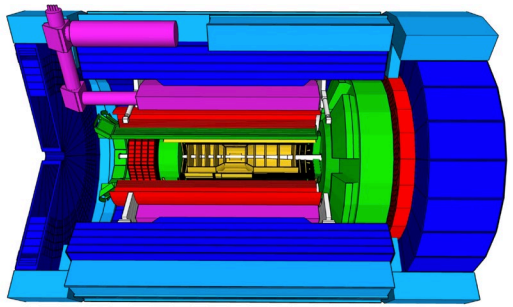


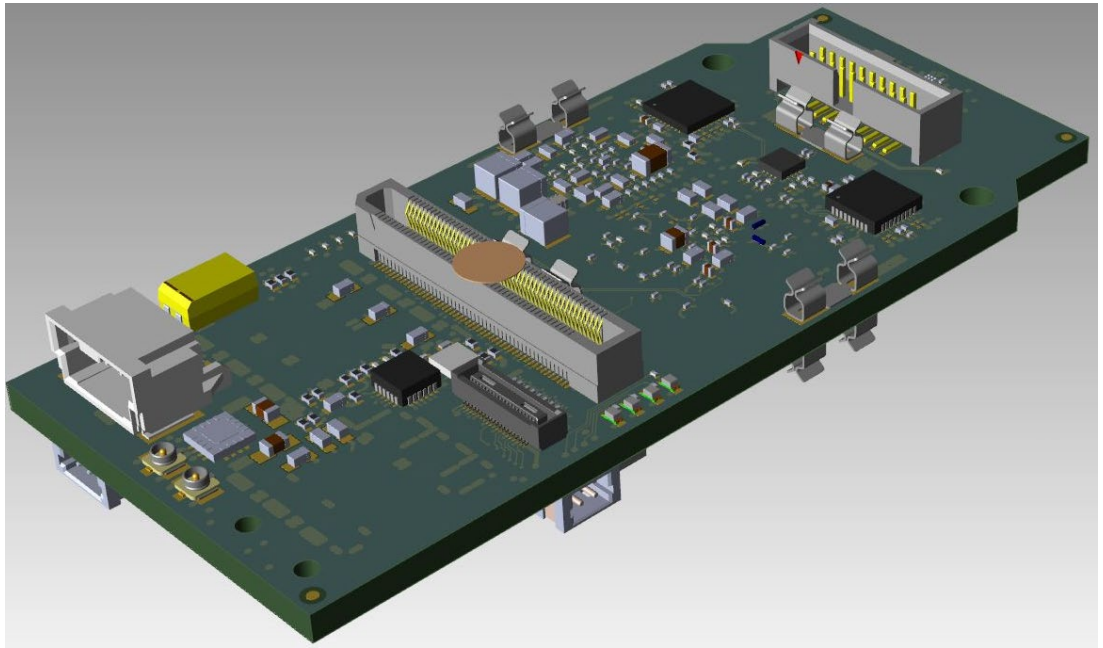
eRD109 update: dRICH RDO

Pietro Antonioli, Davide Falchieri, Sandro Geminiani, Giovanni Torromeo
on behalf of the INFN Bologna RDO team

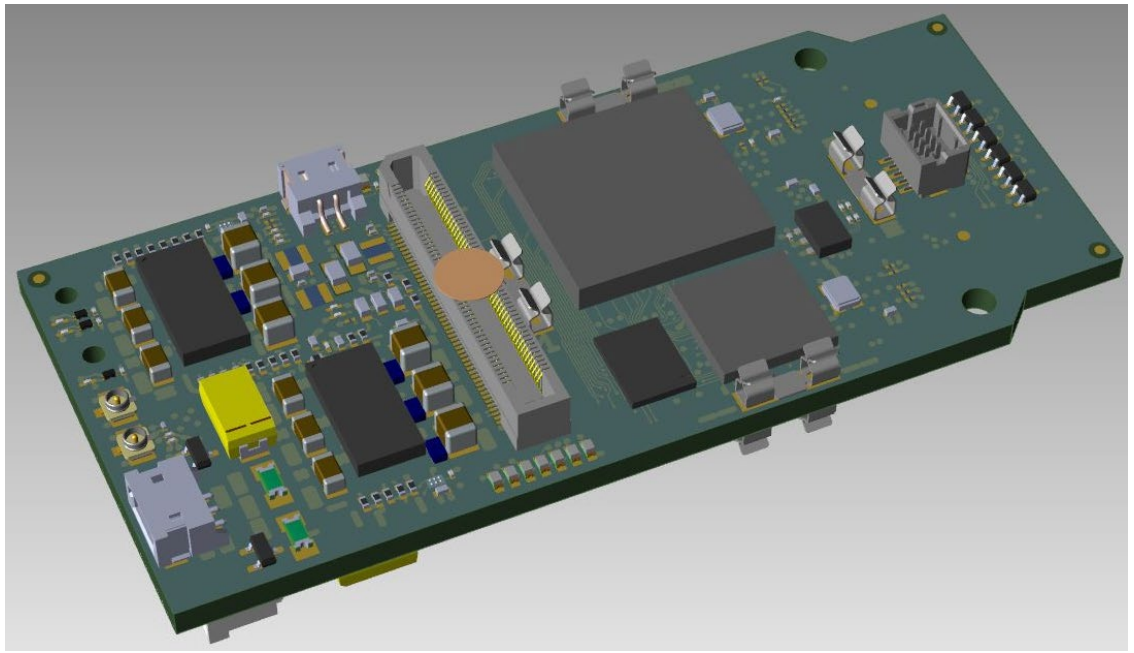
EPIC Electronics & DAQ WG meeting
08 May 2025

Towards RDO final layout

TOP

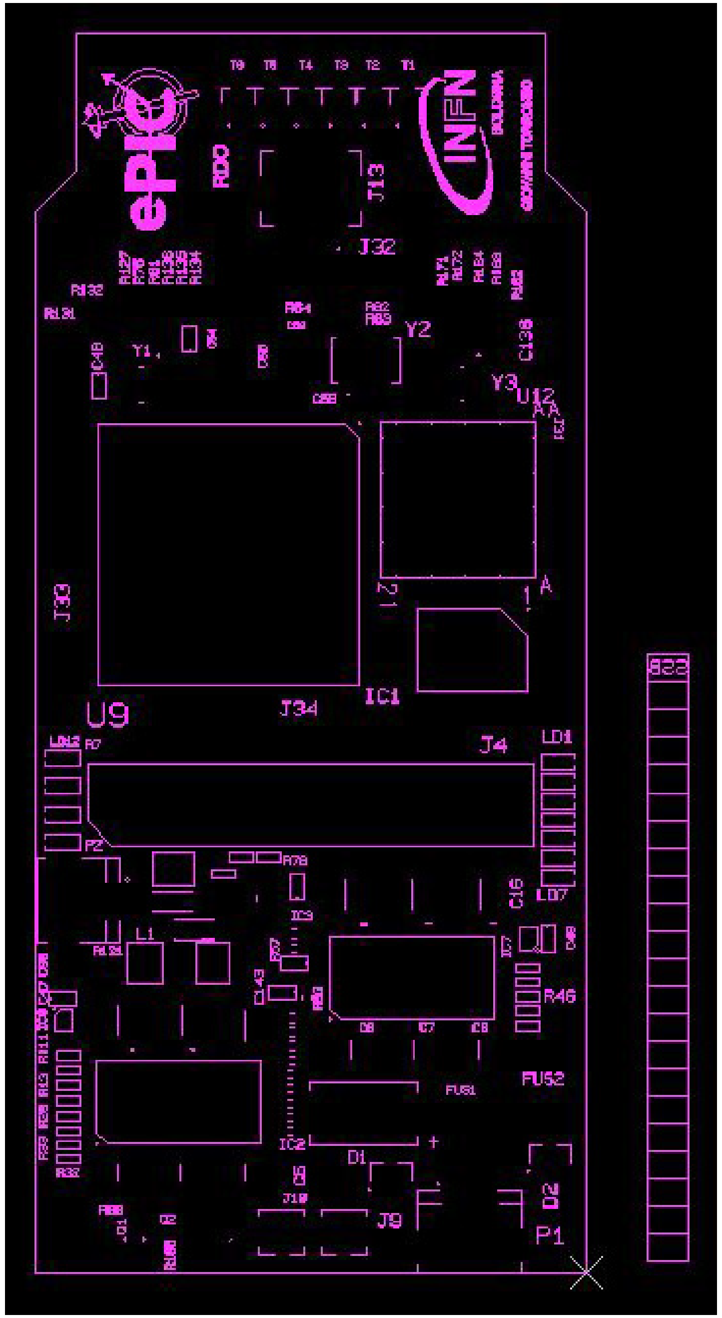


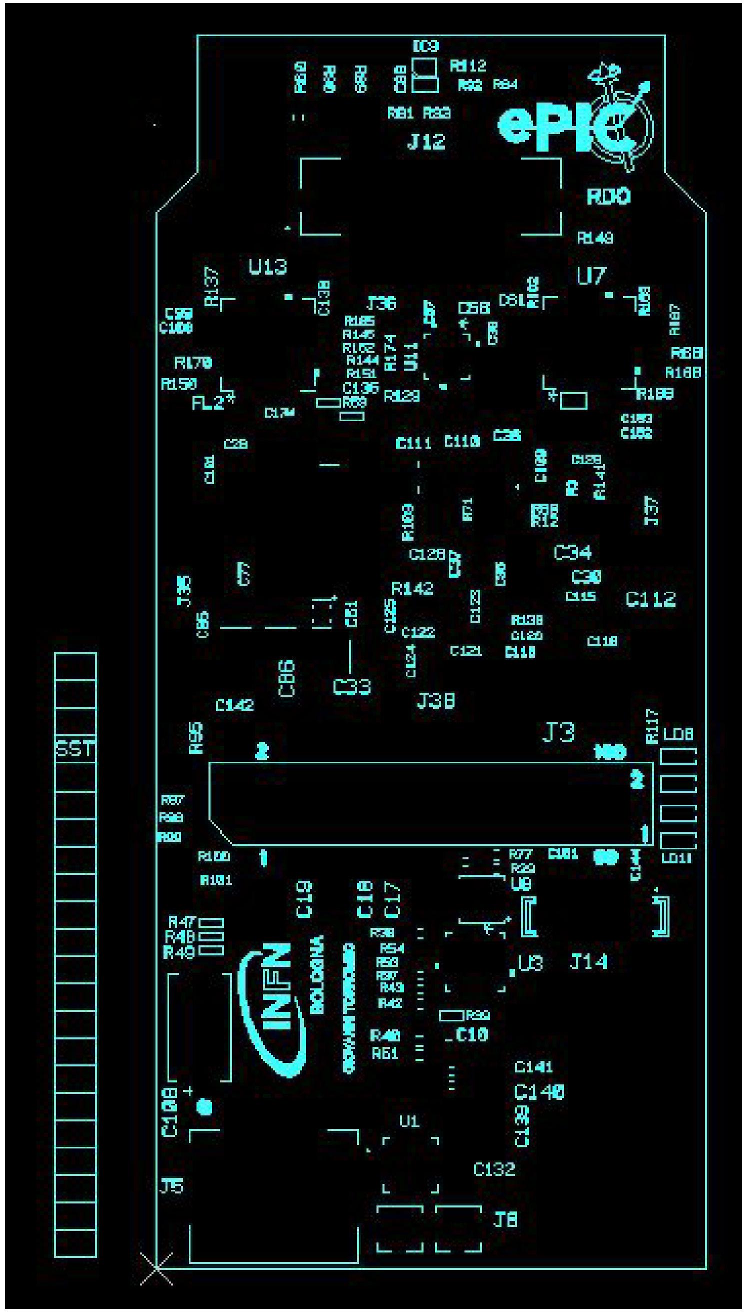
BOTTOM



News: the PCB layout has been finalized and the PCB fabrication has been launched on Tuesday 06 May 2025

we expect 12 PCBs (of which 10 populated) in 5 weeks: first half of June 2025

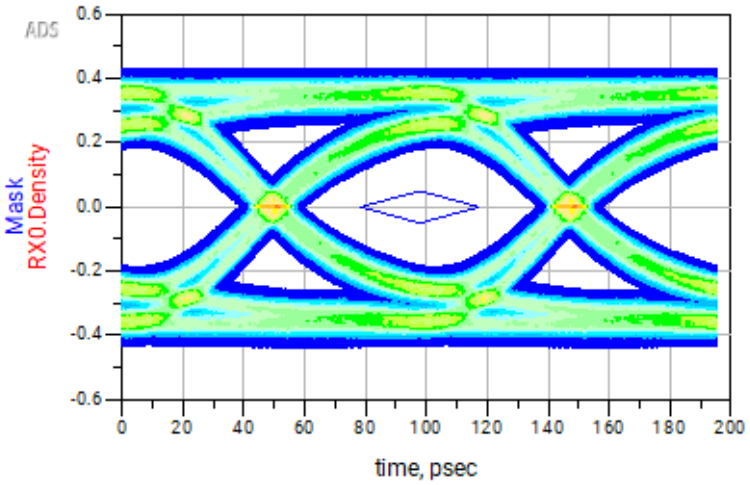

ePIC
INFN
RDO
J13
J32
Y2
Y3
U12
J33
IC1
J34
U9
J4
LD1
LD7
C16
R46
FU52
D2
P1
J9
D1
IC2
L1
SS2


ePIC
RDO
J12
U13
U7
J36
J37
C34
C112
C33
C86
J38
J3
LD8
SST
INFN
U3
J14
C140
C141
C132
J5
J8
U1
C10
C19
C18
C17

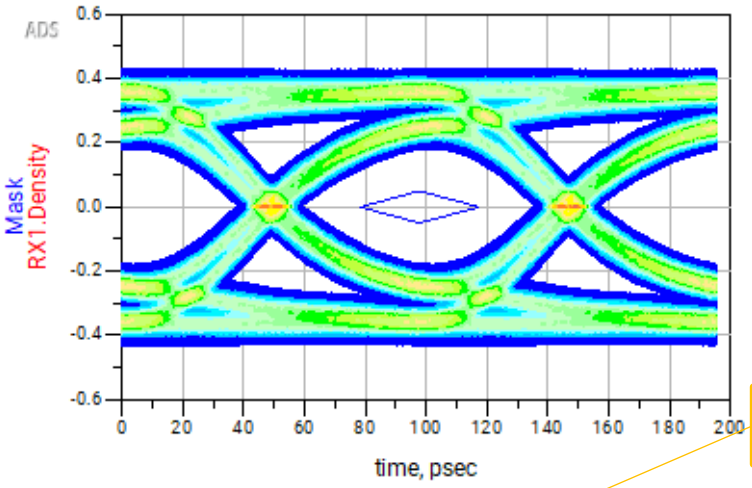
ARTEL S.r.l.
PCB ENGINEERING

4 Channels TX ARTIX Ultrascale+ GTH to VTRX+ receiver
AC coupling termination 100 Ω dielectric FR408HR

ADS Keysight



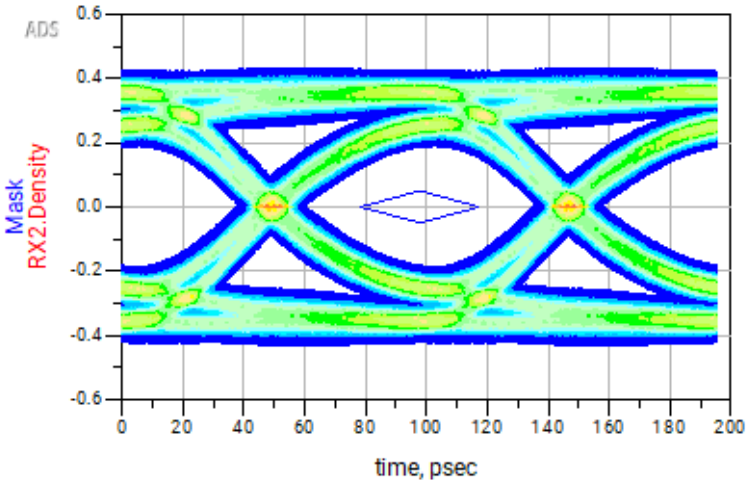
index	...e(RX0.Height)	...te(RX0.Width)
0.000	0.319	7.861E-11



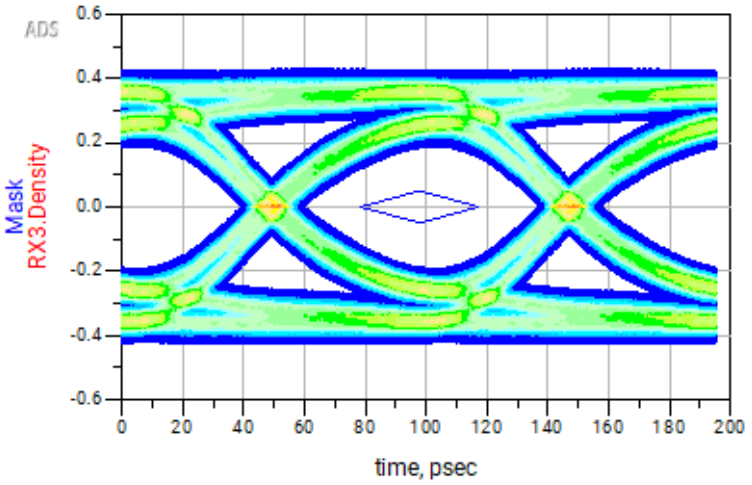
index	...e(RX1.Height)	...te(RX1.Width)
0.000	0.311	7.666E-11

min. Height

min. Width

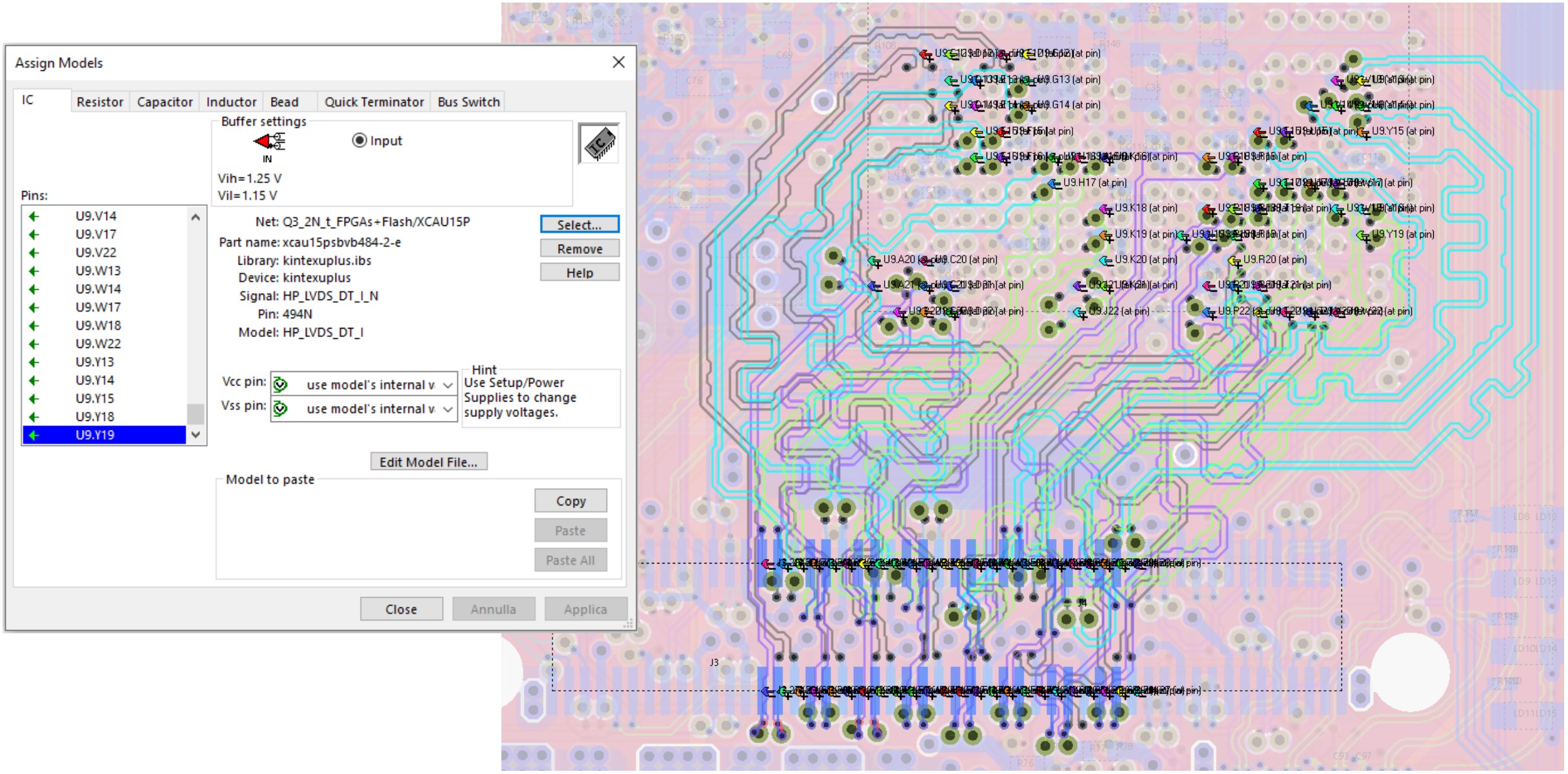


index	...e(RX2.Height)	...te(RX1.Width)
0.000	0.325	7.666E-11

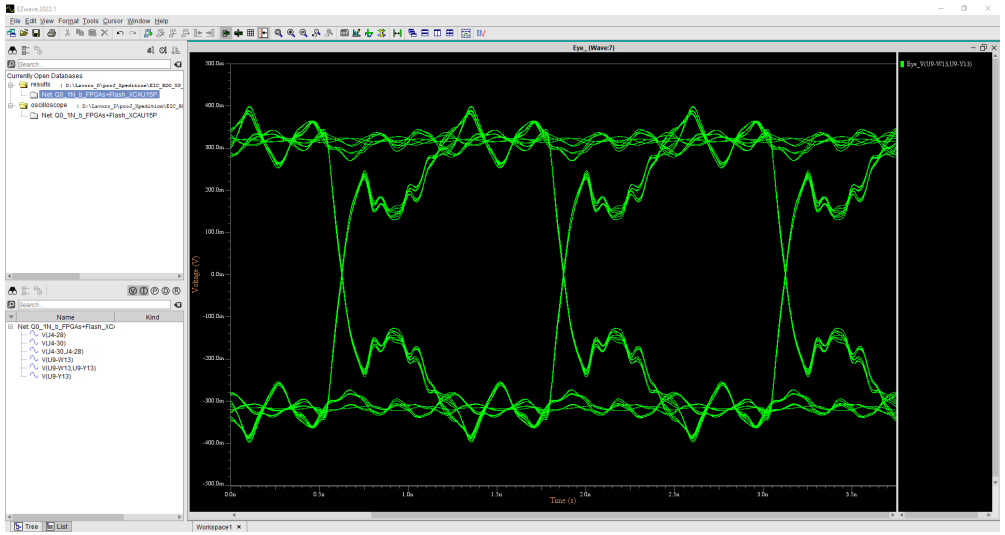


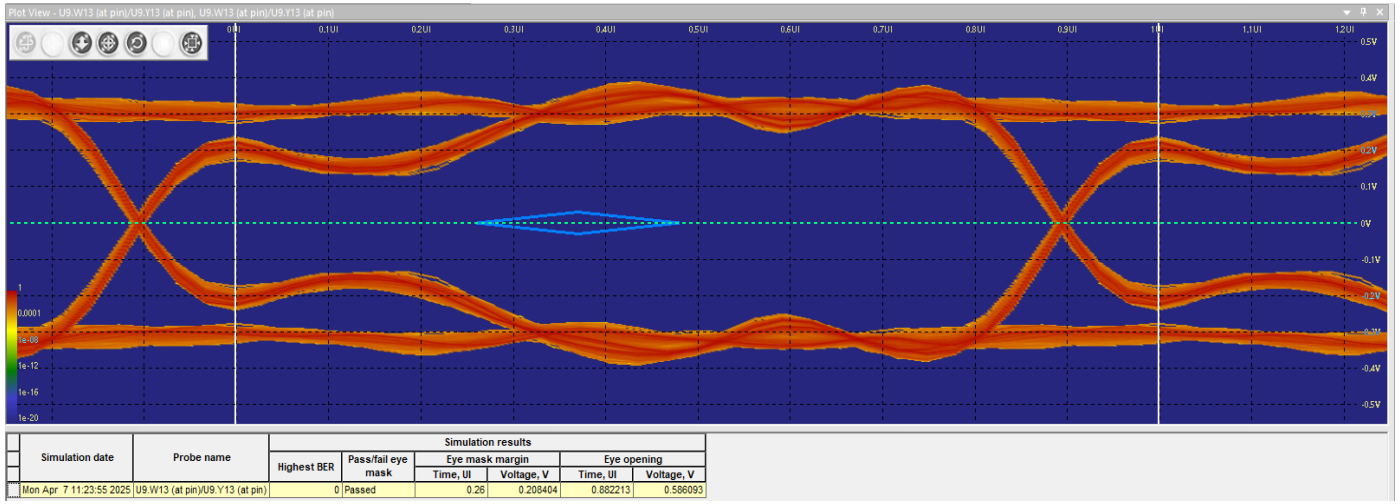
index	...e(RX3.Height)	...te(RX3.Width)
0.000	0.324	7.861E-11

Routing of 32 lanes ALCOR bus

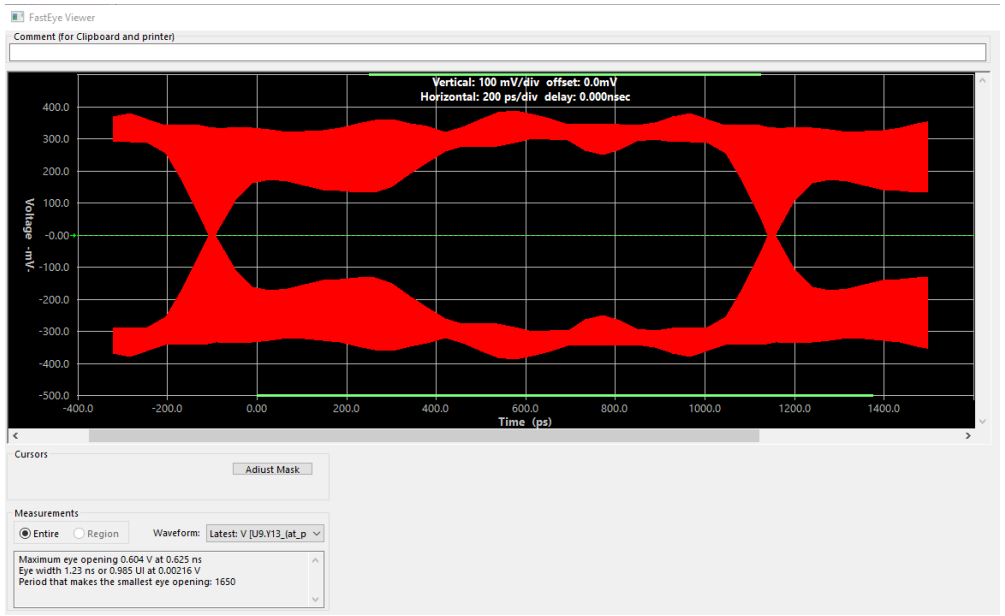


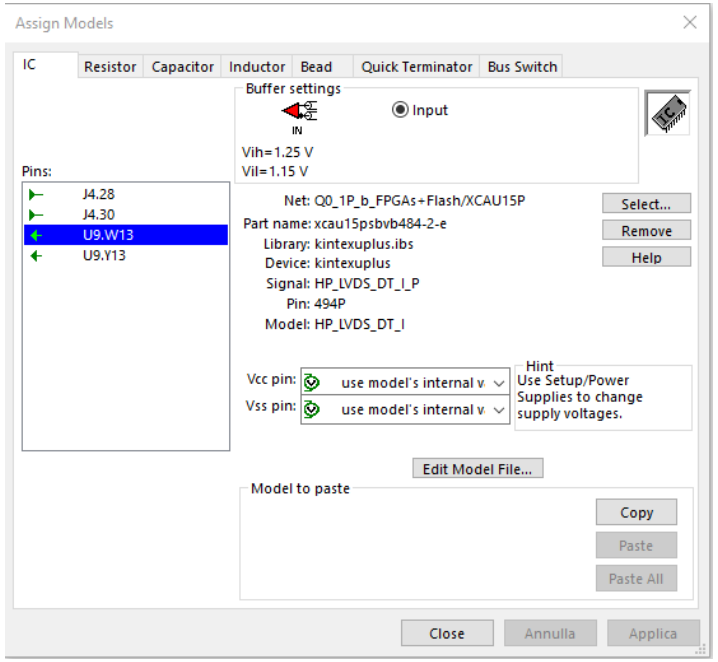
ALCOR Q0_1b lane simulation @800MHz (UI=1.25ns)



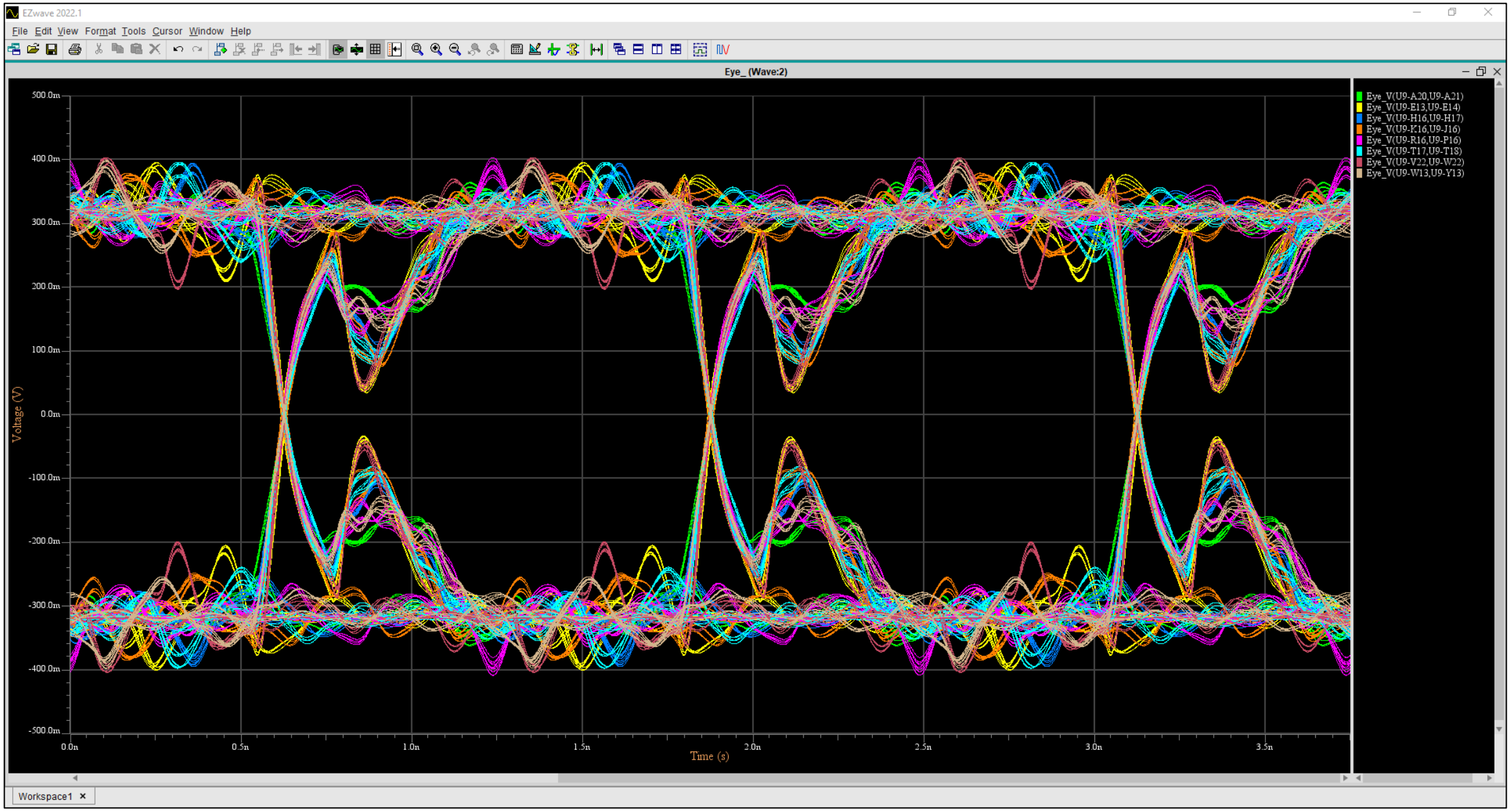


Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Mon Apr 7 11:23:55 2025	U9.W13 (at pin)/U9.Y13 (at pin)	0	Passed	0.26	0.208404	0.882213	0.586093

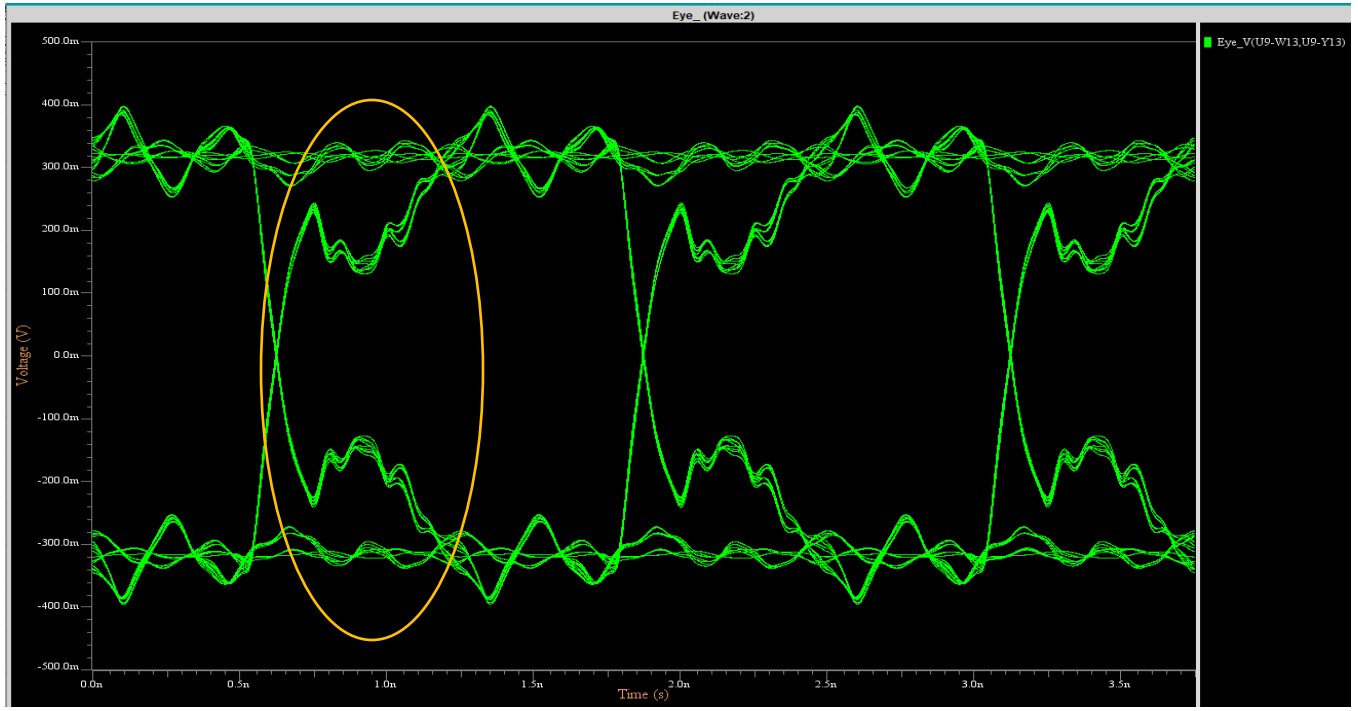




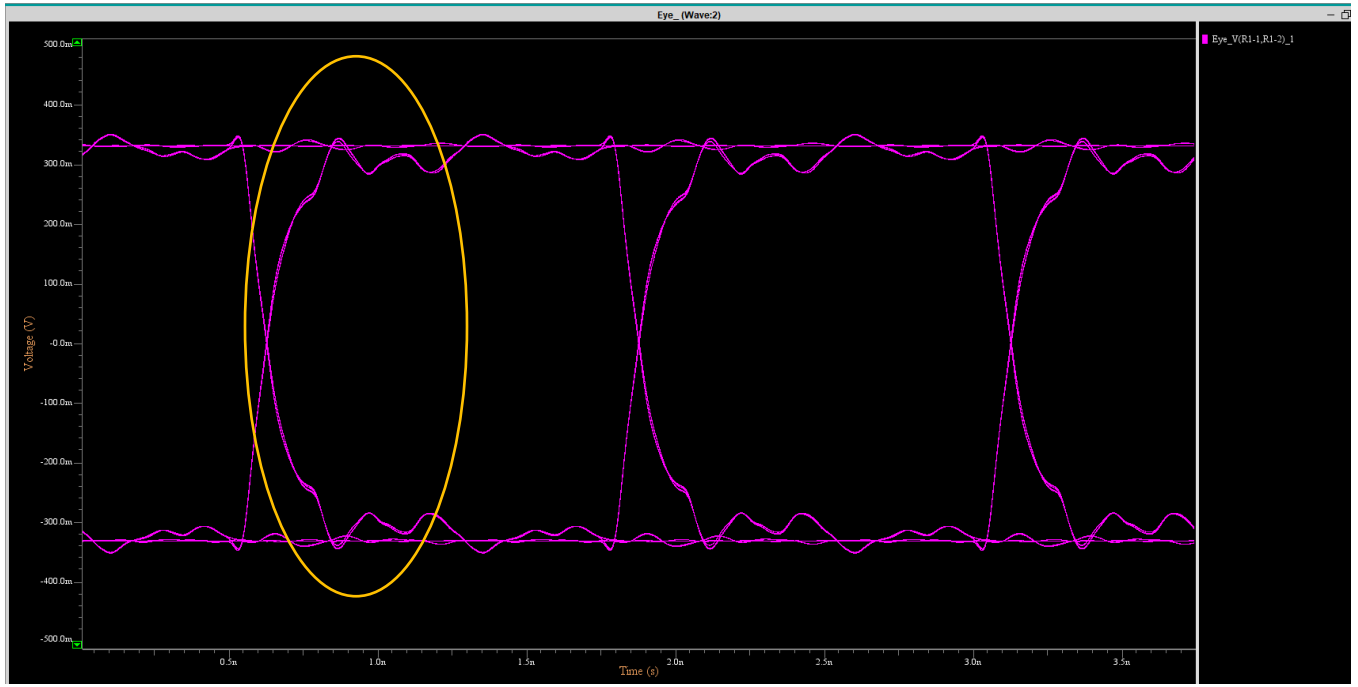
8 stacked eyes of ALCOR BUS lanes (Q0_xt,Q0xb)



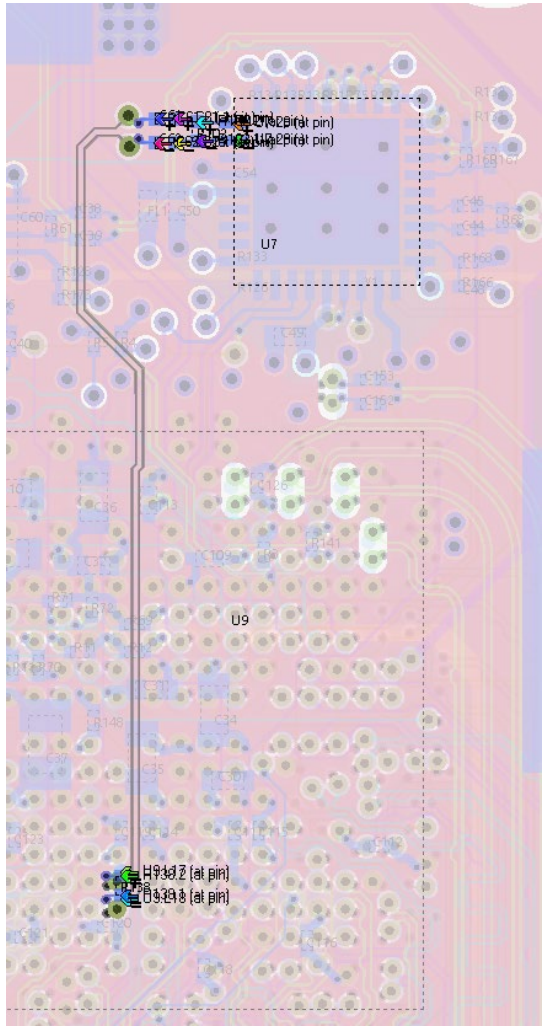
Differential probe on **ARTIX pins** receiving one lane of the **ALCOR bus @800MHz (1.25ns)** (IBIS model kintexuplus.ibs)

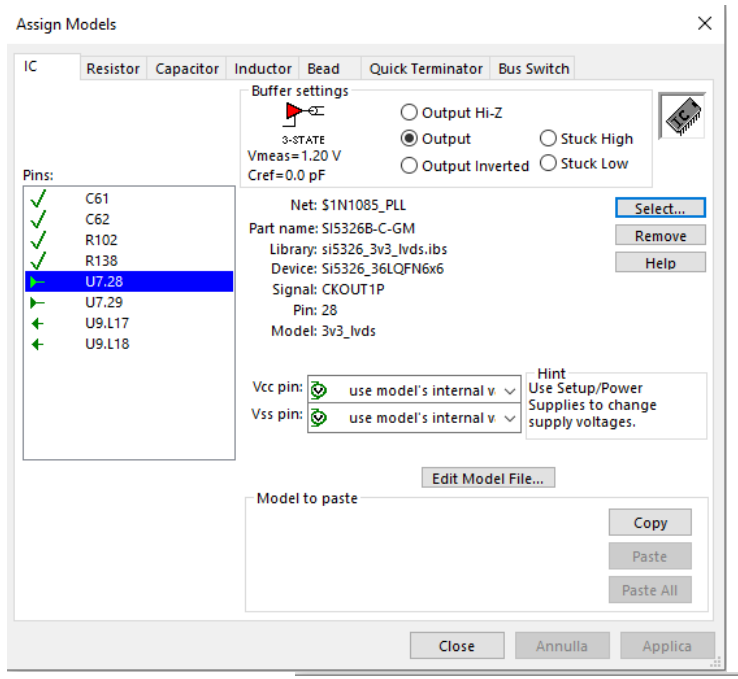


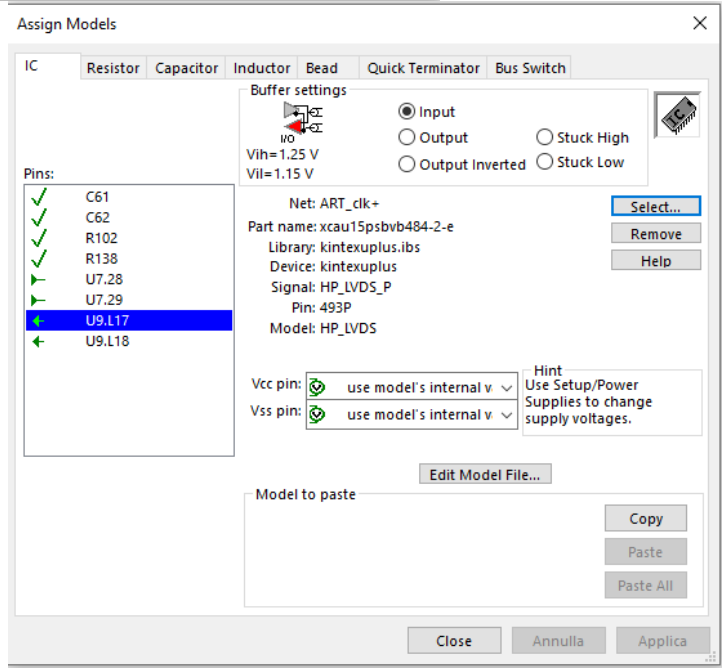
Differential probe **on 100 ohm resistor** that replaces the ARTIX pins receiving one lane of the **ALCOR bus @800MHz (1.25ns)**



- ART_clk+/ART_clk-
- 394MHz
- Driver: U7/28,29 IBIS model: Si5326_3v3_lvds.ibs
- Receiver: U9/L17,L18 IBIS model: kintexuplus.ibs

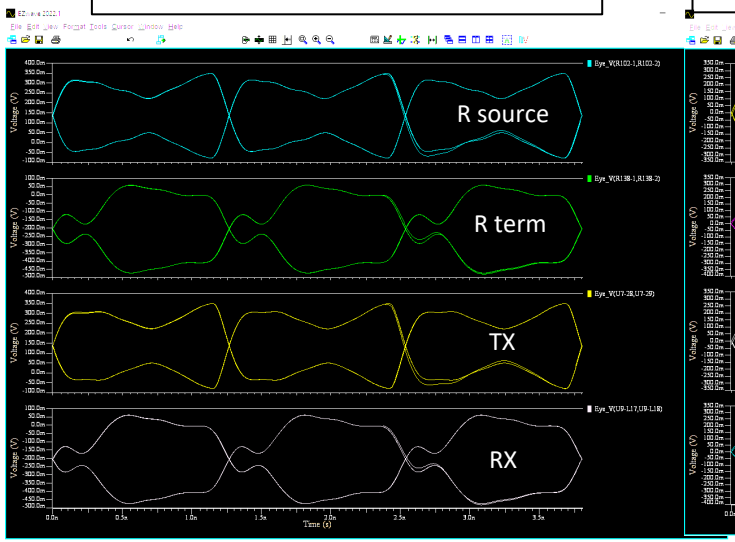




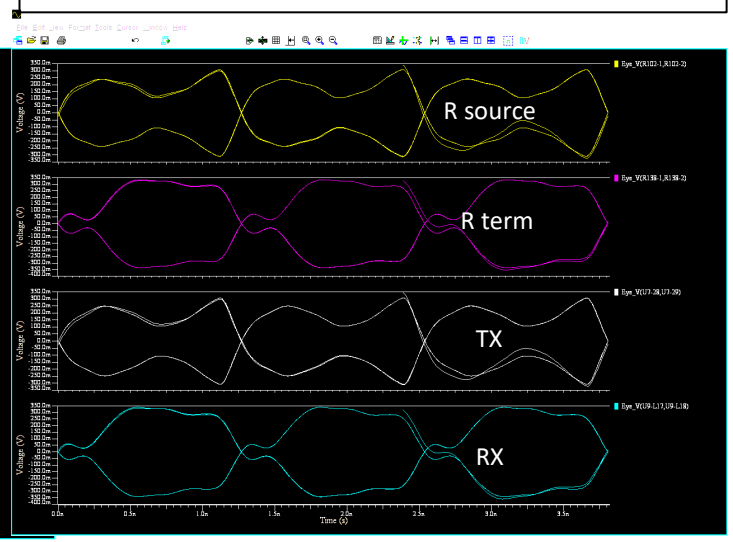


ART_clk+/ART_clk- 394MHz

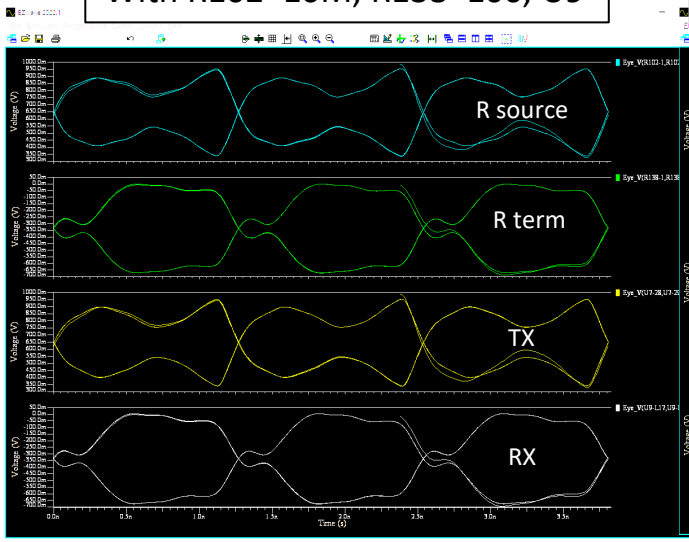
With R102=100, R138=100, U9



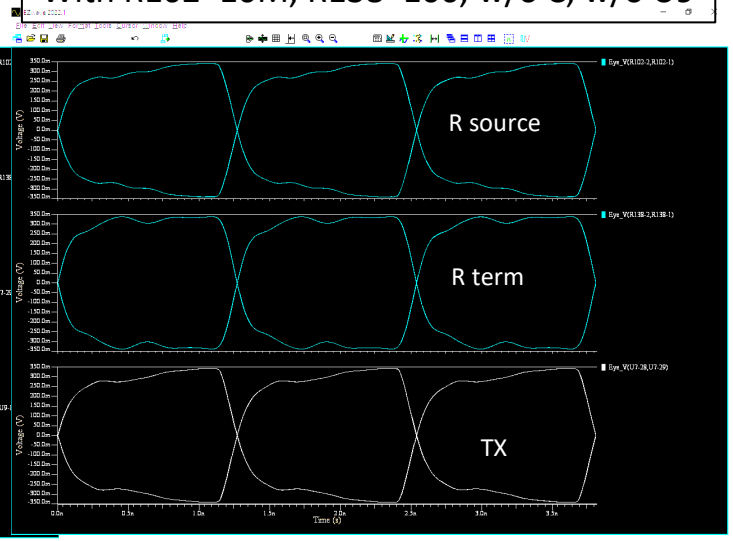
With R102=10M, R138=100, w/o C, with U9



With R102=10M, R138=100, U9



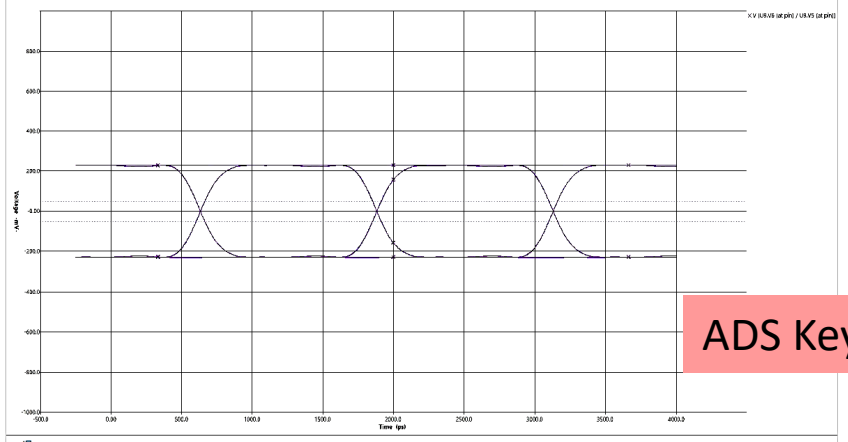
With R102=10M, R138=100, w/o C, w/o U9



EYE DIAGRAM ART_clk+/ART_clk-

Datarate	Model Driver	Model Receiver
788Mbps	3v3_lvds	HP_LVDS

OSCILLOSCOPE



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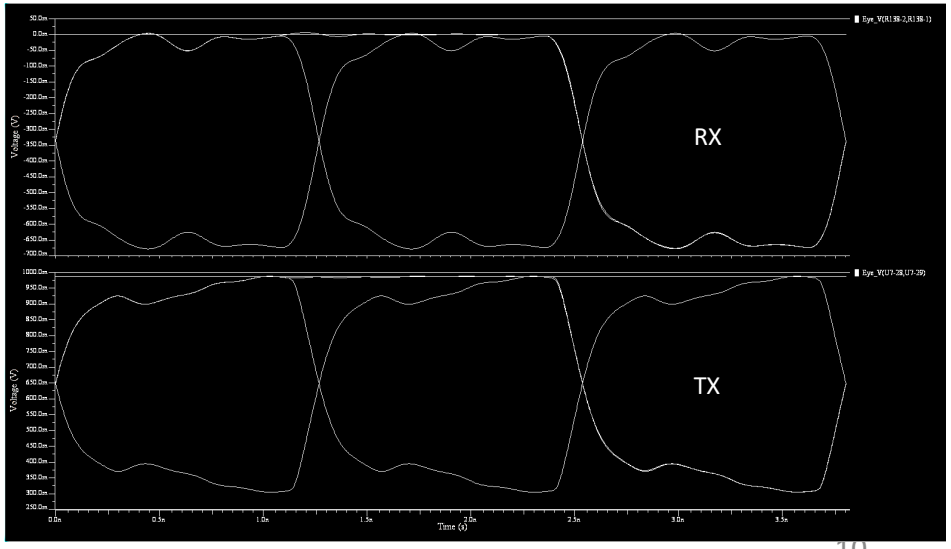
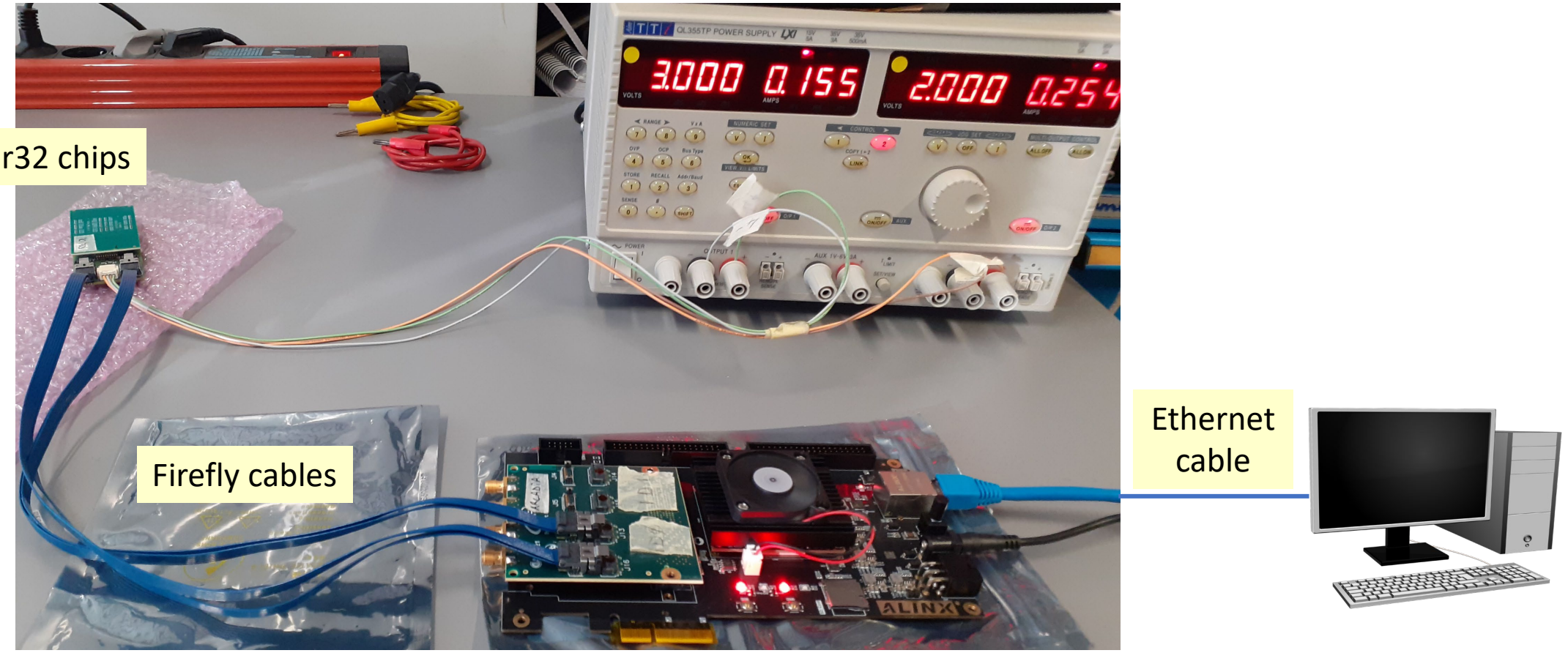
www.artel-srl.com

ADS Keysight

With R102=10M, R138=100, w/o U9



Firmware design: Artix – Alcor interface



In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI and we can correctly receive the data

Artix – Alcor interface: data decoding tests

```
Programming 0
-------- ALCOR #  0  Complete Setup
KC705 mode set to config
Resetting fifos for ALCOR #  0
Alcor reset and lanes alignment
[AlcorLib] Loading conf from  /home/eic/alcor/alcor-utils/conf
 ------------- Setup chip #  0  -----------------
 Lane # : 0  8bit-align    OK   32bit-align    OK
 Lane # : 1  8bit-align    OK   32bit-align    OK
 Lane # : 2  8bit-align    OK   32bit-align    OK
 Lane # : 3  8bit-align    OK   32bit-align    OK
Enabled lanes for readout 0xf
Setting Alcor registers to default
Setting ECCR to:  0xb01b
Executing custom BCR setup
Loading BCR file  /au/pdu/conf/bcr/standard.bcr for chip #  0 ....
Loaded configuration for  8  Bias Control Registers
Executing custom PCR setup (channel ON/OFF driven by PCR file & mask)
Loading PCR file  /au/pdu/conf/pcr/maxthreshold.pcr for chip #  0  Mask 4294967295 ....
Loaded specific configuration for  32 channels
Sending test pulse to reset pixel logic
------ End of configuration
kc705-192 chip-0 lane-0: 320014684 Hz
kc705-192 chip-0 lane-1: 319977680 Hz
kc705-192 chip-0 lane-2: 320308341 Hz
kc705-192 chip-0 lane-3: 320462234 Hz
```

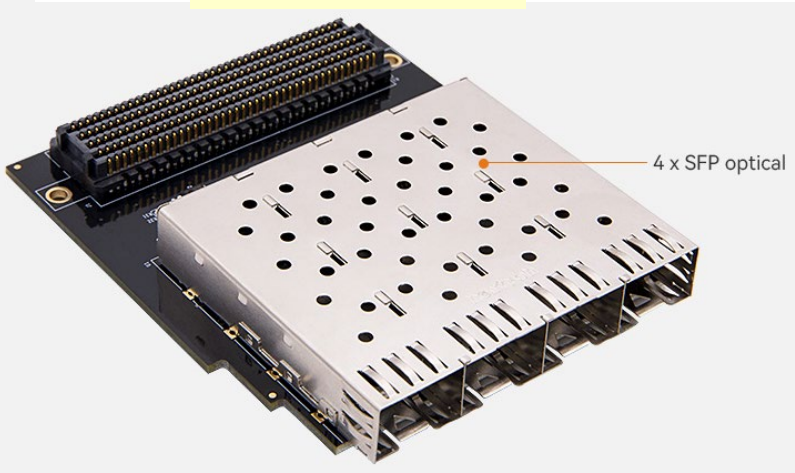
from February 2025 meeting

Firmware design

AXAU15 FPGA Dev Board & Kit with AMD Artix US+ XCAU15P

Alinx

FMC SFP board



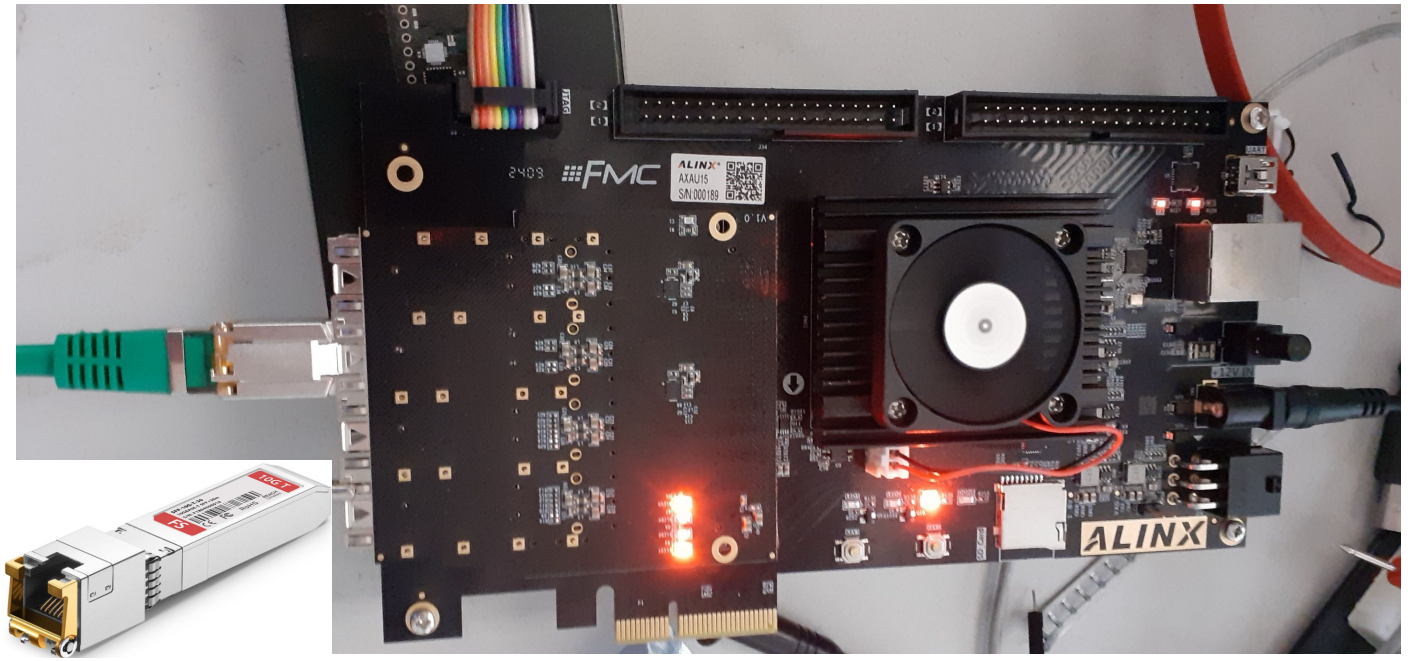
This commercial board hosts the same FPGA as the RDO (AU15P), but with a different package: we are using it to perform firmware design and test before the first RDO board is available

Firmware design: Artix – SFP interface

from February 2025 meeting

Ethernet cable

Alinx + FMC SFP board



GBIC SFP with RJ45 connector

In order to mimic the Artix – VTRx+ interface, we implemented the IPbus firmware on the FPGA and tested it

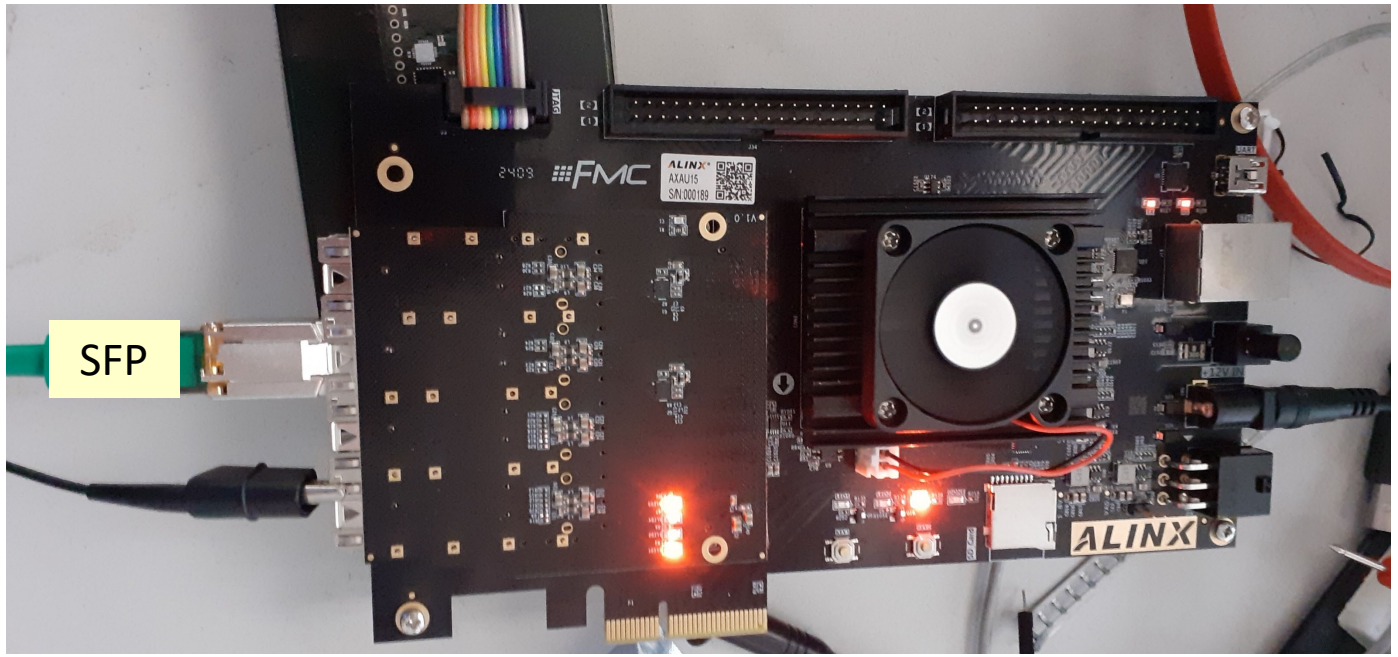
Firmware design: Artix – SFP interface

now working on

NIC card

optical cable

Alinx + FMC SFP board



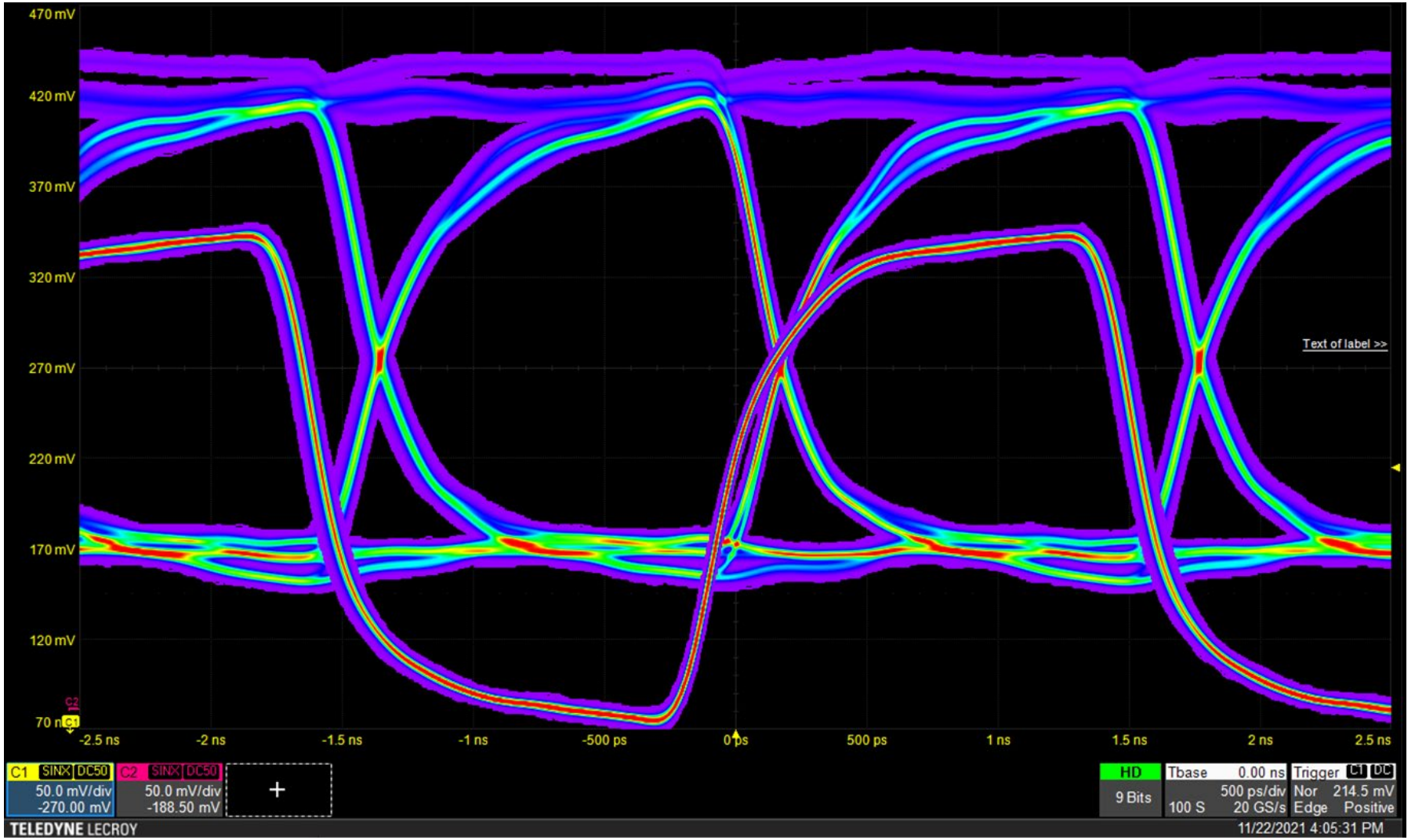
The goal is to have a working IPbus firmware on the FPGA working over optical fiber

Next steps

- learn as much as we can from the Alinx board until the RDO is available
- prepare a firmware for the RDO board to start the tests as soon as the board is ready

Thanks!

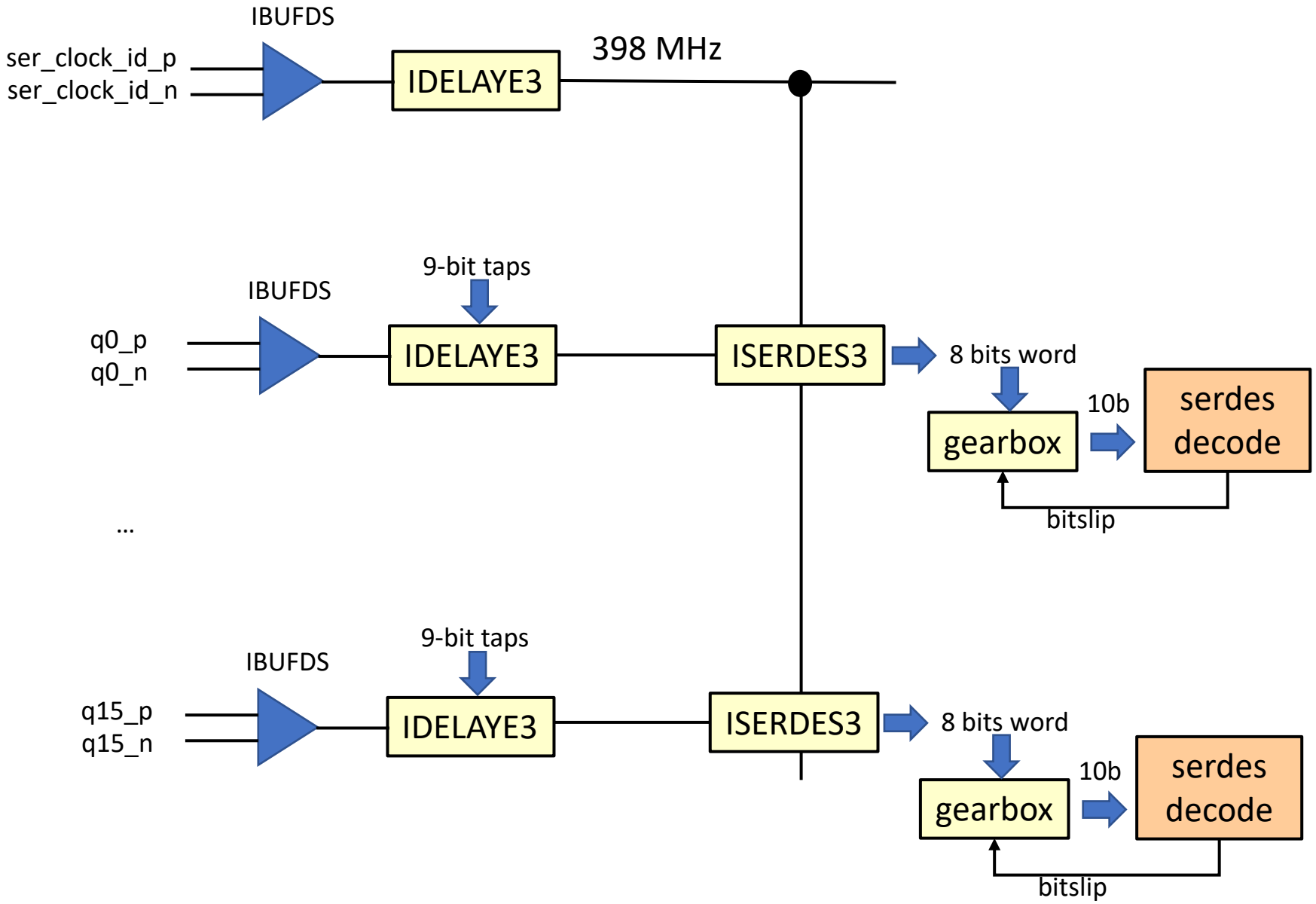
Backup



data

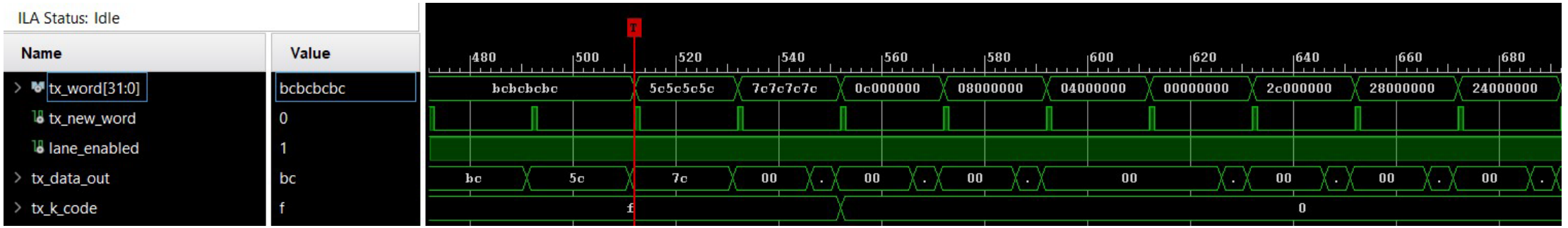
ser_clock

Average tap delay @ 300 MHz = 2 ps, 512 taps available
for a total span of ~1.1 ns
The tap value is chosen via SW, then the sync procedure is run (bitslip mechanism)


IBUFDS
ser_clock_id_p
ser_clock_id_n
IDELAYE3
398 MHz
9-bit taps
IBUFDS
q0_p
q0_n
IDELAYE3
ISERDES3
8 bits word
10b
gearbox
serdes decode
bitslip
...
9-bit taps
IBUFDS
q15_p
q15_n
IDELAYE3
ISERDES3
8 bits word
10b
gearbox
serdes decode
bitslip

Artix – Alcor interface: data decoding tests

bitslip mechanism for data synchronization



32-bit rollover words coming from Alcor