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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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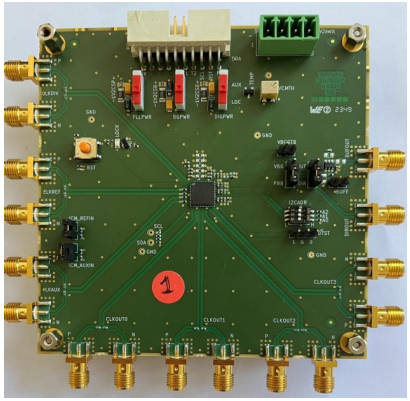
STATUS OF THE PROTOTYPES

PRISMEv1 prototype (PLL test chip)

- Updates done on the PLL block: deterministic jitter noise, radiation hardness, lower internal frequency, inclusion of CDR for unified input interface, compatibility with lpGBT input frequency
- PRISMEv1 prototypes produced and at CERN, packaging right when chips arrive at Saclay, test cards PCB under production



SALSA1 prototype

- SALSA1 tested from January, I2C interface working, slow-control registers responding correctly
- New test-cards in production with SALSA1 soldered on them, instead of socket
- Systematic measurements ongoing on front-end - ADC performance
- Specific tests on ADC performance started, no result yet
- New staff engineer hired at Saclay working on tests, then on SALSA2 developments

CURRENT STATUS: SALSA2

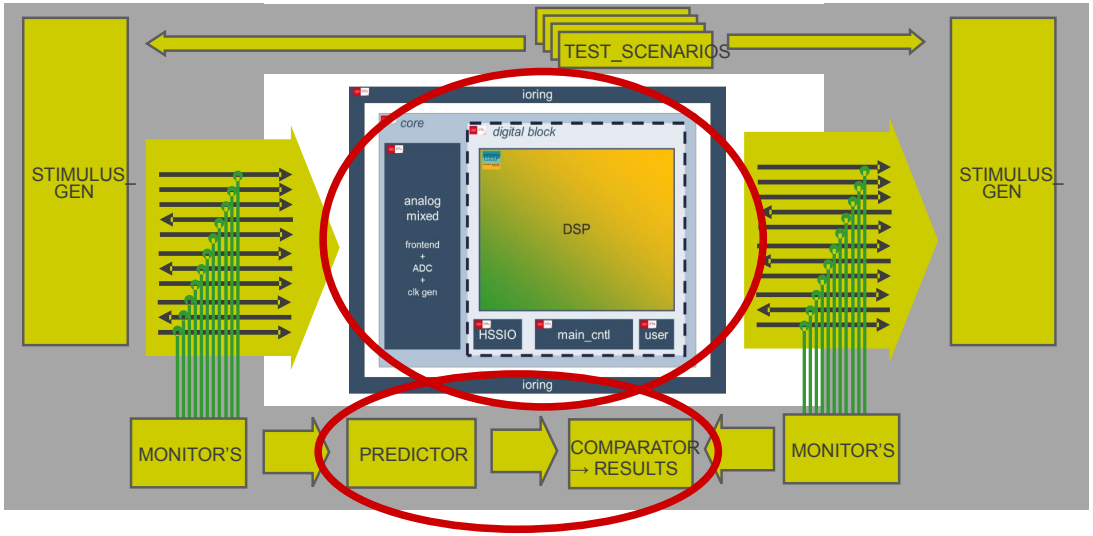
SALSA2 development status

- Work ongoing on HDL code of DSP modules
- Some modules almost ready: digital filtering, pedestal correction, baseline following algorithm, pipeline management zero suppression, PLL, registers, power-on reset, data scrambling/descrambling + Reed-Solomon protection
- Others ongoing: common mode correction, packet building, multiplexer, data serialization
- UVM environment under development, 1st version of predictor DSP model done
- Integration of digital processing modules with other blocks started, floor plan under study
- Packaging under study, planed to be identical to the final SALSA one

Timeline

- Still a lot of works ahead:
  - code development of missing modules
  - code verification and validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission not expected before October 2025 (last MPW run slot of the year)
- Tests in 2026
- Distribution to users before end 26

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done
- Test card production → done
- Performance evaluation → ongoing

Generic R&D program for EIC project (new 65nm PLL block)

- Fully done, follow-up with PRISMEv1 new prototype (not financed by this program)

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming October 2025
- Beginning of SALSA2 tests → 1st semester 2026

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming December 2025
- SALSA3 submission → 2nd semester 2026
- Performance evaluation → 1st semester 2027

Very next steps

- SALSA1 tests → ongoing
- New PRISMEv1 chip → produced, packaging and test-cards production in May
- SALSA2 development → in progress