
Brookhaven
National Laboratory
U.S. DEPARTMENT OF
ENERGY
Cryogenic Readout Electronics Systems for
Liquid Argon TPCs in Neutrino Experiments
Shanshan Gao
10/17/2023
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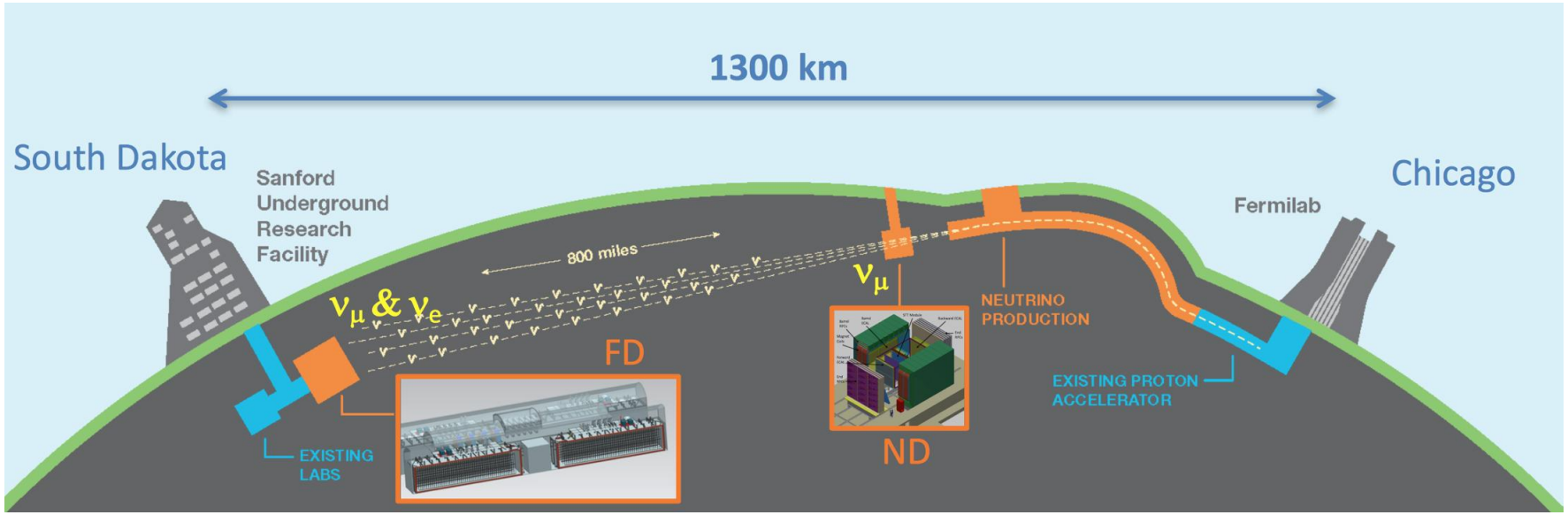
Content

- **Liquid Argon TPC in Neutrino Experiments**
- Cryogenic Readout Electronics (CE)
  - Advantages
  - A Brief History
- Cryogenic Readout Electronics Systems Applied in LArTPCs
  - ProtoDUNE-SP
  - DUNE Far Detector

  } **Long Baseline Neutrino Experiments**
- Summary

Long Baseline Neutrino Program: LBNF/DUNE



An international flagship experiment to unlock the mysteries of neutrinos

Three major discovery areas

Origin of Matter

DUNE scientists will look at the differences in behavior between neutrinos and antineutrinos, aiming to find out whether neutrinos are the reason the universe is made of matter.

Unification of forces

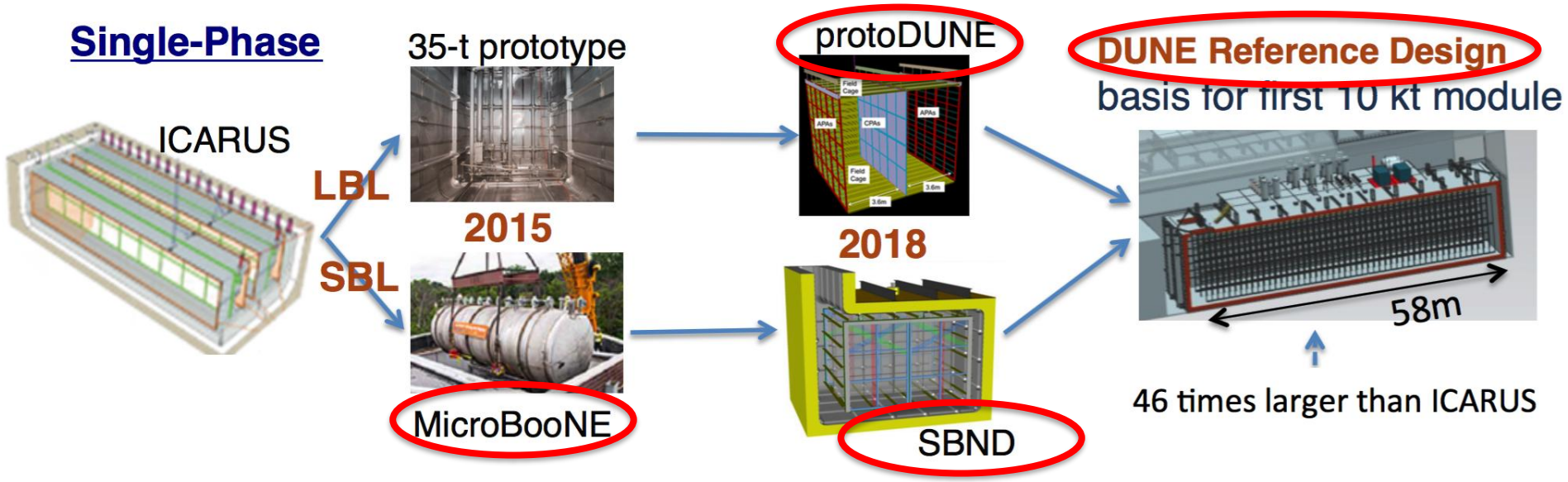
DUNE's search for the signal of proton decay—a signal so rare it has never been seen—will move scientists closer to realizing Einstein's dream of a unified theory of matter and energy.

Black hole formation

DUNE will look for the gigantic streams of neutrinos emitted by exploding stars to watch the formation of neutron stars and black holes in real time, and learn more about these mysterious objects in space.

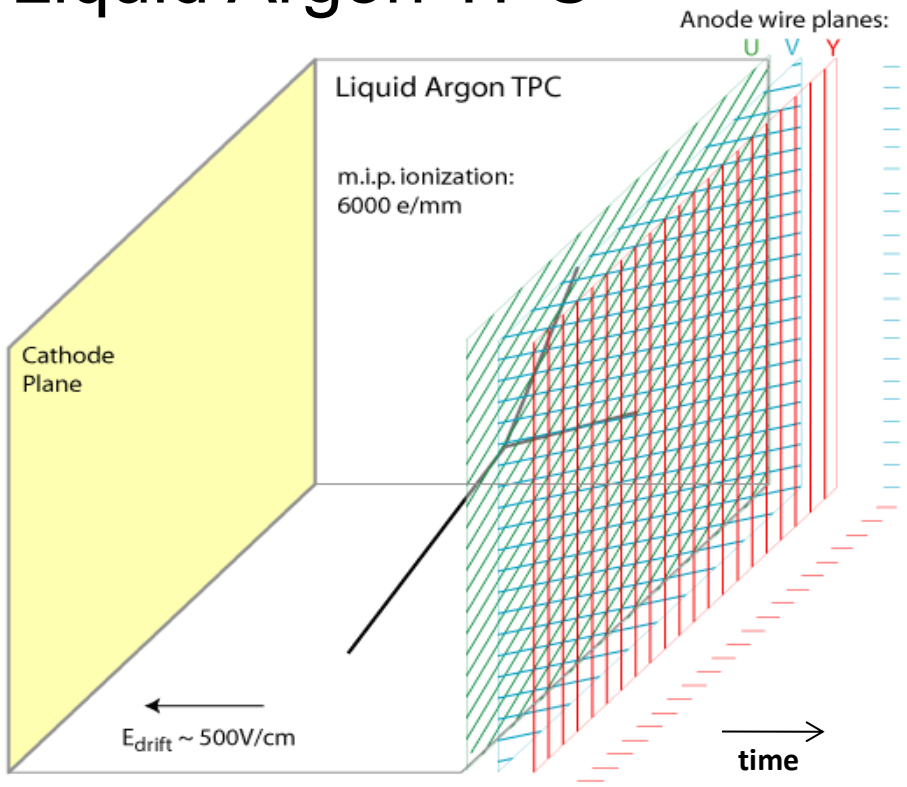
Development of LArTPC for Neutrino Experiments

- **BNL is leading TPC readout electronics *SYSTEM* design**
  - Including MicroBooNE and SBND as part of the Short Baseline Neutrino Program



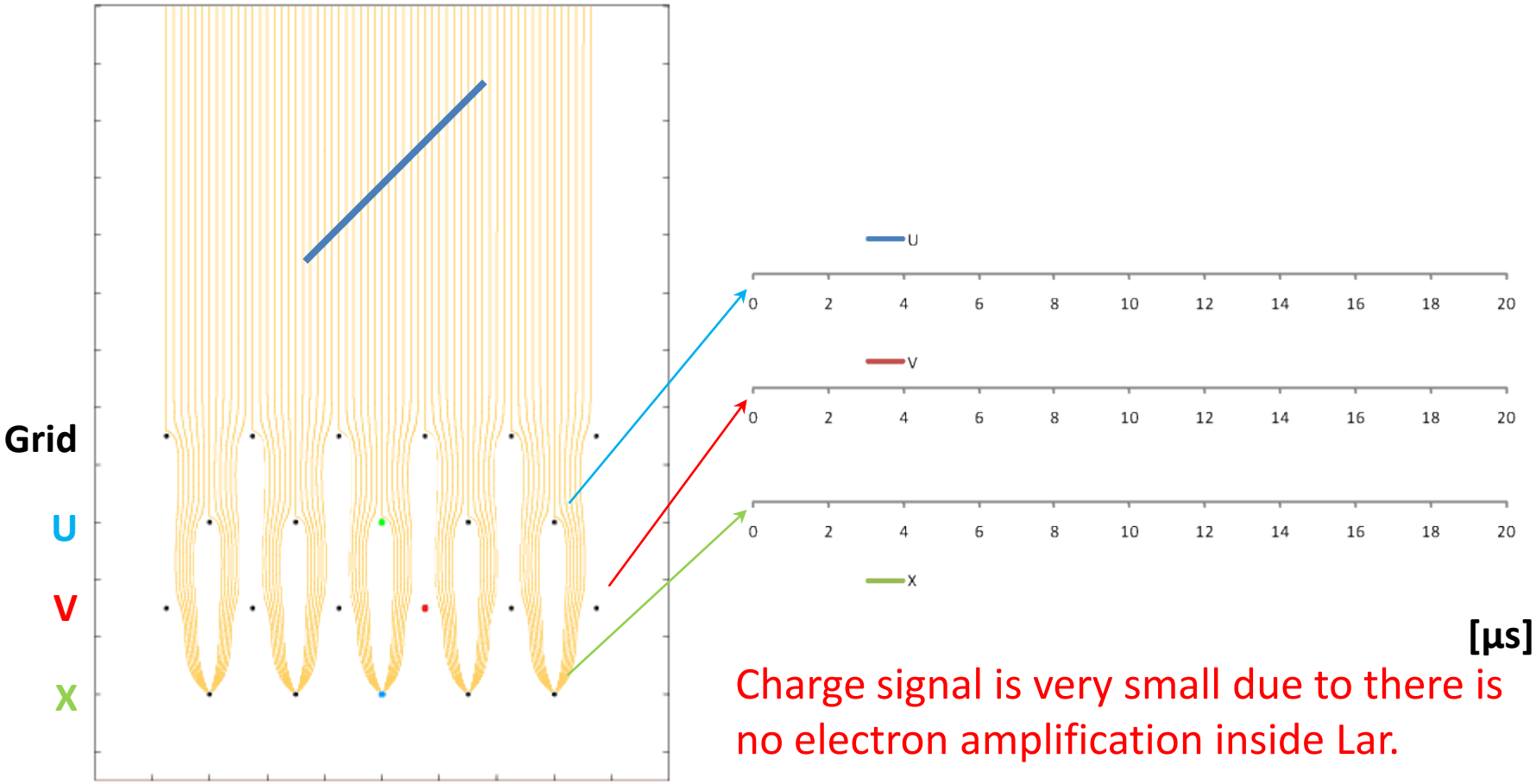
Liquid Argon TPC

Charged particles passing through detector ionize the argon atoms, and the ionization electrons drift in the electric field to the anode wall on a timescale of milliseconds. The anode consists of layers of active wires forming a grid.



- 3 Wire Plane readout with Excellent Space and Energy resolution
- 3D-imaging: full event topology reconstruction
- Higher sensitivity to neutrino physics and for some of the proton decay channels (e.g. p → K**ν**)

Signal Formation:
Induced Signals from a Track Segment



Charge signal is very small due to there is no electron amplification inside Lar.

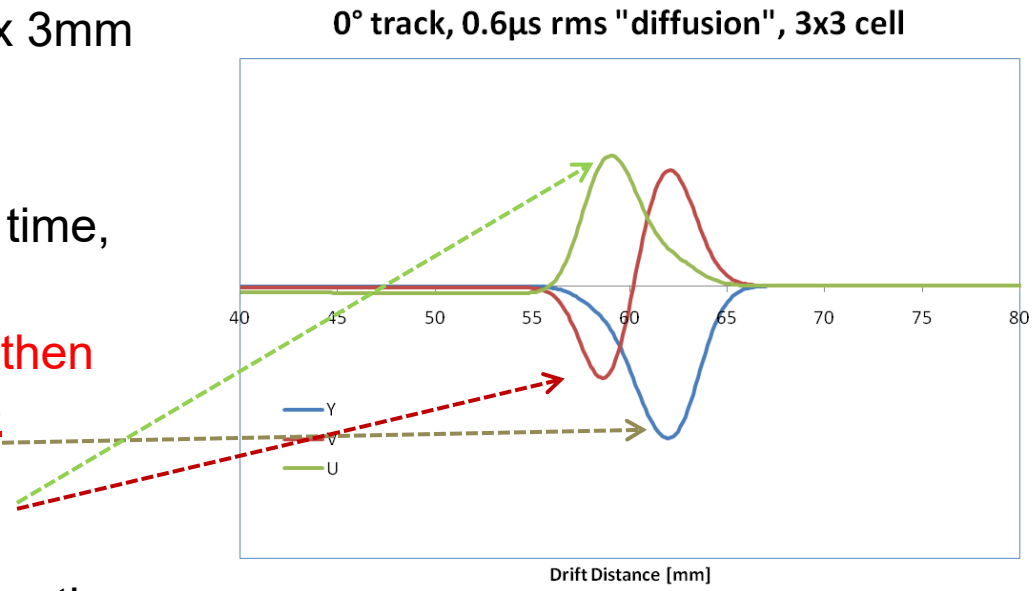
DUNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian to mimic diffusion

Signals in LAr TPC

- **Charge signal is very small**
  - There is no electron amplification inside LAr
  - A 3mm MIP track should create 210keV/mm x 3mm /23.6eV/e = 4.3fC
  - After a 1/3 initial recombination loss: ~2.8fC
  - Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368
  - The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for **the "collection signal"**
  - The induction signals are smaller
  - The time scale of TPC signals is determined by the **wire plane spacing** and **electron drift velocity**, (~1.5 mm/μs at 500 V/cm)

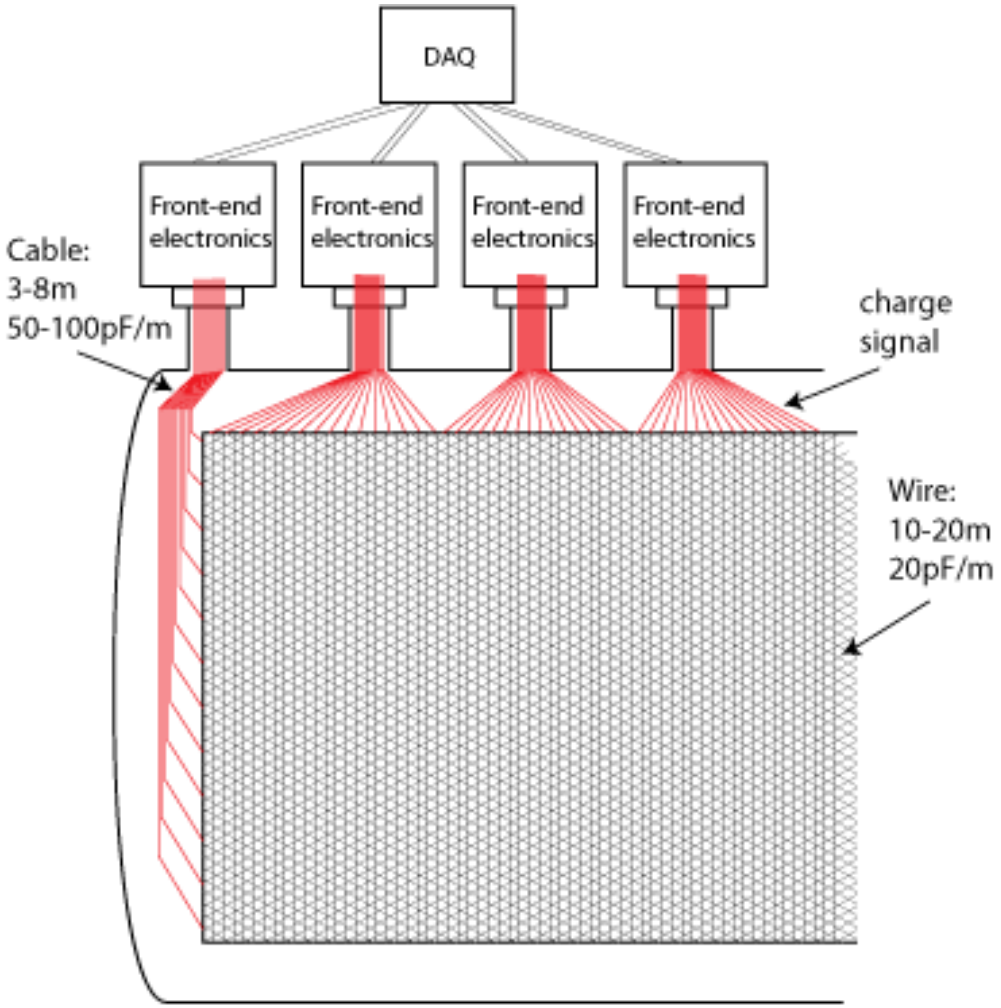
Noise Sensitive!

Induced Current Waveforms on 3 Sense Wire Planes



S:N requirement to "distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume."

“Warm” Electronics



- A typical readout configuration with warm electronics: long cables connect the sense wires to the FEE, resulting in high capacitance and large electronics noise.
- To reduce the cable length, one has to implement cold feedthroughs below the liquid level, which increases the cryostat complexity.

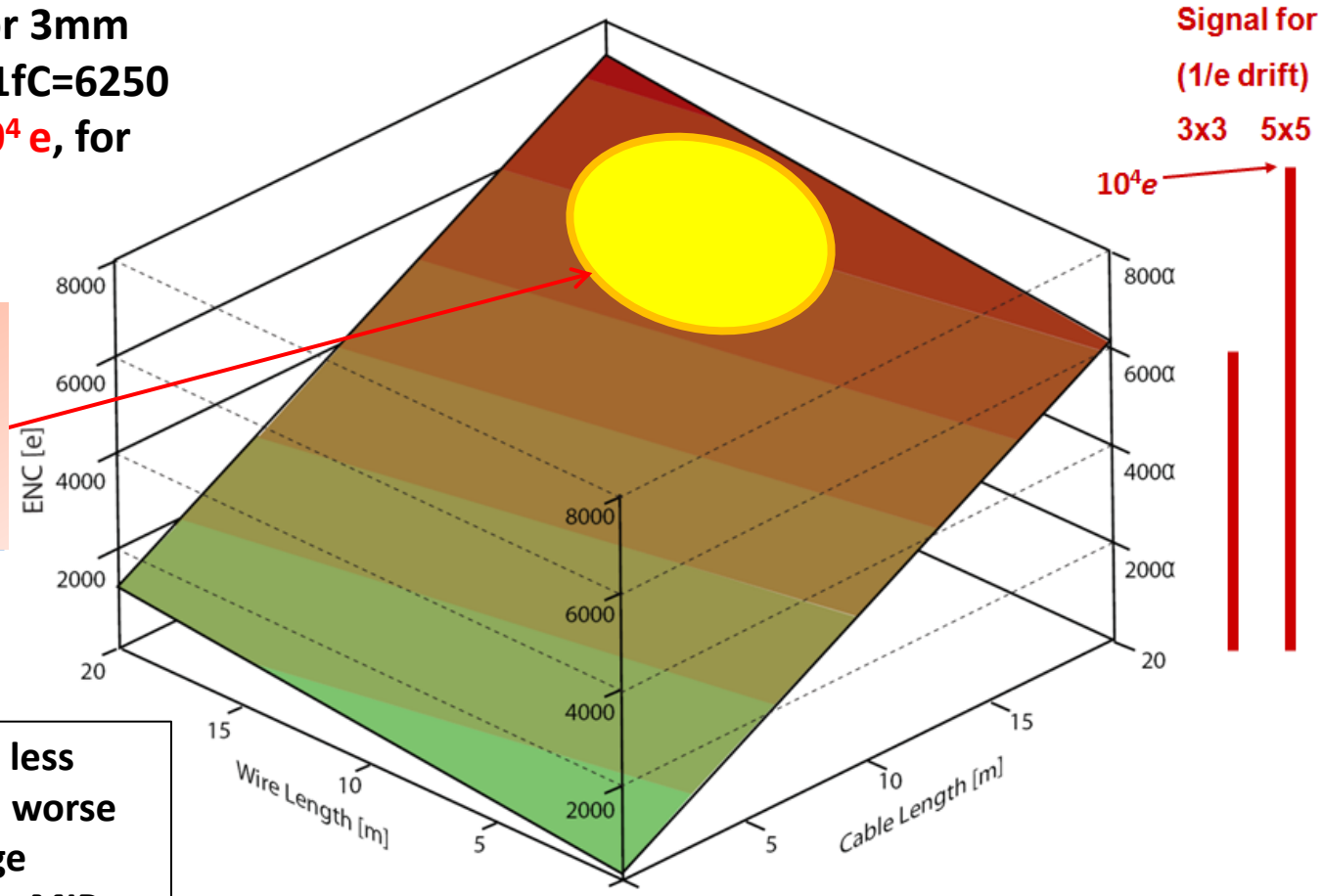
“Warm” Electronics

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length

MIP Signal for 3x3 and 5x5 mm Sense Wire Spacing

The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for the “collection signal”

10kton DUNE LArTPC with warm electronics (300K) ENC ~$6x10^3$ e rms



DUNE: Total ENC shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.

Cryogenic Electronics is the Optimal Solution for Large LArTPCs

Cold electronics for "Giant" Liquid Argon Time Projection Chambers

1st International Workshop towards the Giant Liquid Argon Charge Imaging Experiment (GLA2010)

Veljko Radeka[1*], Hucheng Chen[1], Grzegorz Deptuch[2], Gianluigi De Geronimo[1], Francesco Lanni[1], Shaorui Li[1], Neena Nambiar[1], Sergio Rescia[1], Craig Thorn[1], Ray Yarema[2] , Bo Yu[1]

[1] Brookhaven National Laboratory, Upton, NY 11973-5000, USA

[2] Fermi National Laboratory,

[*]Correspondence, e-mail: radeka@bnl.gov

Abstract. The choice between cold and warm electronics (inside or outside the cryostat) in very large LAr TPCs (>5-10 ktons) is not an electronics issue, but it is rather a major cryostat design issue. This is because the location of the signal processing electronics has a direct and far reaching effect on the cryostat design, an indirect effect on the TPC electrode design (sense wire spacing, wire length and drift distance), and a significant effect on the TPC performance. All these factors weigh so overwhelmingly in favor of the cold electronics that it remains an optimal solution for very large TPCs. In this paper signal and noise considerations are summarized, the concept of the readout chain is described, and the guidelines for design of CMOS circuits for operation in liquid argon (at ~89 K) are discussed.

Veljko Radeka

- https://www.bnl.gov/newsroom/news.php?a=220971

Veljko Radeka joined Brookhaven Lab's Instrumentation Division in 1962 where he has held numerous roles, including Division Head. For more than four decades he led and positioned the division as a world class organization. His unique contributions to the field of instrumentation are internationally recognized and encompass a broad range of scientific applications. Veljko is still a very active member of the scientific community, and his work has inspired colleagues and other researchers around the world.

Brookhaven's Veljko Radeka Recognized by International Committee for Future Accelerators

Radeka becomes one of the first recipients of the ICFA Instrumentation Award in its inaugural year

December 7, 2022

“I always felt that the purpose of instrumentation is to make Brookhaven Laboratory competitive,” said Radeka. “We want to **provide these scientists with the best tools** so that they can perform important work that is the basis of all nuclear and particle physics.”

Hucheng Chen

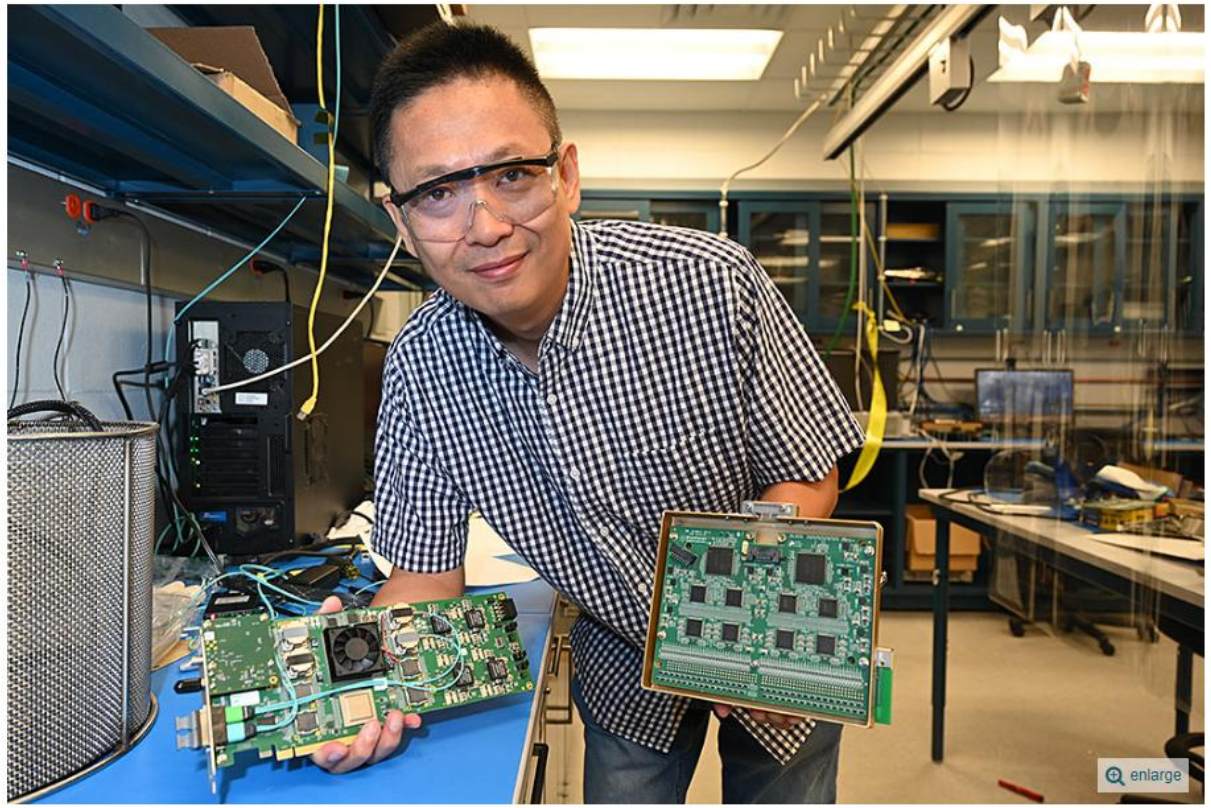
- https://www.bnl.gov/newsroom/news.php?a=221373

“Many challenges come with designing electronics that work in extreme environments,” Chen explained. “There are no readily available solutions from industries, and special R&D studies are required to address these obstacles. Over the past decade we have developed the design rules, used cryogenic models, and realized stringent test programs following the integral system design concept. This all ensures the long-term reliability of devices, which need to last for the entire lifetime of the experiment, often 20 to 30 years.”

Brookhaven Lab's Hucheng Chen Named a Battelle 'Inventor of the Year'

Honored for designing particle detector electronics that can read out signals under super cold conditions

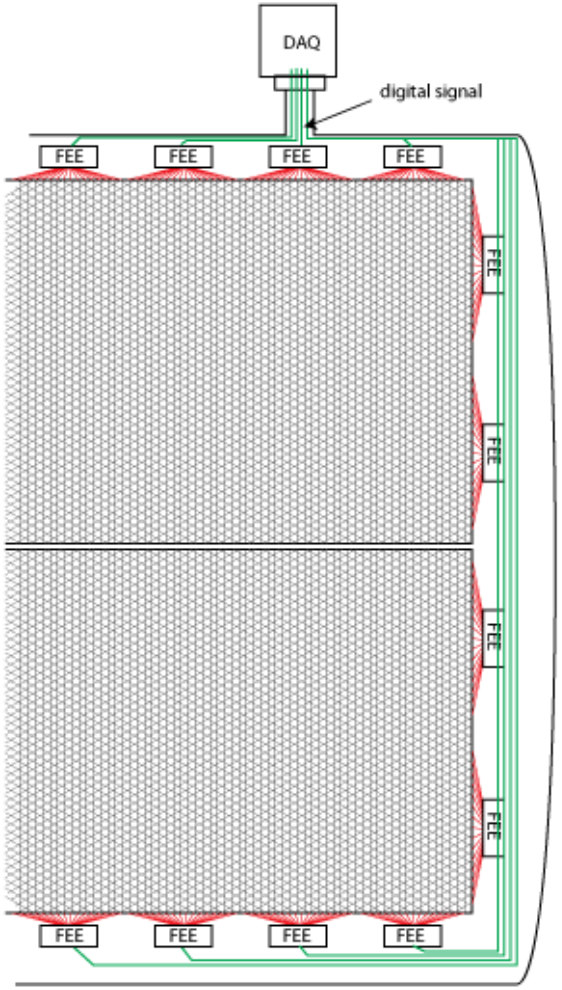
August 15, 2023



Brookhaven Lab's Hucheng Chen, named a Battelle "Inventor of the Year," shows two electronics boards he designed for particle detectors. The Front-End LInk eXchange (FELIX), shown on the left, is a readout electronics board for the ATLAS, ProtoDUNE-SP, and sPHENIX experiments. On the right is the Front-End MotherBoard (FEMB), which operates at cryogenic temperatures for DUNE.

Advantages of Cryogenic (“Cold”) Electronics

- Having front-end electronics in the cryostat, close to the wire electrodes yields the best SNR. Noise is independent of the fiducial volume.
- Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations

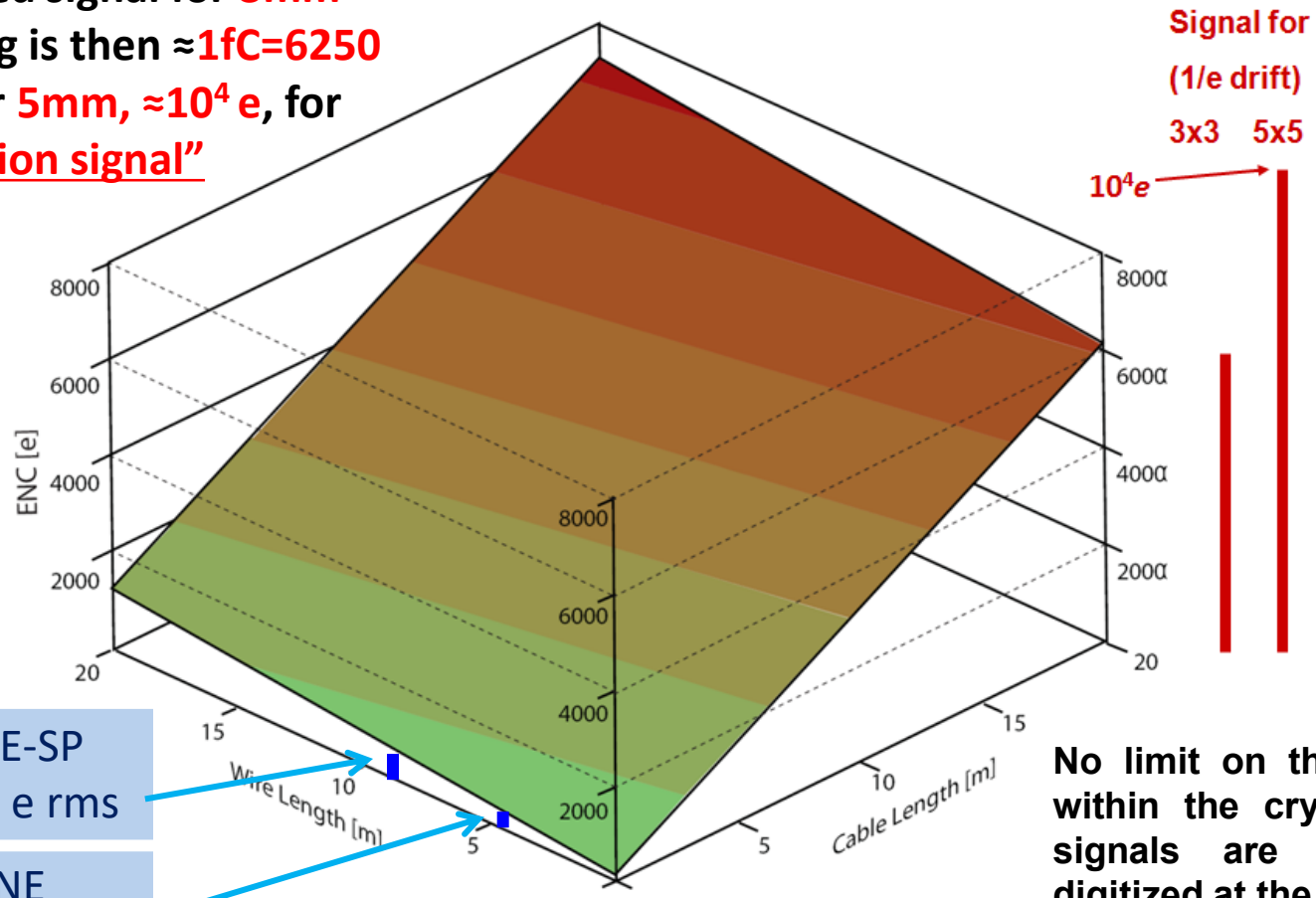


“Cold” Electronics as an Optimal Solution

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length

MIP Signal for 3x3 and 5x5 mm Sense Wire Spacing

The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for the “collection signal”

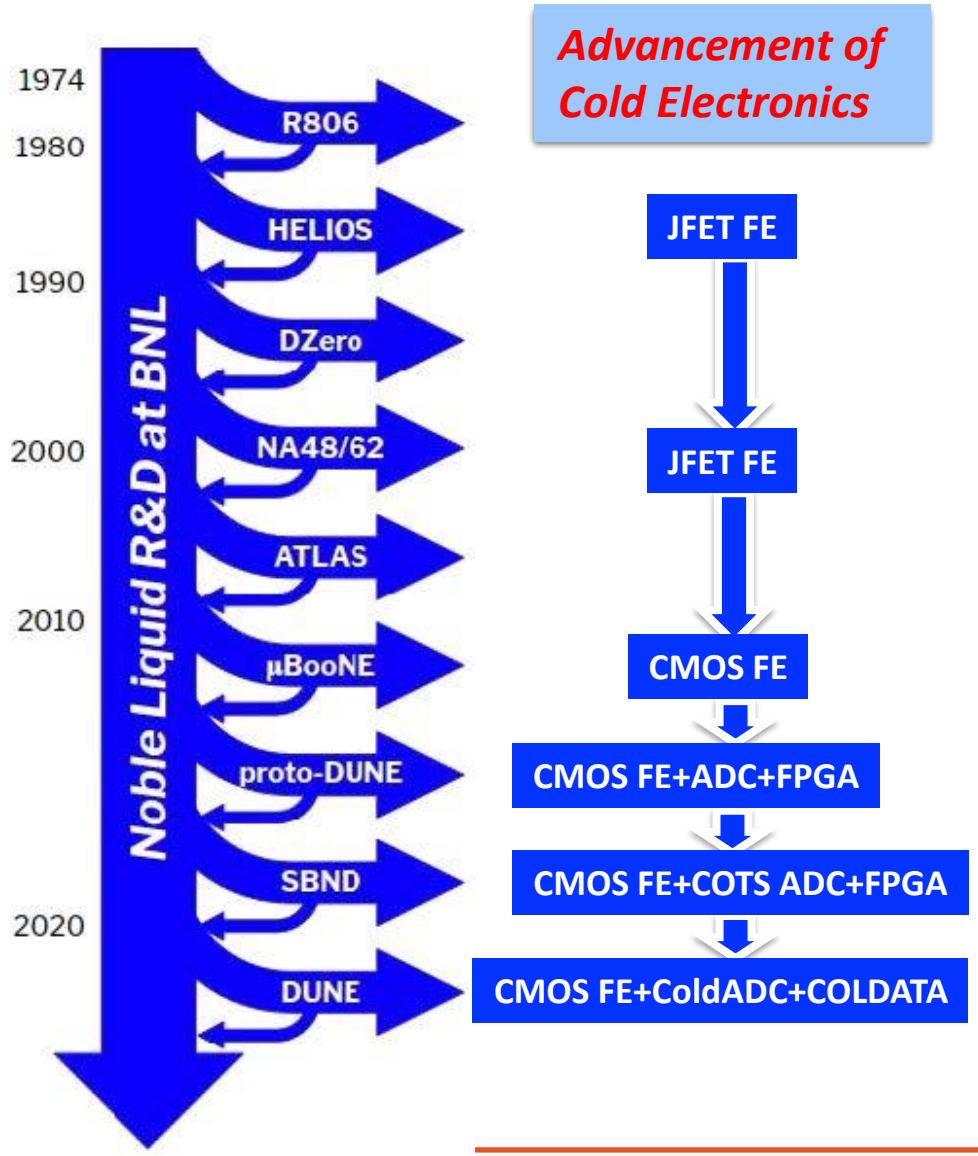


ProtoDUNE-SP
ENC ~600 e rms

MicroBooNE
ENC ~400 e rms

No limit on the cable length within the cryostat after the signals are amplified and digitized at the sense wires.

A Brief but Long History of CE Development



- BNL pioneered LAr based detector technology in 1974 [1]
- Physics/Engineering expertise which has made essential contributions to various programs, e.g. ATLAS, MicroBooNE
- Unique experience in cryogenic electronics and micro-electronics
- The R&D effort makes the experiments possible; the experiments, in turn, feed information back into the R&D process
- Cryogenic/Cold electronics development is making continuous advancement, from JFET to CMOS, from analog front-end to mixed signal ADC and FPGA
- ***A strong cold electronics team is built up as a core BNL competence, in close collaboration with other institutes, to realize various LAr TPC experiments***
- *[1] W. Willis, V. Radeka, Nucl. Instr. Methods, 120 (1974) 221*

Performance as ASIC is submerged in LN_2

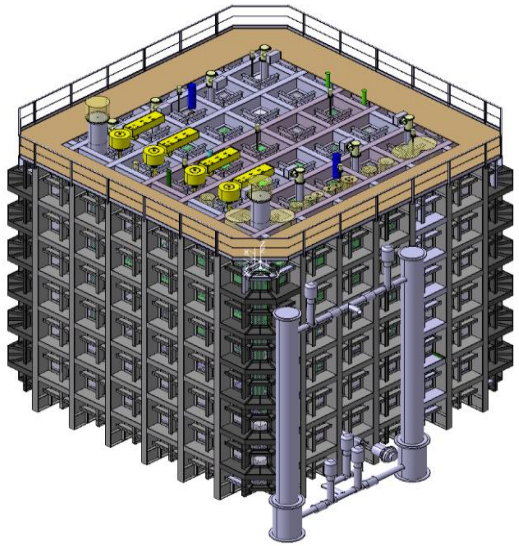
ProtoDUNEs

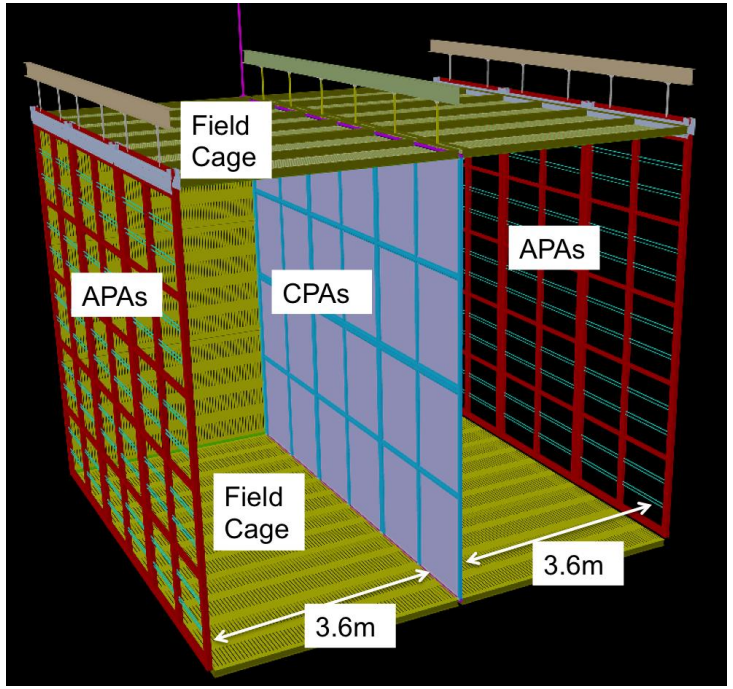
- ProtoDUNEs provide critical validation of technology, detector performance, and long-term stability

- BNL focused on ProtoDUNE-SP Cold Electronics R&D (both electrical and mechanical), production, installation and commissioning

ProtoDUNE-SP Phase I

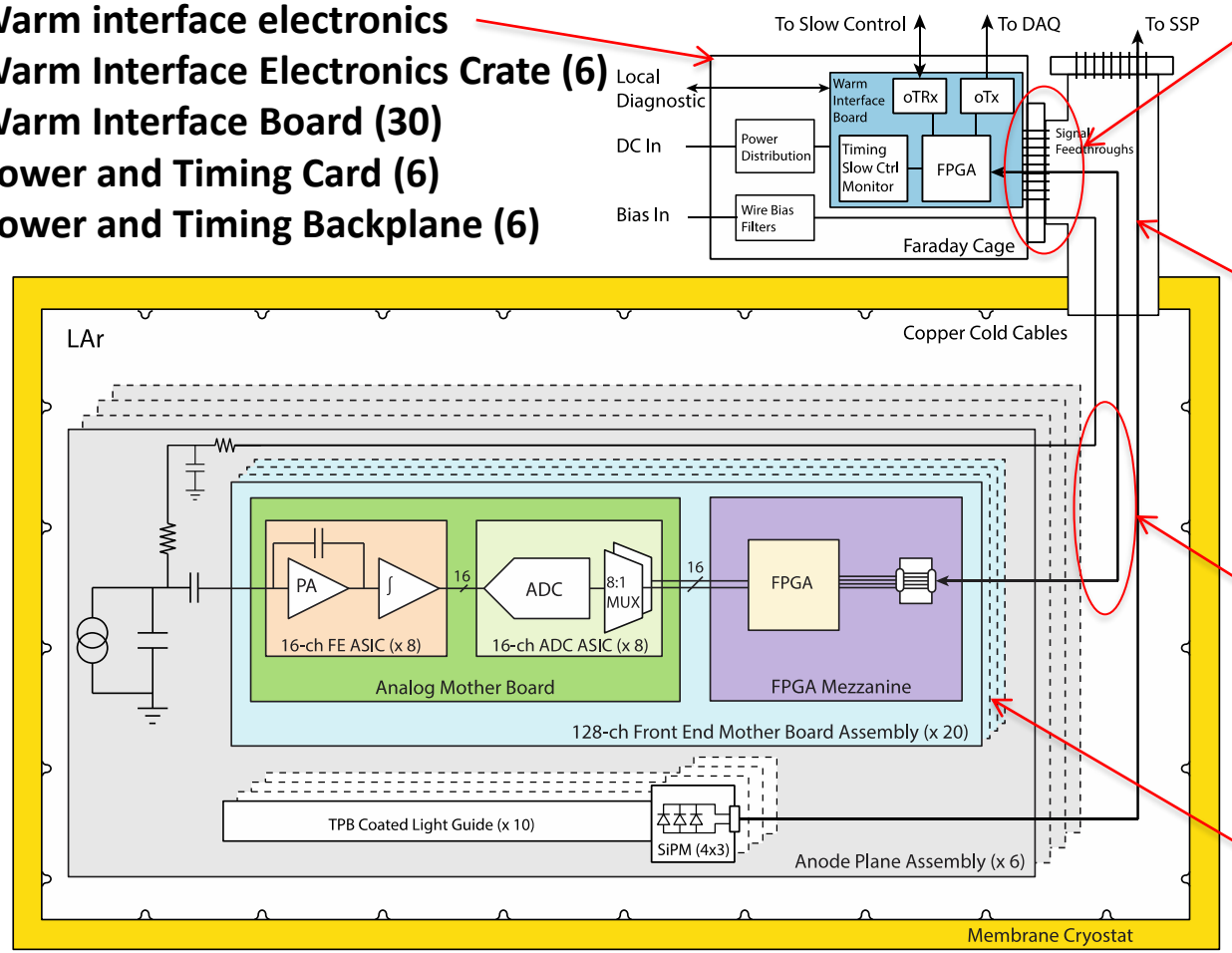
- NP04 experiment at CERN
  - 400-ton fiducial LArTPC
  - Sit in H4 beam line
- Single-phase TPC prototype
  - Use full scale components of DUNE far detector module
  - 6 full-size APAs plus 3 CPAs
    - 2 x 3.6m drift regions
  - Total 15,360 TPC channels
  - RUN I has been completed in 2020
  - RUN II is planned ~2022
- A key test of:
  - Components
  - Construction methods
  - Installation procedures
  - Commissioning
  - Detector response to particles
  - Confirm modeling and simulation





ProtoDUNE-SP Phase I Cold Electronics System

Warm interface electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



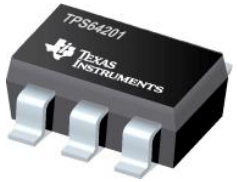
CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable
LV and data cable (120+120) to FEMB and APA wire-bias SHV cable (48)

Front End Motherboard (FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

Cold Electronics R&D

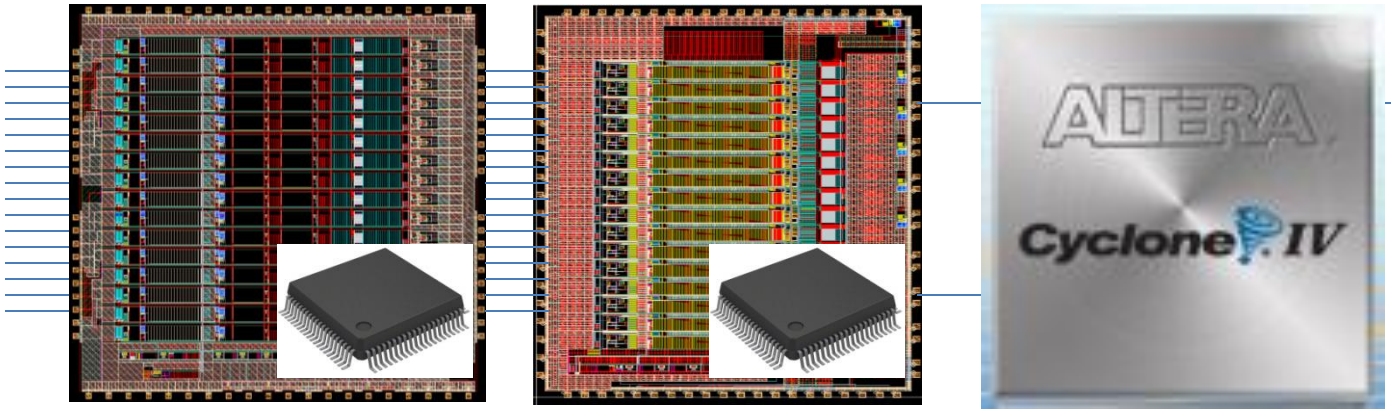


voltage regulation (COTS)
(< 100mV dropout)

Front end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.

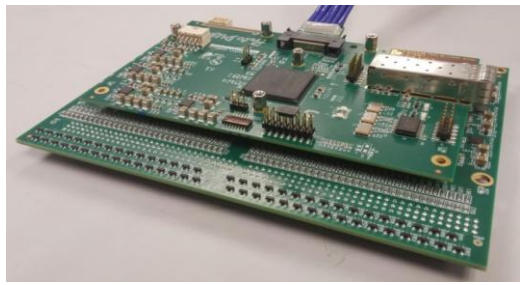


overall 128:4
multiplexing

1 x

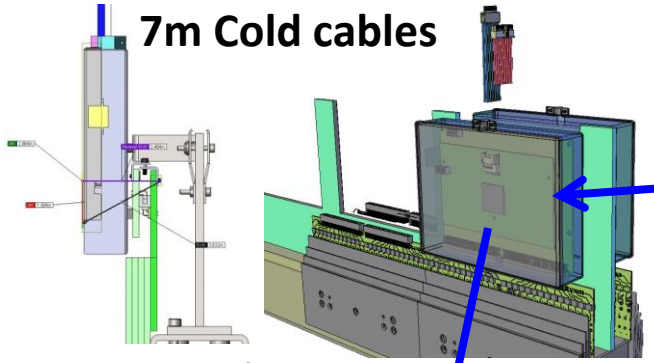
8 x

R&D produced key components to form a complete cold front-end readout chain for LAr TPC experiments

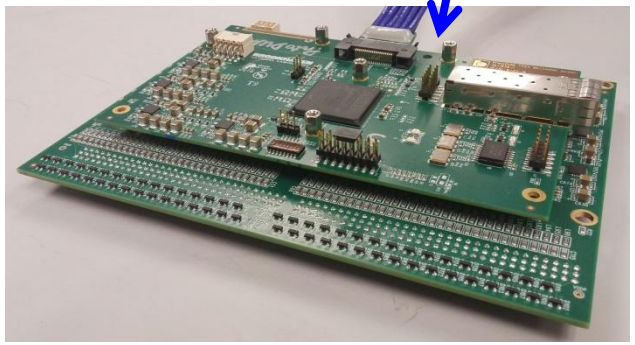


One WIEC for One APA Readout

7m Cold cables

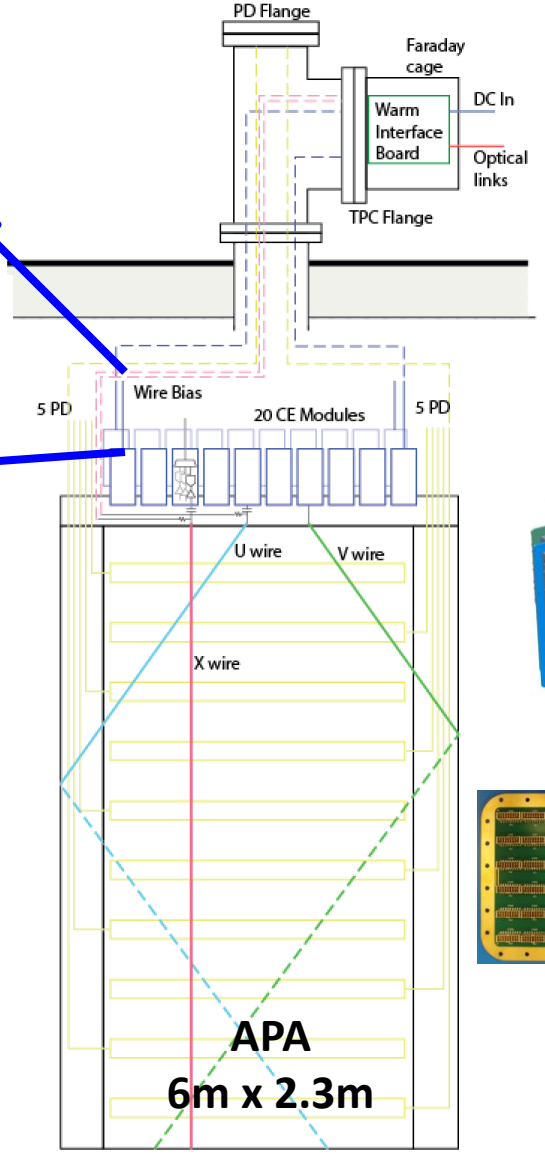


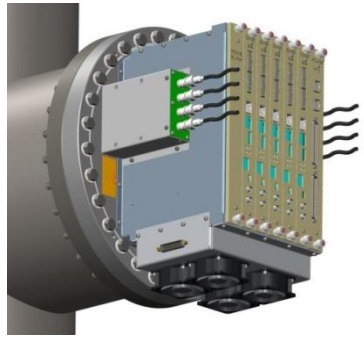
20 CE boxes on APA



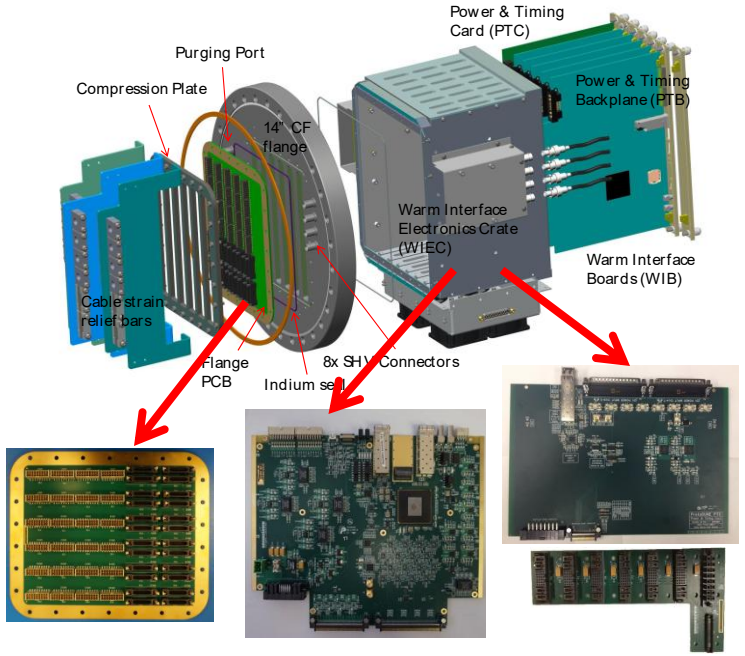
FEMB (inside CE box)

Cold Side





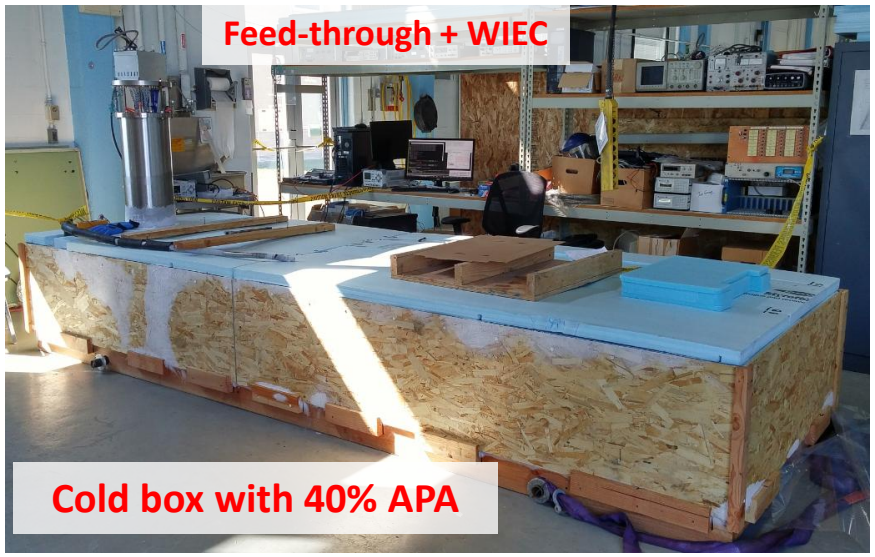
Signal Feed-through Assembly



Flange Board, WIB, PTC, PTB

Warm Side

Integration Test Stands at BNL and CERN

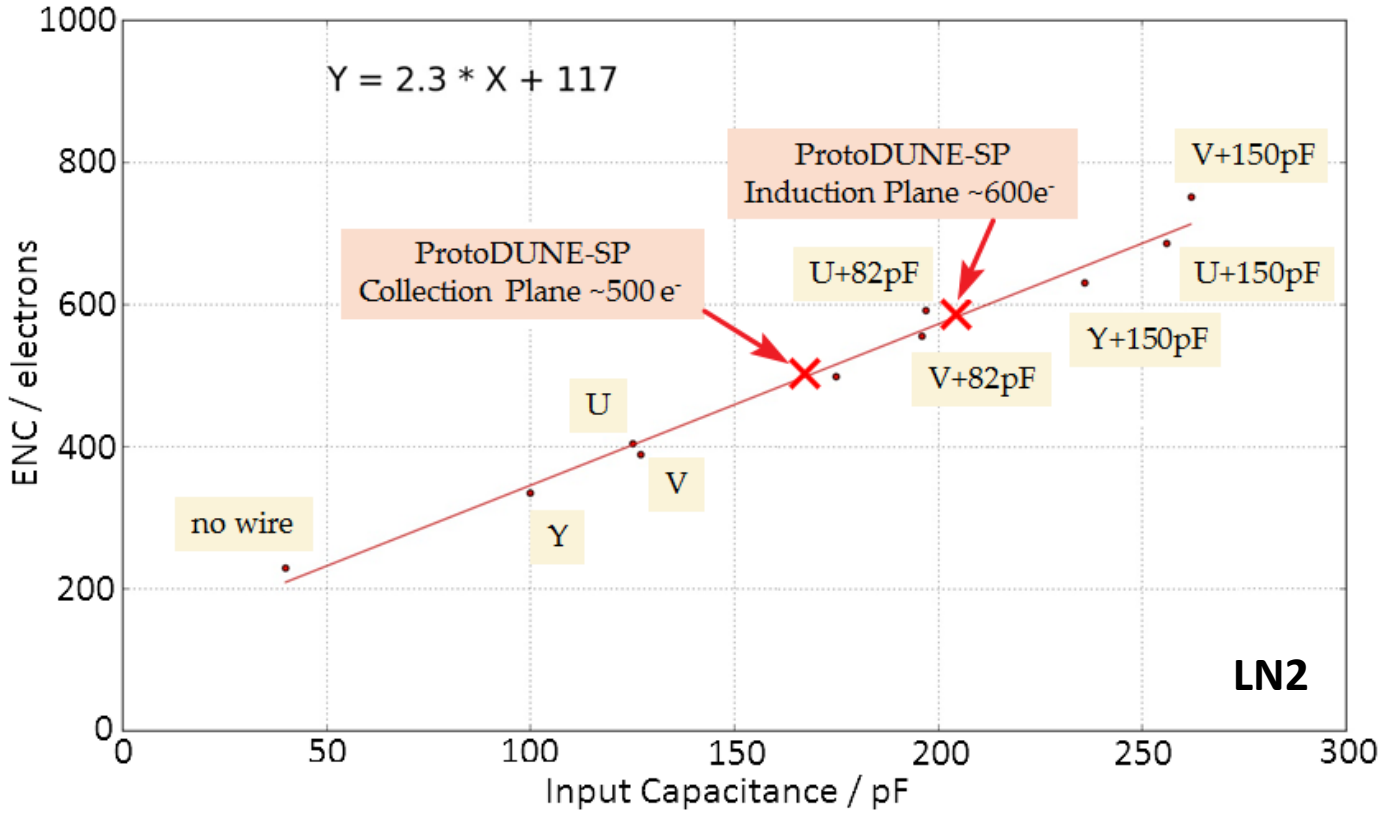


40% APA: 2.8m x 1.0m, 1024 wires

- Warm test
- Cooling down
- Cold test (~150 K)
- Warming up
- Warm test

DUNE APA: 6m x 2.3m, 2560 wires

ENC Projection Based on 40% APA



- **40% APA**
  - **U/V wire: 4.0 m**
  - **Y wire: 2.8m**

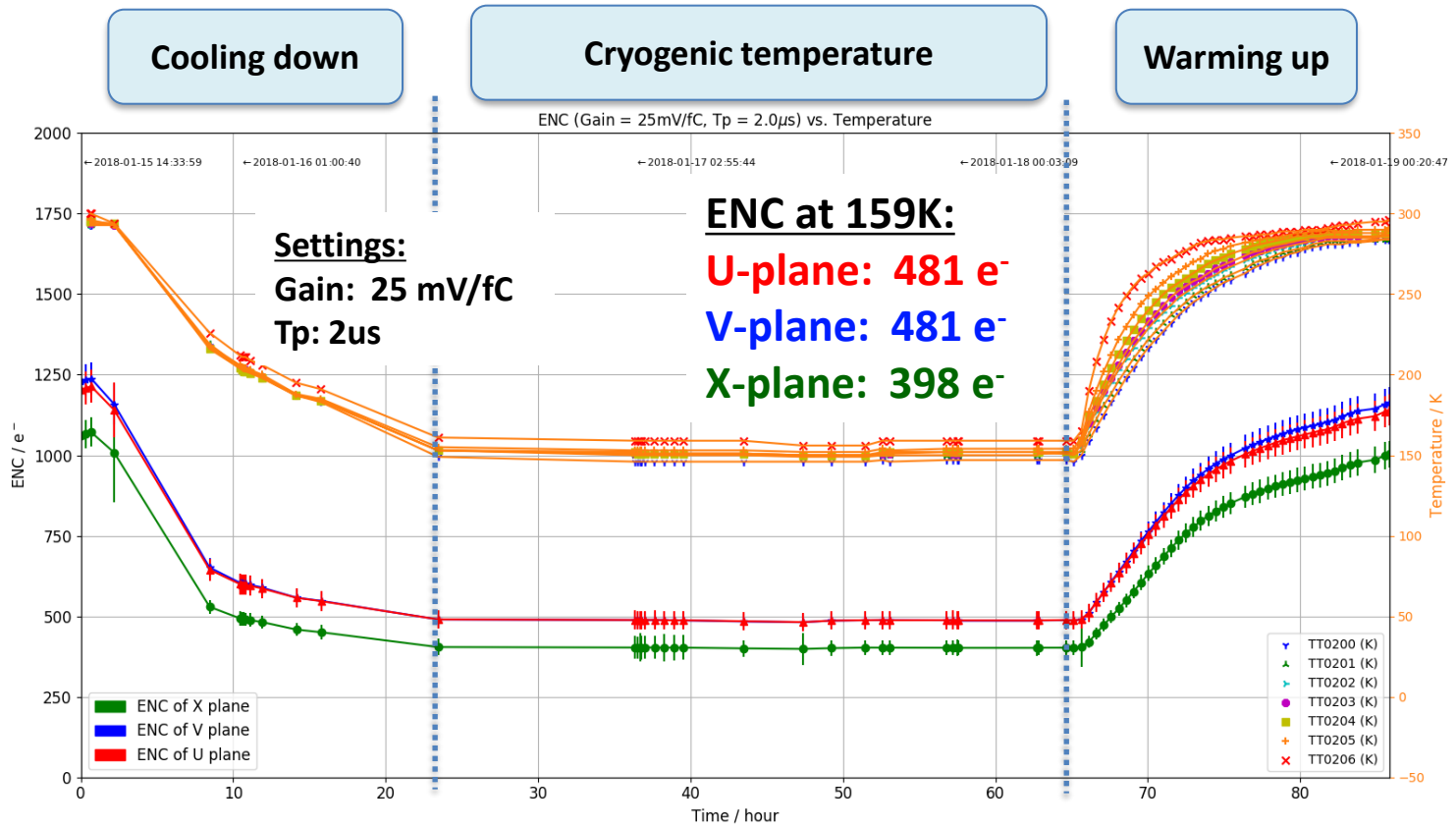
Note: 82pF and 150pF mica capacitors are added on some wires

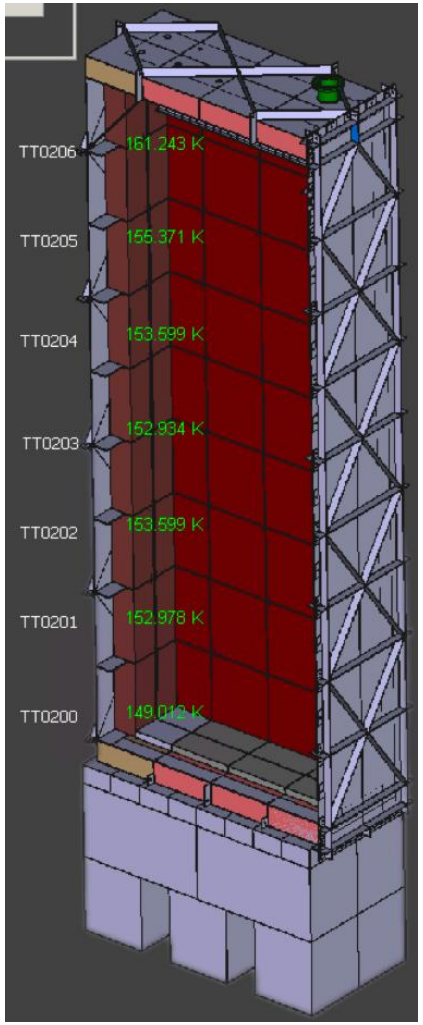
- ProtoDUNE APA
  - U/V wire: 7.39m
  - Y wire: 6.0m

- **DUNE Far Detector**
  - Same APA as ProtoDUNE-SP
  - Threshold: 1,000 e-
  - Goal: as low as possible

CERN Cold Box Integration Test

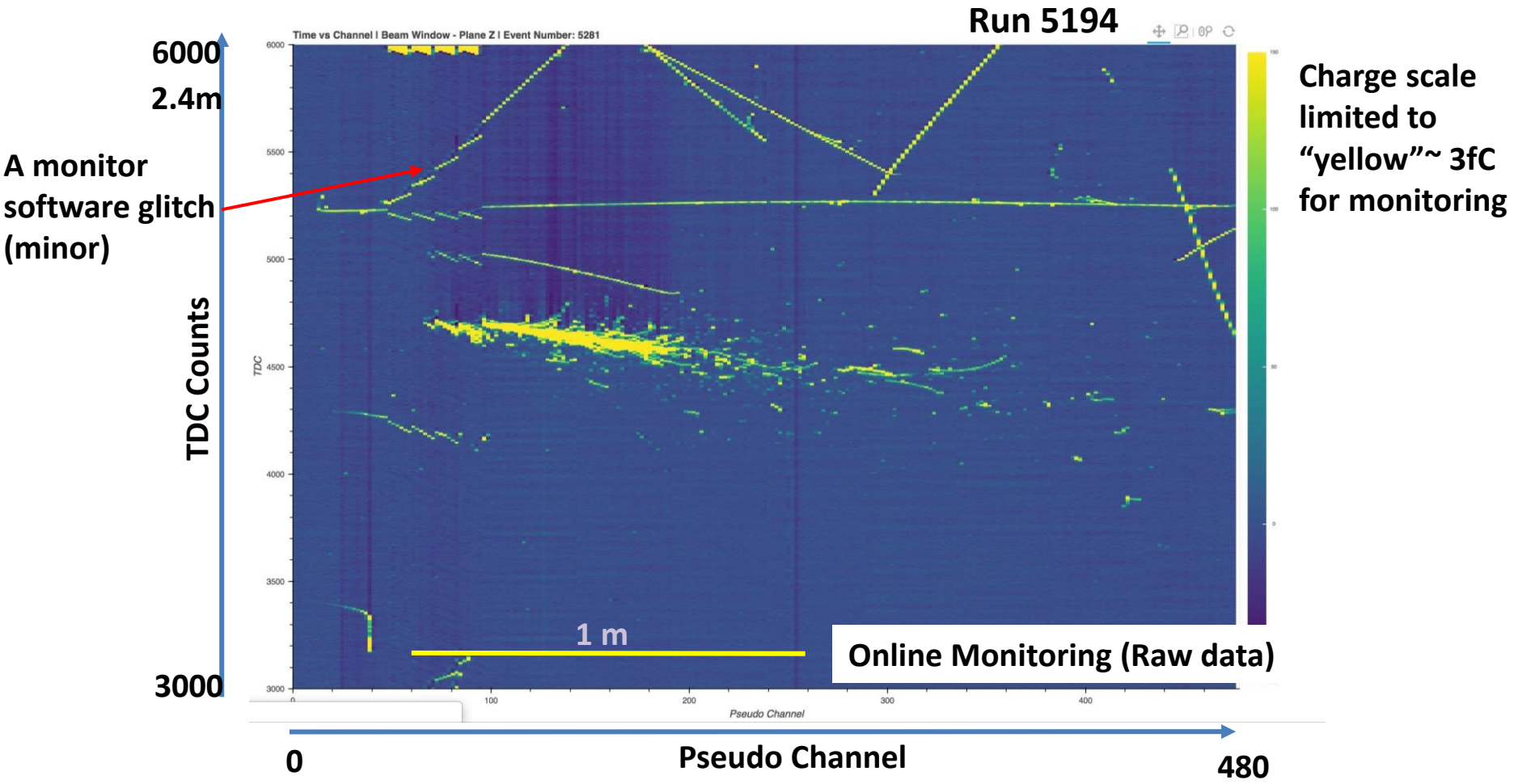
APA2 (2018-01) Cold nitrogen gas with lowest temperature reached ~ 159K





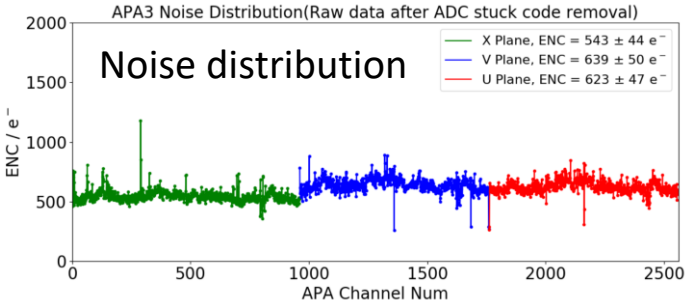
1. Uniform gain (77 e-/bin) is applied for calculating noise of all channels
2. HV Bias voltages were off
3. Data are read out chip by chip over local diagnostic GbE port.

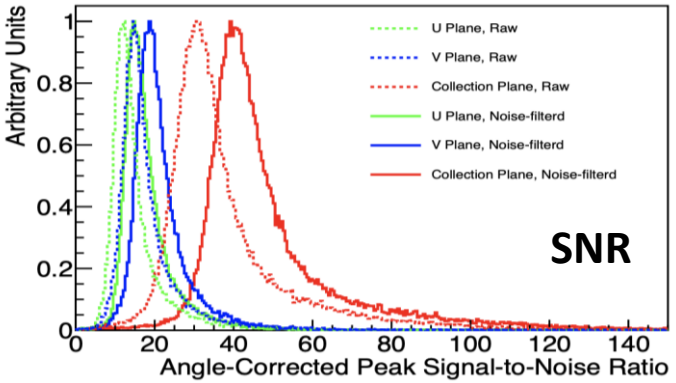
Shower Event under 7GeV Beam

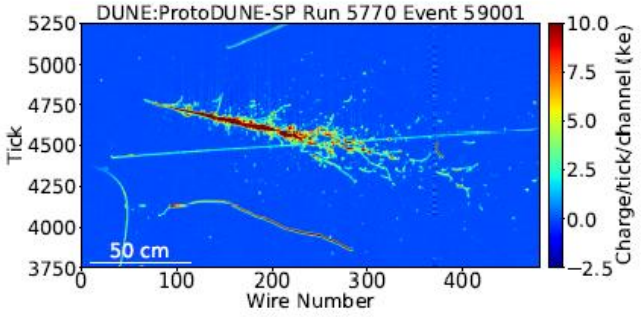


Excellent Performance of the ProtoDUNE-SP

- **High yield**
  - **99.74% (15320 of 15360) of TPC channels are active**
    - **Only 4 inactive cold electronics channels when commissioning started**
    - **2 more inactive cold electronics after >1 year running**
- **Low noise**
  - **92.83% TPC channels are good with excellent noise performance**
    - **Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-**
- **Good stability**
  - **No measurable degradation is observed over a year**
- **CE is demonstrated as the promising technology towards DUNE LArTPC**

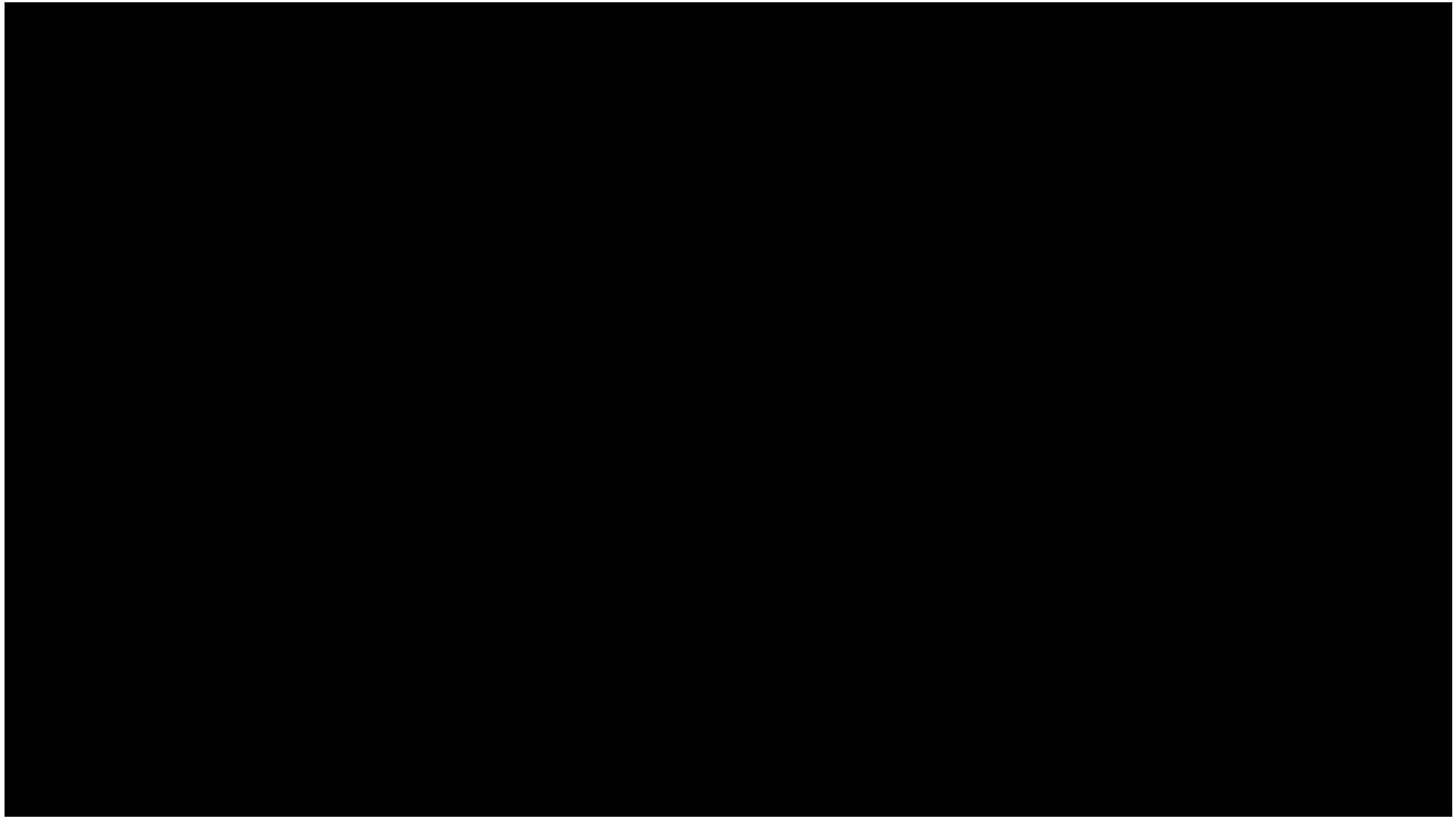






A 6 GeV/c electron candidate

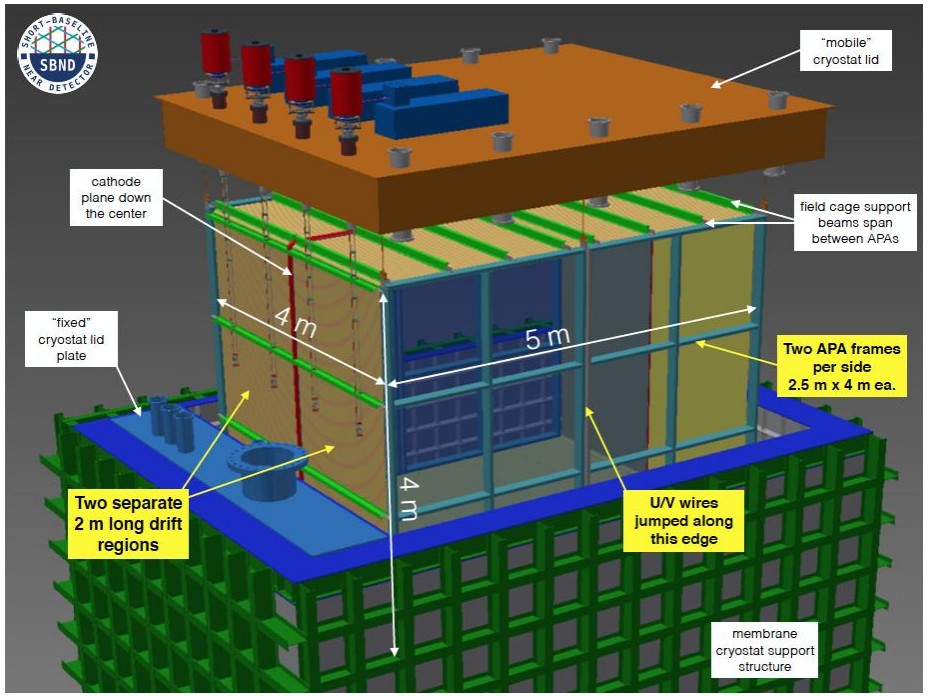
NP04 (ProtoDUNE-SP) CERN Beam Test



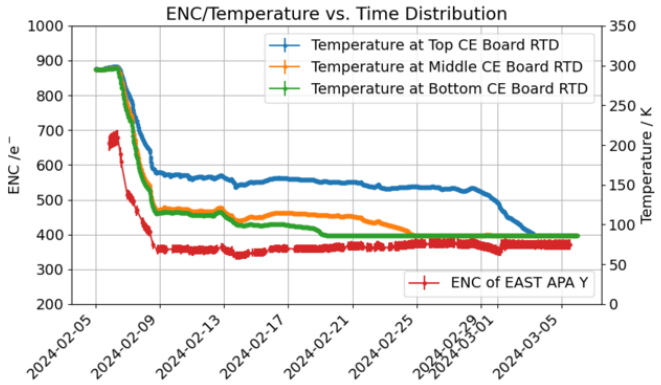
SBND Highlight

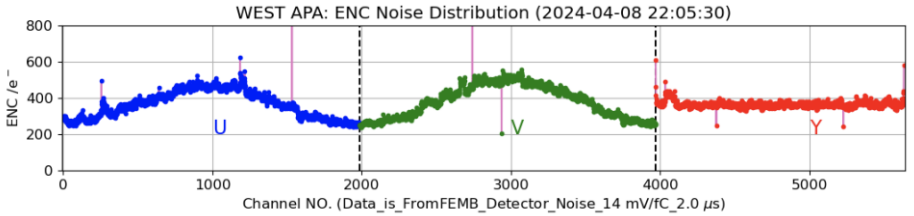
- BNL delivered the cryogenic electronics for TPC charge read out

SBND in a cryostat holding 260-ton LAr and consists of four 2.5 m (L) × 4 m (W) Anode Plane Assembles (APAs) plus 2 Cathode Plane Assemblies (CPAs), which has 2 × 2m drift regions and 11, 264 TPC (Time Projection Chamber) readout channels

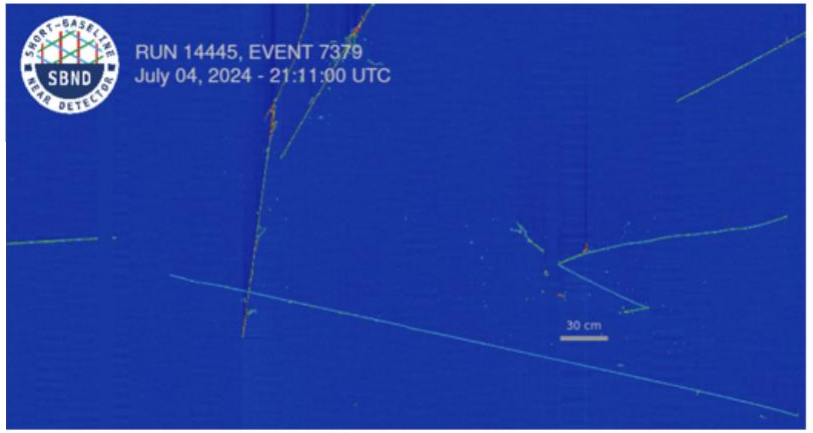


The Short-Baseline Near Detector (SBND) reached full voltage on the Time Projection Chamber Wednesday, July 3. The detector has been operating stably since then and will collect neutrino data through the end of this year's accelerator run

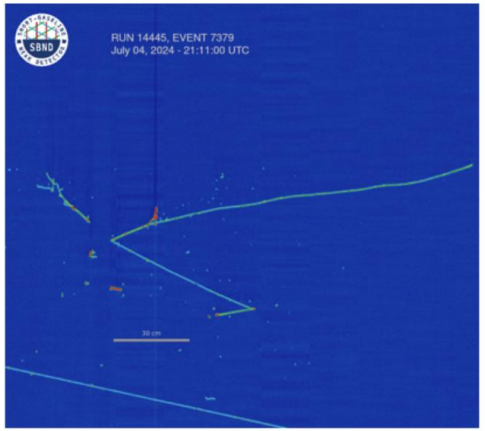




First SBND neutrino events

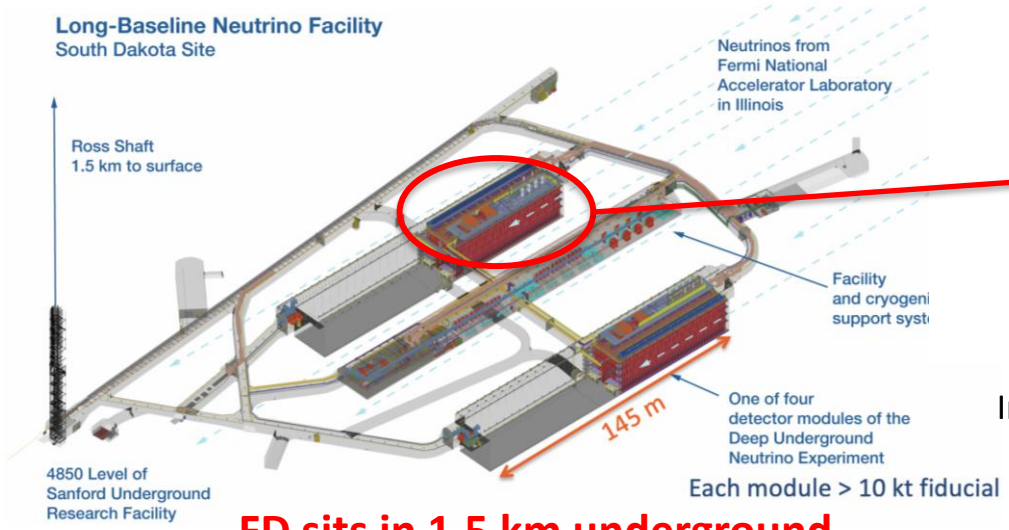


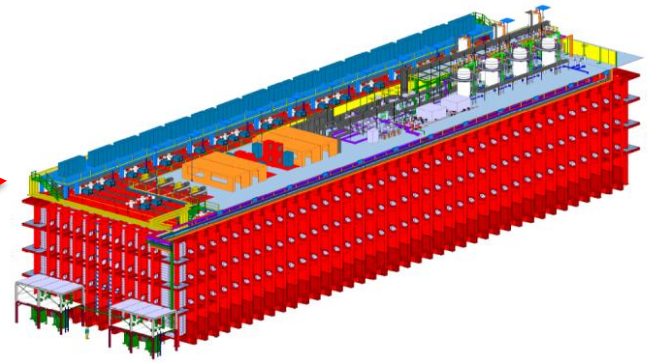
Full image



Zoomed in image

Single-Phase LArTPC for the First DUNE Far Detector Module





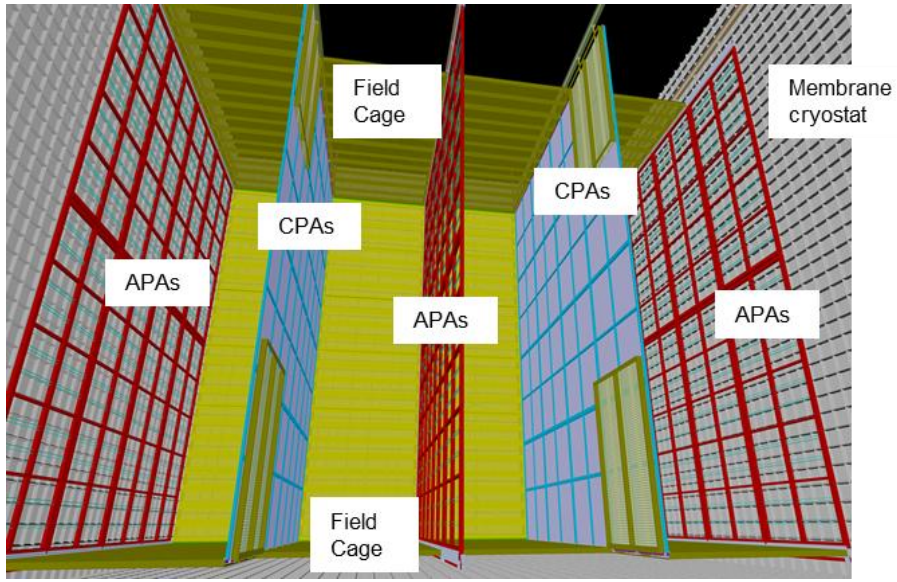
Outer:
65.8 m (L)
18.9 m (W)
17.8 m (H)

Inner active volume: 14.0 m (W) × 12.0 m (H) × 58.2 m (L)

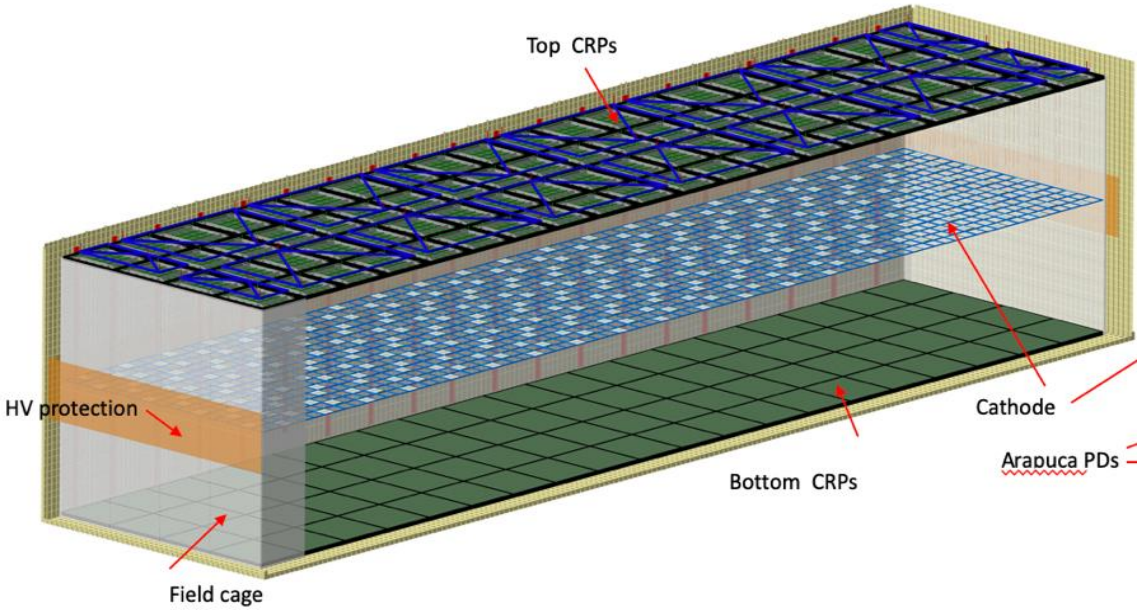
FD sits in 1.5 km underground

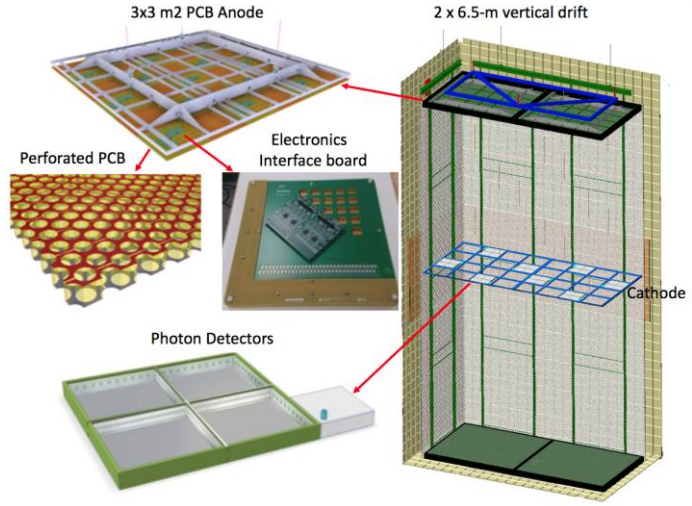
DUNE 10 kt Far Detector LArTPC CE

150 APA units
384,000 channels
24,000 FE ASICs/24,000 ADC ASICs
6,000 COLDATA ASICs
3,000 Front End Mother Board assemblies
Aim for 30 years operation without replacement and maintenance



Vertical-Drift (VD) LArTPC for the 2nd Far detector

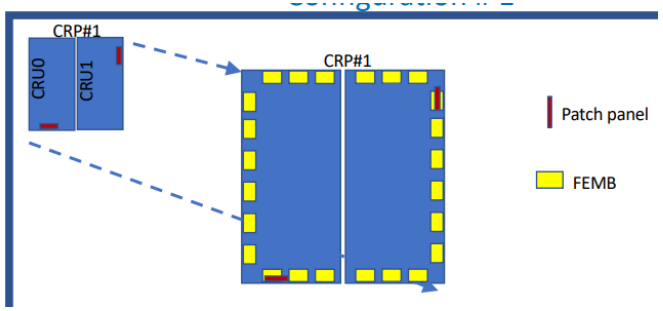




Builds on experience gained with Dual Phase detector and long e-lifetime achieved in ProtoDUNE

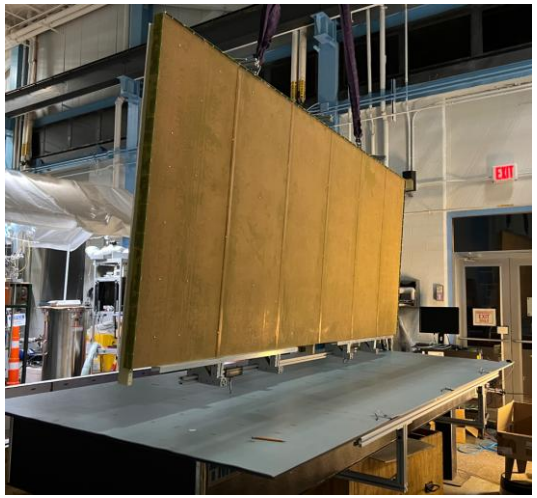
- Bottom Cold Electronics
  - CE requirements are similar between HD and VD
    - Share the same or minor-modified FEMB design
  - 80 CRPs to be readout
    - 24 FEMB per CRP (charge-readout unit)
- ProtoDUNE-VD
  - 2 CRP readout by CE (48 FEMBs in need)

PCB-based charge readout

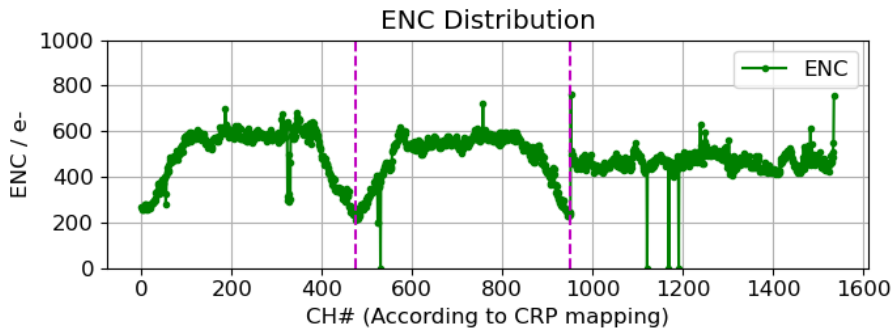


CRP5A Integration Test at BNL

- CRP5A: 3.0m x 1.5m, 1536 readout channels (12 FEMBs)



Promising noise performance at LN2



HV BIAS on, 900mV baseline, 14mV/fC gain, 2.0us peak time

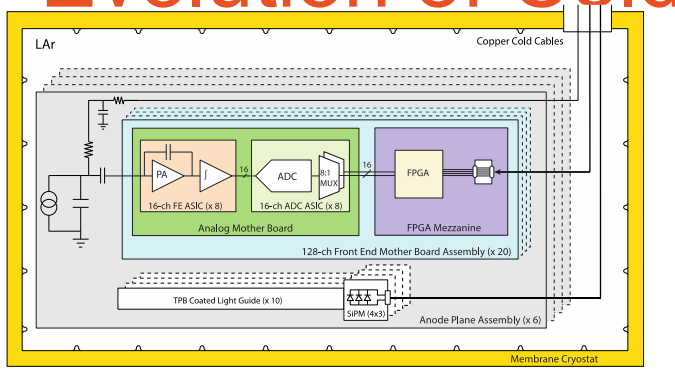
Cold Electronics in need

	FD1	FD2
anode unit	150 APA	80 CRP
Electrodes (charge readout)	384,000	245,760
LArASIC	24,000	15,360
ColdADC	24,000	15,360
COLDATA	6,000	3,840
FEMB Assembly *	3,000	1,920
Cold cable bundles	150	80
Feed-through	75	40
CE flanges	150	80
WIEC crate	150	80
WIB	750	480
PTC	150	80
PTB	150	80

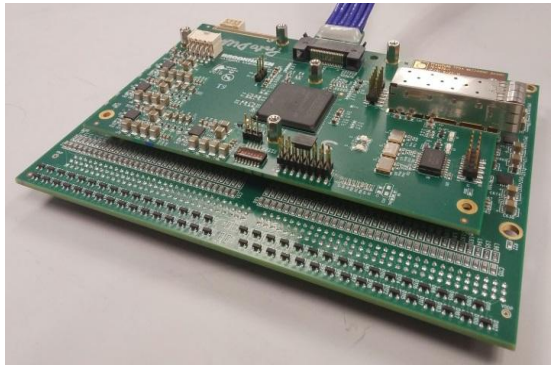
*: require at least 10% spares

DUNE Production has started after LArASIC PRR in March 2022

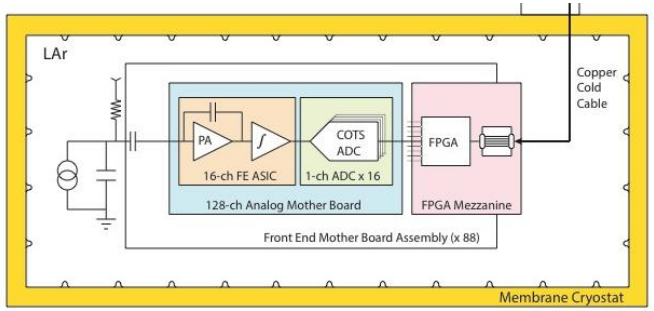
Evolution of Cold Electronics towards DUNE



ProtoDUNE (Cold FPGA)

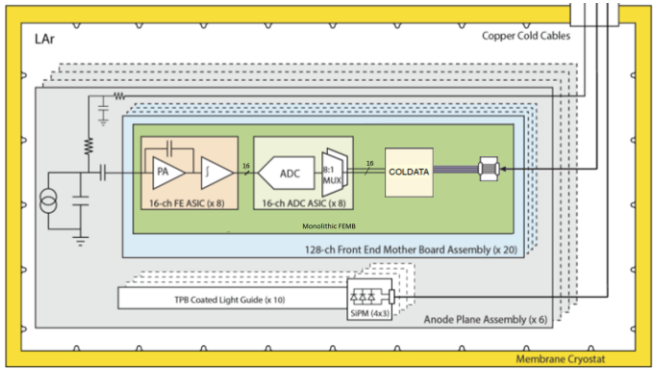


ProtoDUNE-SP FEMB with Cold FPGA successfully verified the feasibility of digitized readout at 7-89 K

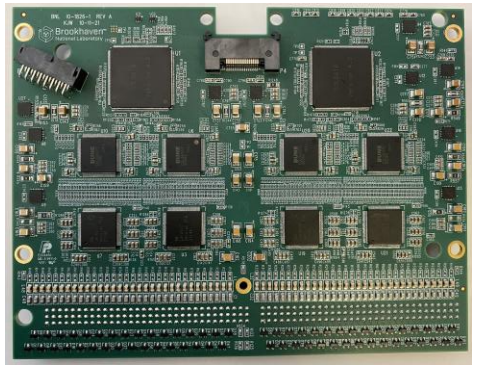


SBND (Cold FPGA + COTS ADC)

SBND FEMB with Cold FPGA and COTS ADC proves high-resolution readout can be achieved at 77-89 K



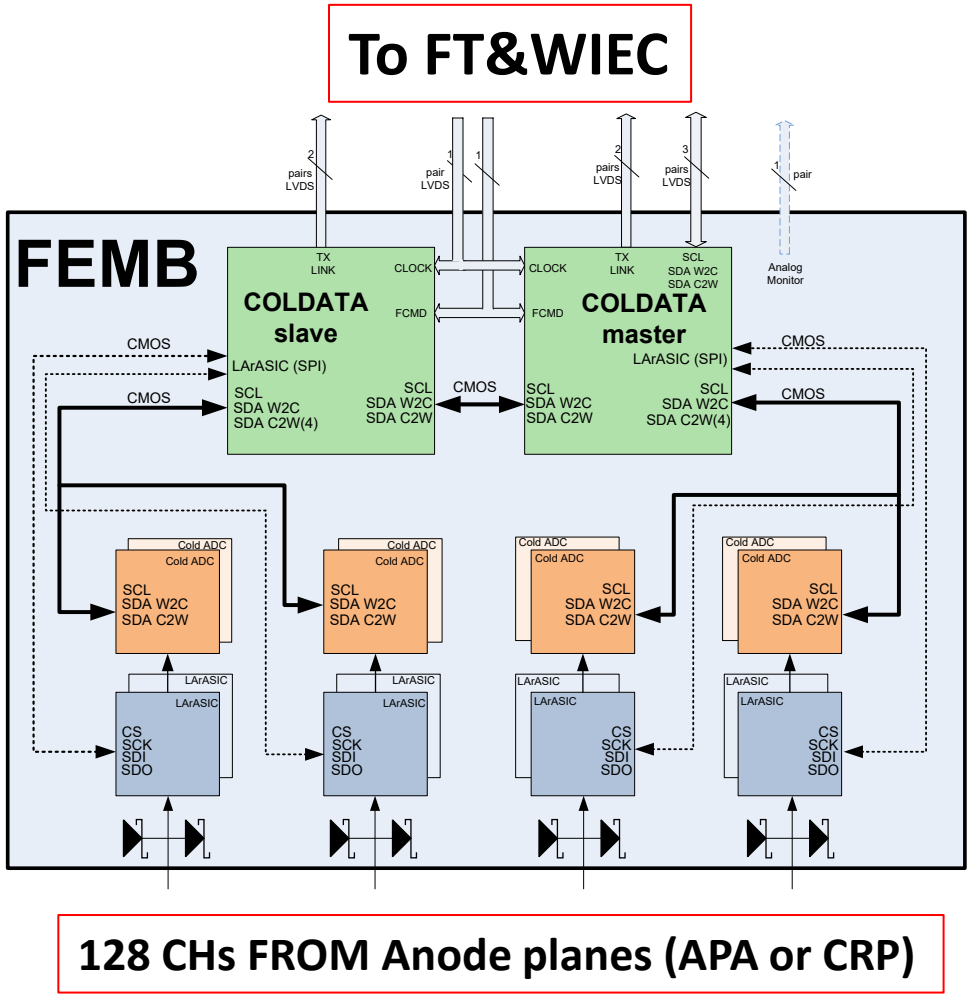
DUNE (3 Cryogenic ASICs)



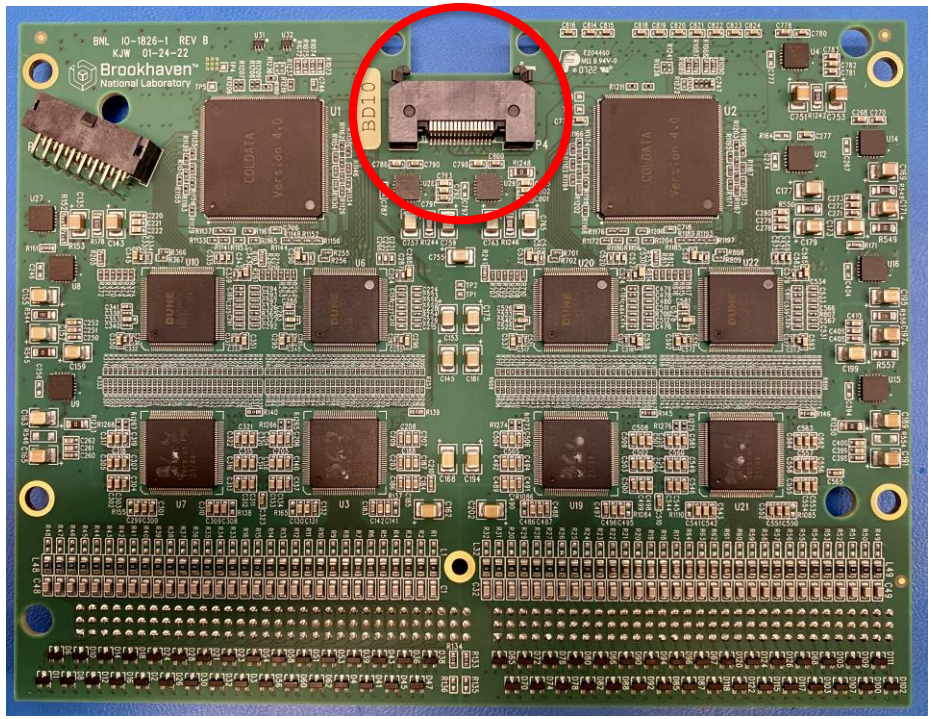
FEMB with **three** cryogenic-qualified ASICs (LArASIC, ColdADC, COLDATA) well addresses the long lifetime (30 years) and reliability requirements of DUNE far detector.

The Monolithic FEMB with 3-ASIC

- **Perform digitized readout of 128 TPC electrodes in liquid Argon**
  - 8x LArASIC (P5B)
    - 16-ch programmable charge amplifier
    - Enhanced ESD protection
  - 8x ColdADC (P2)
    - 16-ch, 12-bit, 2 MS/s ADC
    - INL < 5 LSB, DNL < 0.3 LSB
  - 2x COLDATA (P4)
    - Used to be FPGA in ProtoDUNE-I
    - Serializer and controller
      - 2 x 1.25 Gb/s TX data link per chip

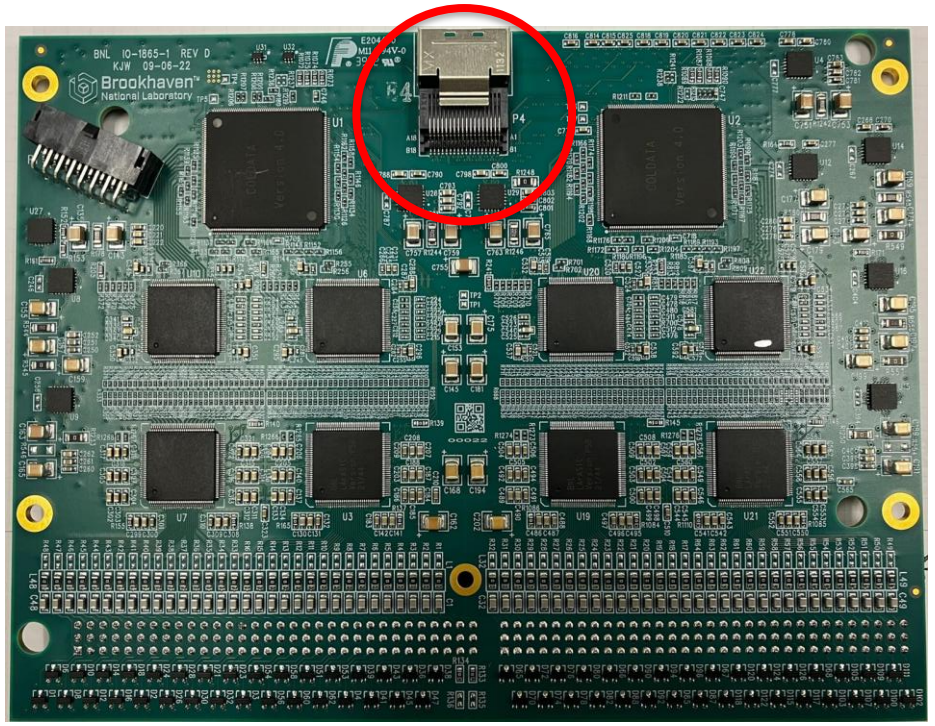


The Monolithic FEMB-HD and FEMB-VD



IO-1826-1B used in ProtoDUNE-HD

Samtec ASP-191865-03 connector



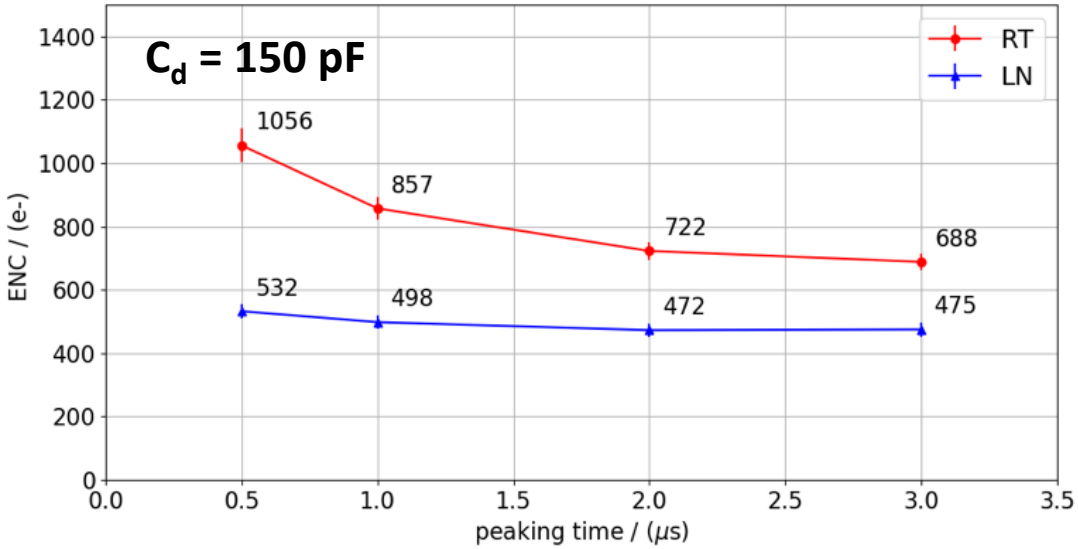
IO-1865-1D used in ProtoDUNE-VD

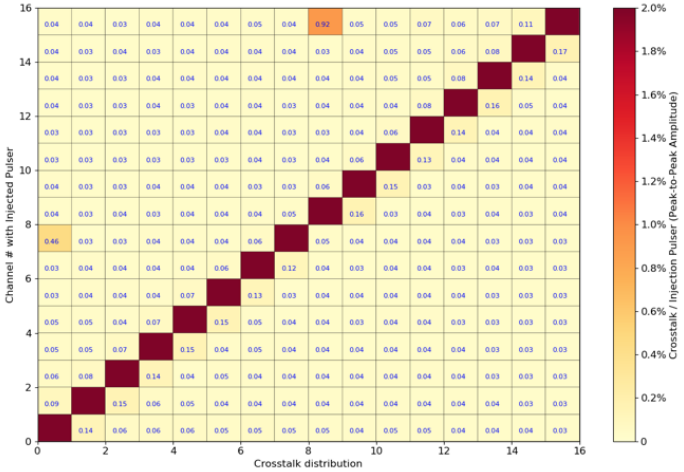
MiniSAS connector

The only difference between FEMB-HD and FEMB-VD is data cable connector!

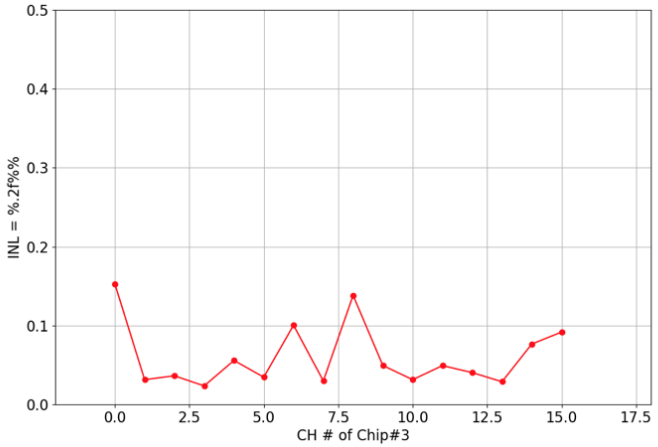
FEMB Performance

- **FEMB with P5B LArASIC, P2 ColdADC and P4 COLDATA meets DUNE requirement**



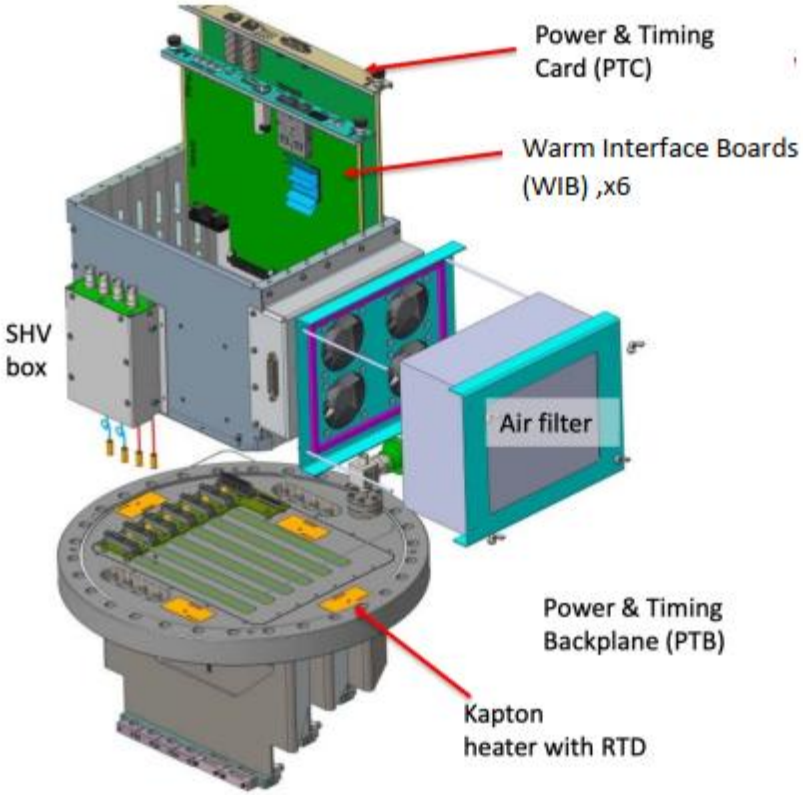


The overall crosstalk is < 0.1% at LN2 temperature for both single ended and differential interfaces, except CH0 (affected by CH7) and CH8 (affected by CH15), which are still < 1%.

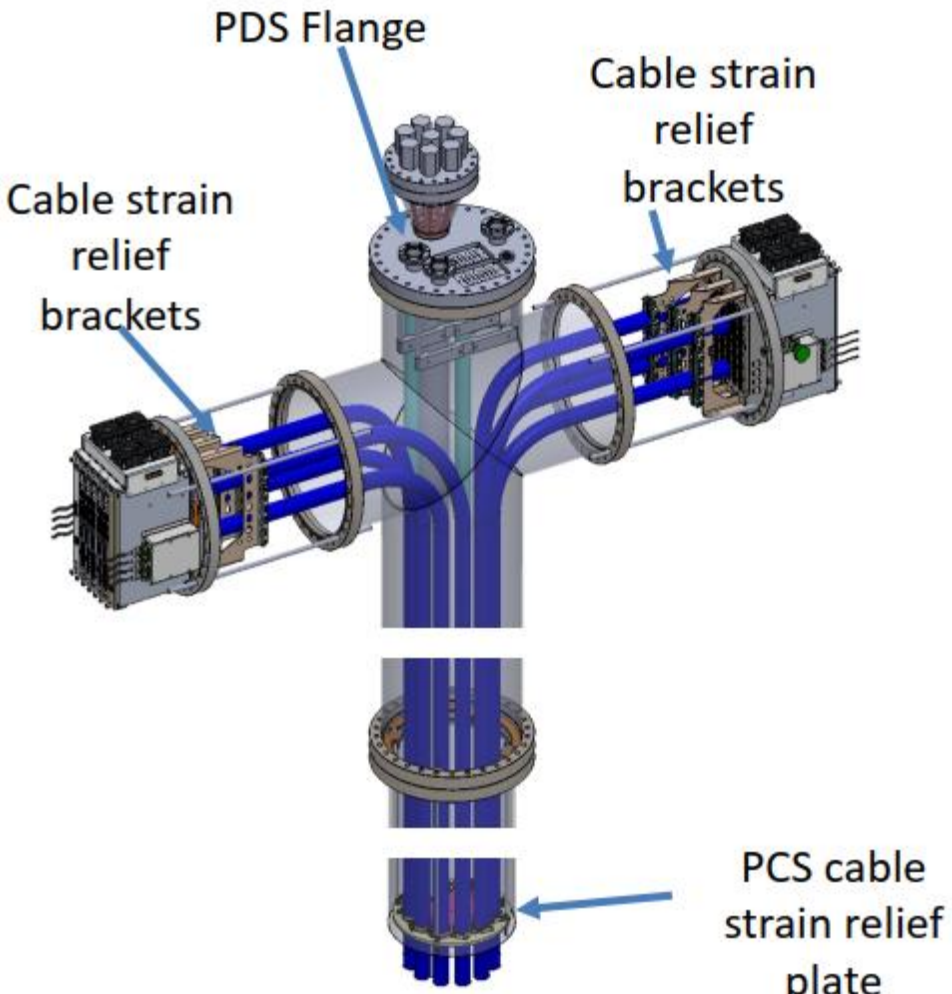


Integral non-linearity (INL) of 16 channels on the monolithic FEMB at LN2 temperature. The INL < 0.1% can be achieved for most channels up to the full dynamic range of 80 fC, except CH0 and CH8 have slightly larger non-linearity. Overall the measurements show that the INL of the monolithic FEMB is well below the DUNE requirement of 1%.

Warm Electronics and Cryostat Penetration

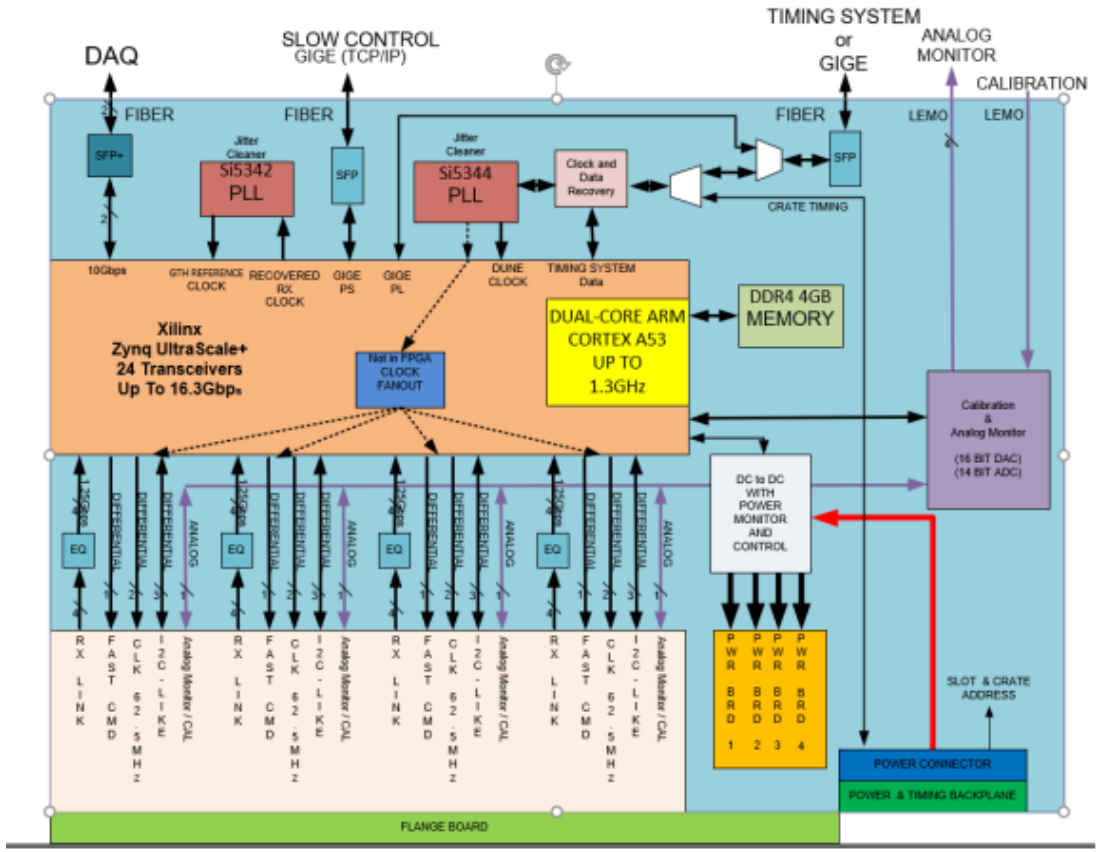


FD2: 80 Warm Interface Electronic Crates



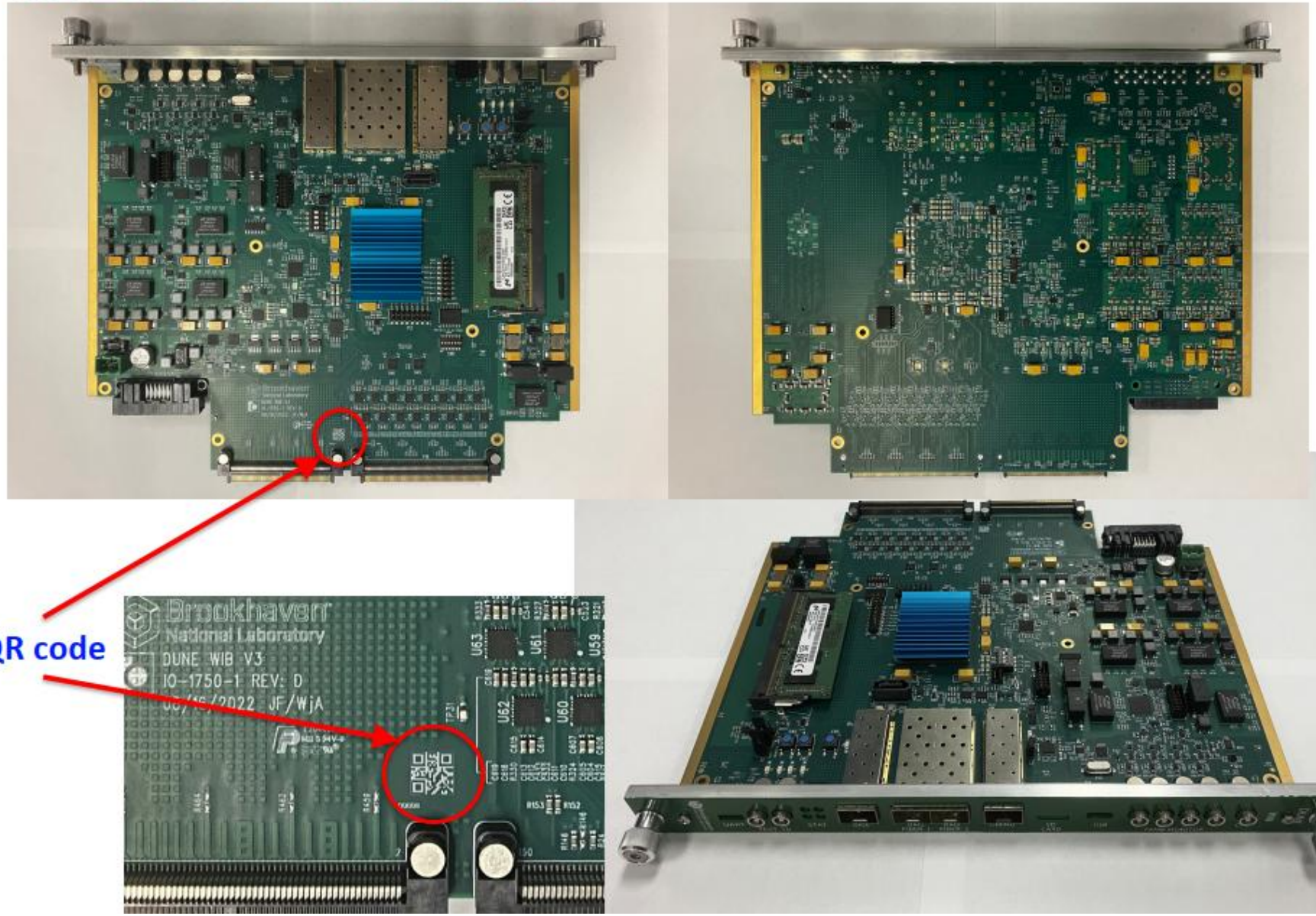
FD2: 40 penetrations

Warm Interface Board



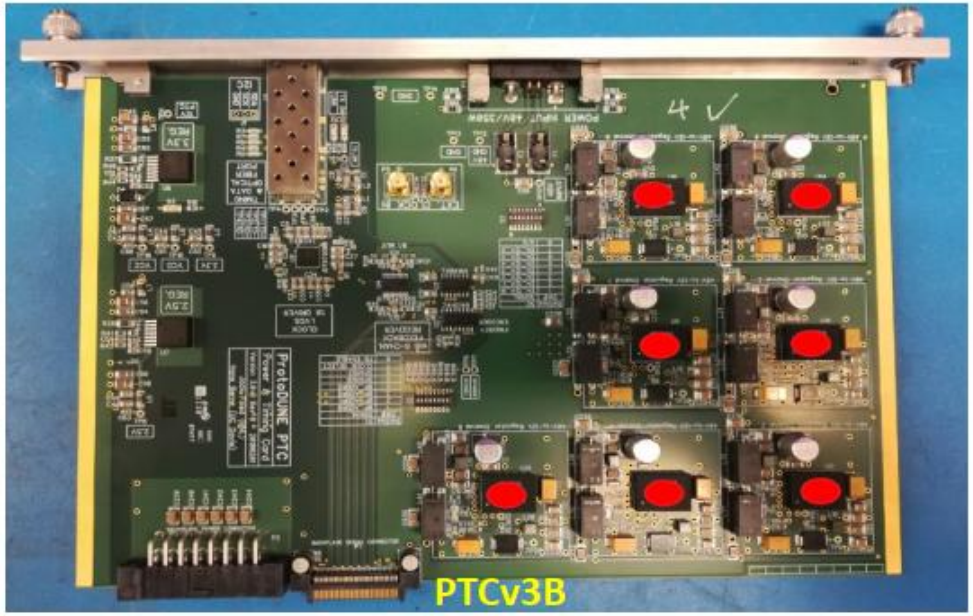
- Receive data 4 FEMBs through cold cables
- Send data to DAQ system through fiber optical links
- Receive power and timing information from PTC through PTB
- Distribute power, timing and control to 4 FEMBs through cold cables
- Slow control interface through GbE
- Monitoring and calibration interface for diagnostic

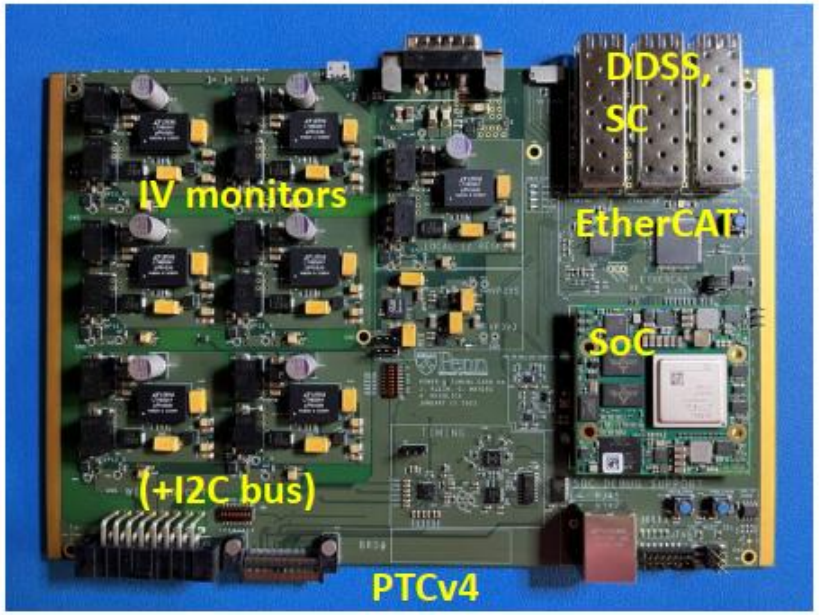
WIBv3 IO-1750-1D



PTC

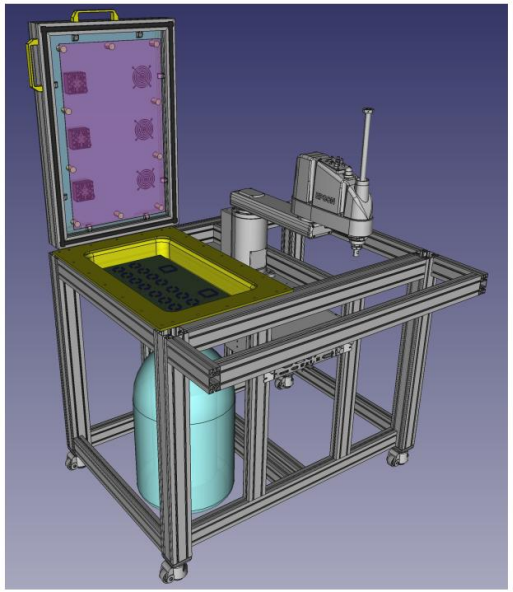
- Power and Timing Card
  - Provides Warm Interface Boards (WIBs) with 12V power on backplane (Power and Timing Backplane, or PTB)
  - Distributes DUNE timing master clock and data (62.5MHz) to WIB over PTB
  - Priority encodes WIB transmission back to timing master (one WIB at a time)





DUNE CE ASIC QC

An automatic ASIC cryogenic test stand is being developed to test over 100k chips for DUNE FD1 and FD2-BDE



The RTS comprises:

A commercial robot to pick and place the ASICs from trays to test sockets

Test chambers that support the testing hardware.

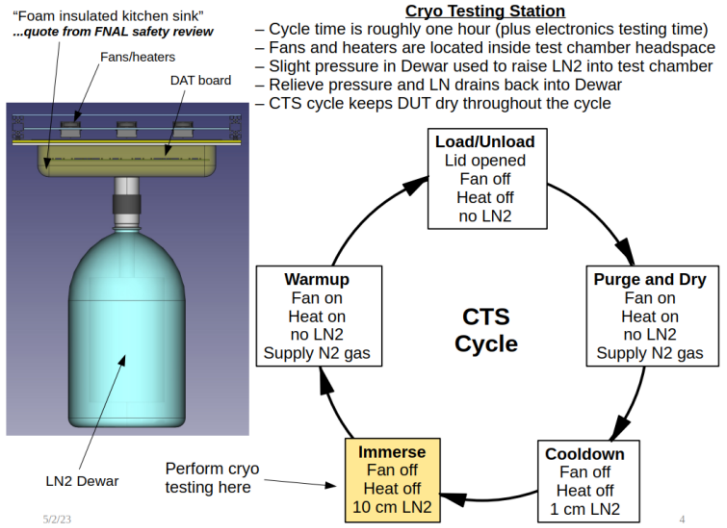
Test chambers are also Faraday enclosures.

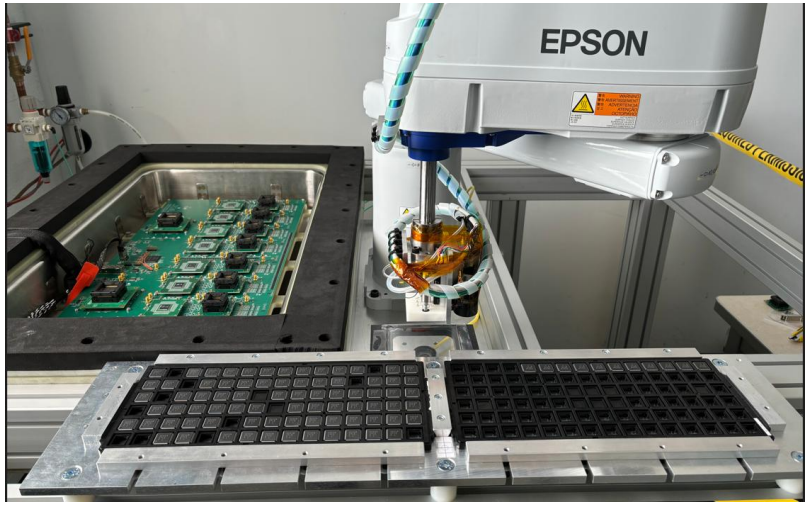
A cryogenics system that can fill and drain the test chambers.

An aluminum strut framework to hold this all together.

An upper level to the strut framework to provide a safety enclosure with access doors (not shown).

RTS system has two test chambers, only one is shown here.





Brookhaven National Laboratory DUNE


ASBESTOS
REFRIGERANT SUCTION
REFRIGERANT LIQUID
EPSON
WARNING
AVERTISSEMENT
ADVERTENCIA
ATENÇÃO

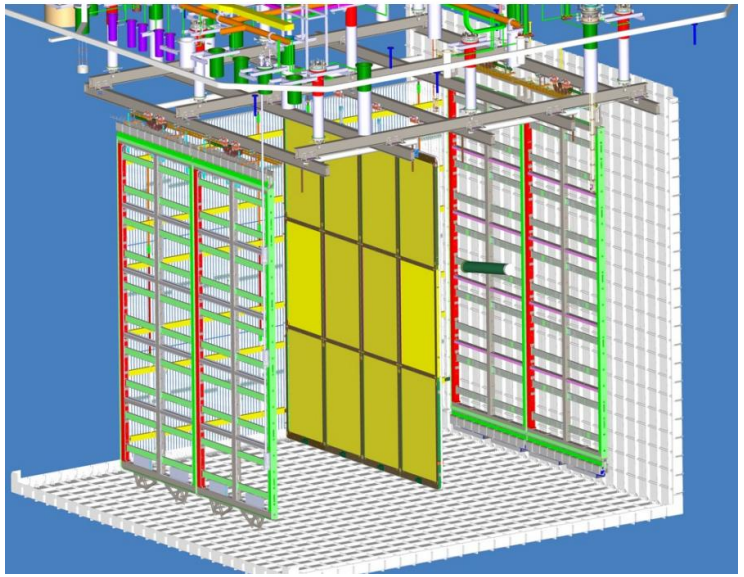
DUNE CE FEMB QC

- QC activities will be monitored and led by the **TPC electronics consortium**
  - The **same hardware setup** CTS and the same QC procedure will be distributed to all test sites.
  - FEMB QC based on CTS can perform thermal cycle testing (room temperature to liquid nitrogen) for up to 4 FEMBs simultaneously

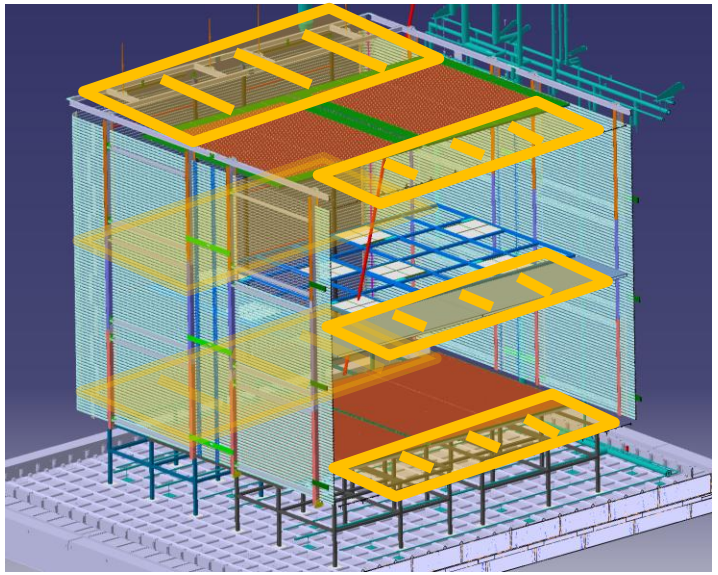
QC Test Setup Hardware

ProtoDUNE RUN-II (HD & VD)

- ProtoDUNE Horizontal Design (HD) and Vertical Design (VD)
  - Provide critical validation of technology, detector performance, and long-term stability
  - ProtoDUNE HD: 4x APA, 10,240 detector electrodes readout by cold electronics submerged in LAr
  - ProtoDUNE VD: 2x Bottom CRP, 6,144 detector electrodes readout by cold electronics submerged in LAr
- BNL focused on Cold Electronics R&D (both electrical and mechanical), production, installation and commissioning
  - ProtoDUNE HD: We delivered a full set of high-quality cold electronics to CERN. Detector installation and APA integration cold test are ongoing
  - ProtoDUNE VD: A CRP2b integration test at BNL will be performed in this month. CE production is planed.



ProtoDUNE HD



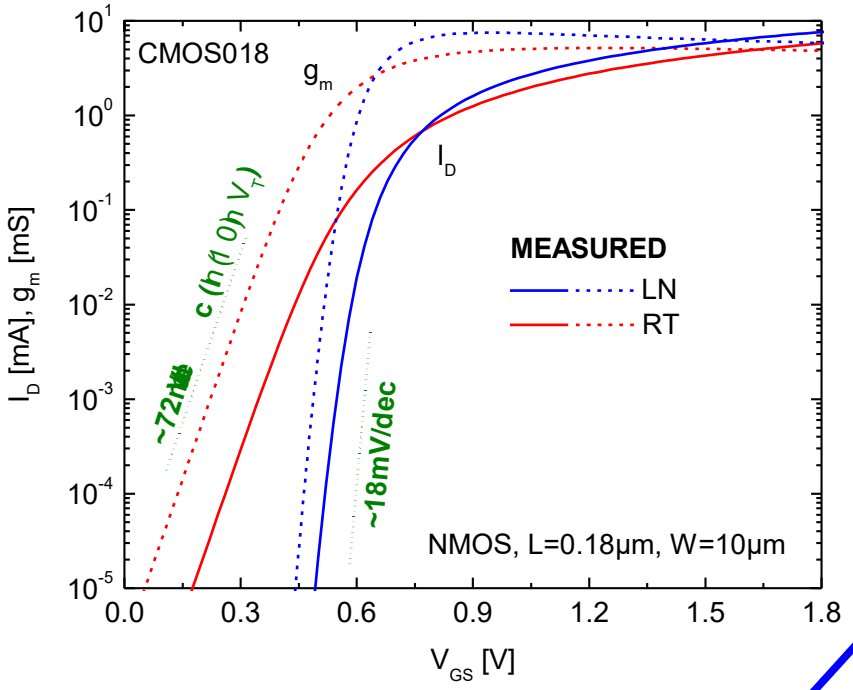
ProtoDUNE VD

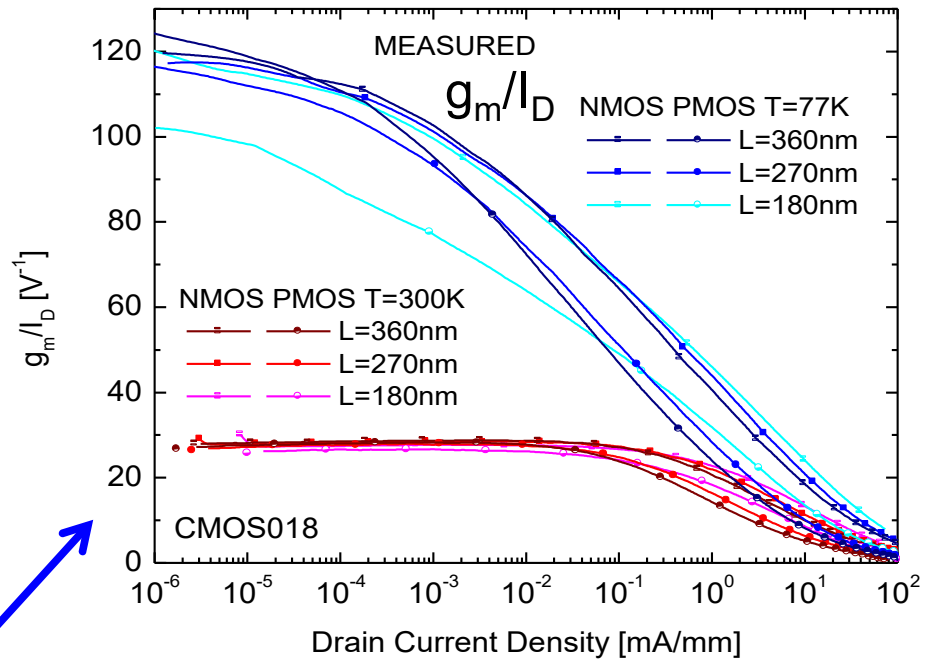
Summary

- Readout electronics developed for low temperatures (77 K – 300 K) is **an enabling technology** for noble liquid detectors for neutrino experiments
- Excellent performance of ProtoDUNE-SP
  - The integral design concept were sufficiently verified
  - High yield, low noise, good stability
  - A promising step towards DUNE-SP LArTPC
- **CE with 3 ASIC solution meets the DUNE performance needs**
  - Three cryogenic-qualified ASICs (LArASIC, ColdADC, COLDATA) for long lifetime (> 30 years) at 89K
  - ProtoDUNE-SP RUN-II in 2022 will be instrumented with final 3-ASIC FEMB
- **It is your excellent opportunity for groundbreaking discoveries**
  - DUNE experiment is expected to start in 2026, and last for 20-30 years
  - Provide the best detector to help you change our understanding of the universe
    - Origin of Matter, Unification of Forces, Black Hole Formation

backups

CMOS Characteristics in LAr



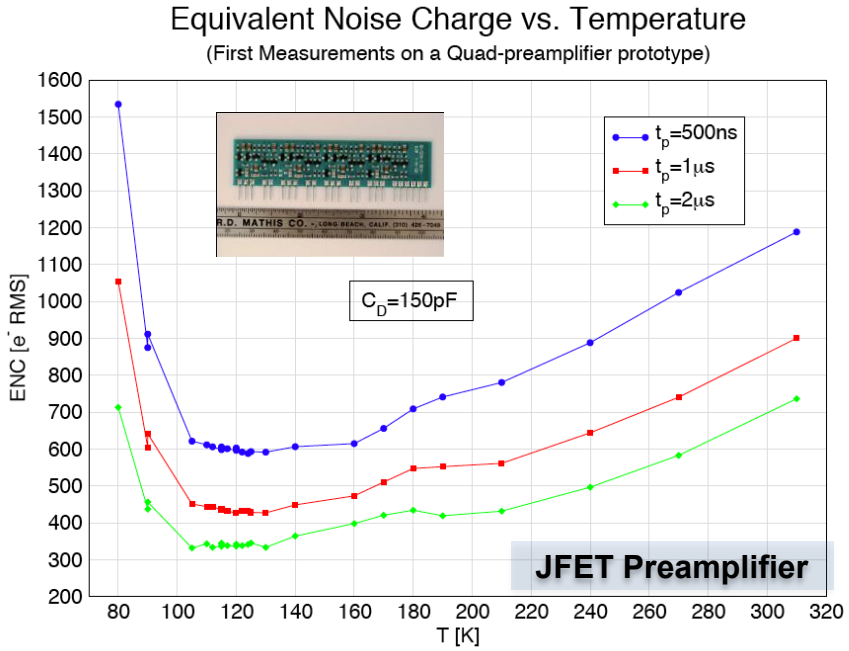


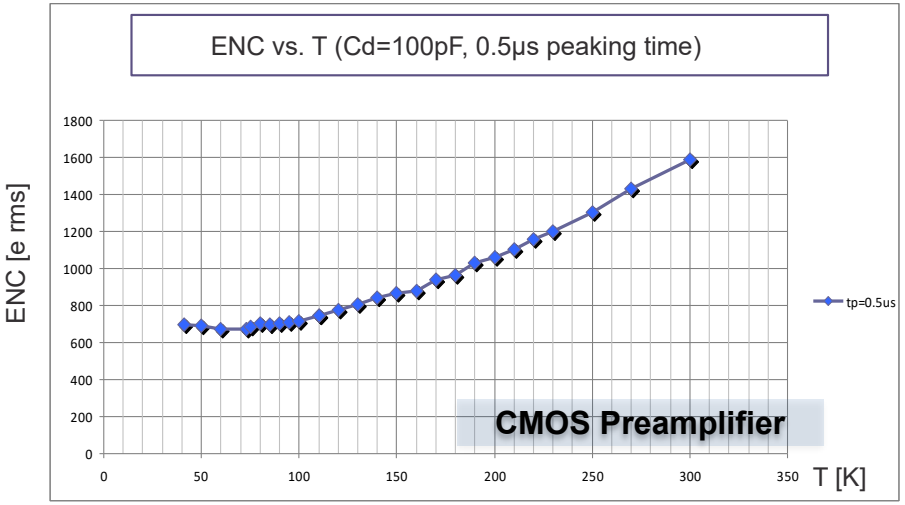
Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

From JFET to CMOS





- JFET based preamplifier designed for MicroBooNE
  - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
- CMOS technology – test result of an existing ASIC in 0.25 *µm (not designed for LAr)*
  - CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
  - R&D of CMOS cold electronics at BNL started in 2008

CMOS Reliability at Cryogenic Temperatures

- Studies of CMOS lifetime and reliability at 77 K have been conducted
  - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
- Most of the major failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature
  - Such as electro-migration, stress migration, time-dependent dielectric breakdown and negative-bias temperature instability
- The degradation (aging) due to channel Hot Carrier Effects (HCE)
  - **The only remaining mechanism** that may affect the lifetime of CMOS devices at cryogenic temperature
  - Lifetime due to HCE aging
    - A limit defined by a chosen level of monotonic degradation
      - Drain current, transconductance, threshold voltage etc.
    - The aging mechanism does **not** result in **sudden device failure**
    - The device "fails" if a chosen parameter gets out of the specified circuit design range
- The degradation mainly concerns NMOS devices
  - PMOS usually exhibits a lifetime much longer than NMOS.

FEMB Power Consumption

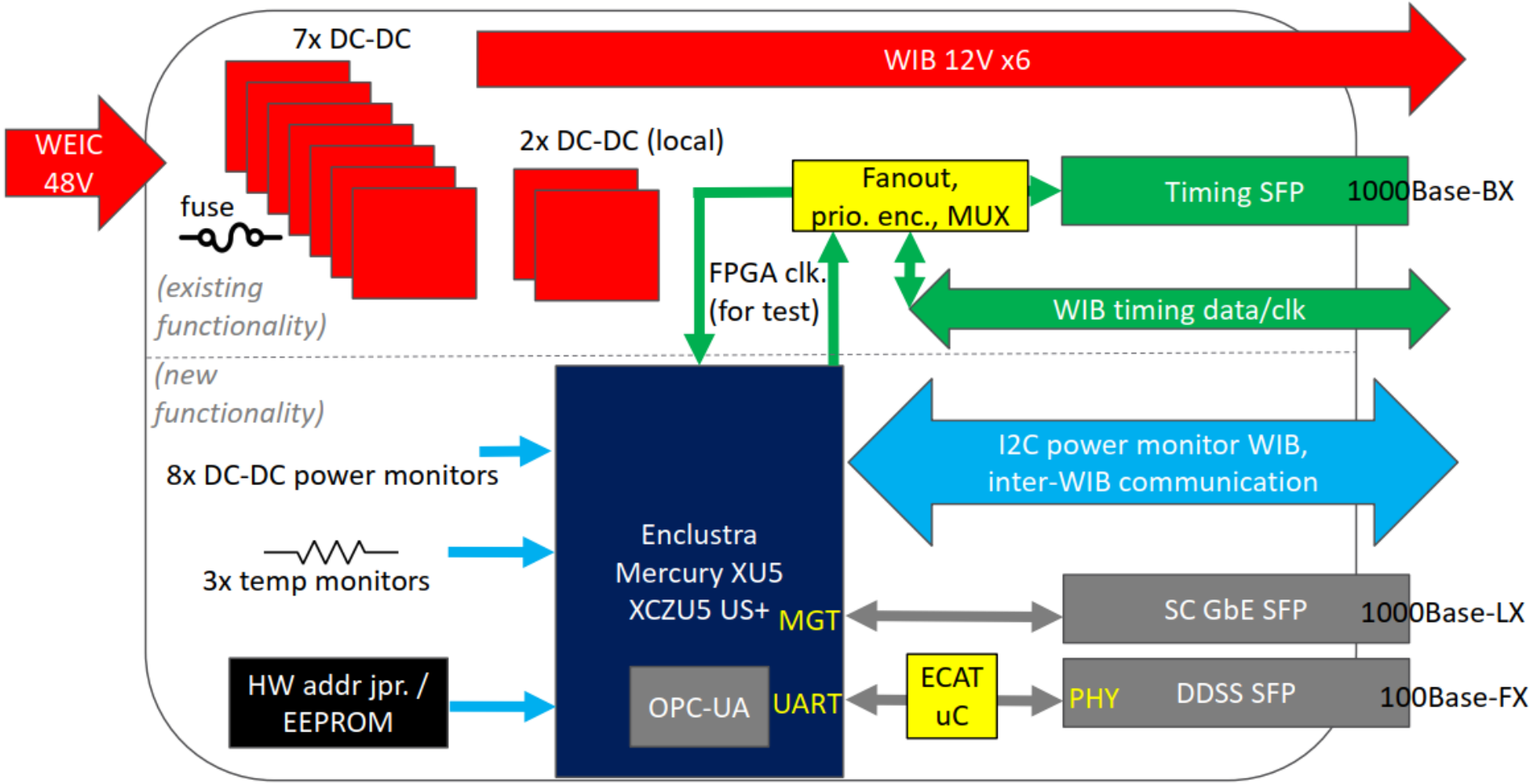
- Meet < 50 mW/ch requirement
  - The power consumptions of P5 LArASIC, P2 ColdADC and P3 COLDATA have been measured. The power consumption is ~29 mW/ch with single ended output without buffer, and ~34 mW/ch with differential output and SEDC buffer turned on. Taking into account the power consumption in voltage regulators, with ~300 mV voltage drop of voltage regulators, the total power consumption of a monolithic FEMB is less than ~45 mW/ch, or a total ~5.8 W

Env	SMU	Current at 900 mV BL (mA)			Current at 200 mV BL (mA)		
		OFF	SE ON	SEDC ON	OFF	SE ON	SEDC ON
RT	VDDP = 1.8V	31.5	31	31.5	31.5	31	31.4
	VDD = 1.8V	20	47	50.6	18.5	43	49.8
	VDDO = 1.8V	0.1	6	12.4	0.1	6	14.2
	Power per ch. (mW)	5.8	9.5	10.6	5.6	9.0	10.7
LN2	VDDP = 1.8V	31.3	31	31.3	31.3	31	31.2
	VDD = 1.8V	17.1	44	50.1	15.5	42	51.4
	VDDO = 1.8V	0.1	6	12	0.1	5	13.2
	Power per ch. (mW)	5.5	9.1	10.5	5.3	8.8	10.8

Power rail / V	RT	LN2
	CMOS Reference	CMOS Reference
	Current / mA	Current / mA
2.25V (VDDA2P5, VDDD2P5)	128.0	132.4
1.1V (VDDD1P2)	1.3	1.2
2.25V (VDDIO)	15.3	14.5
Total Power Consumption /mW	323.9	331.8
mW/CH	20.2	20.7

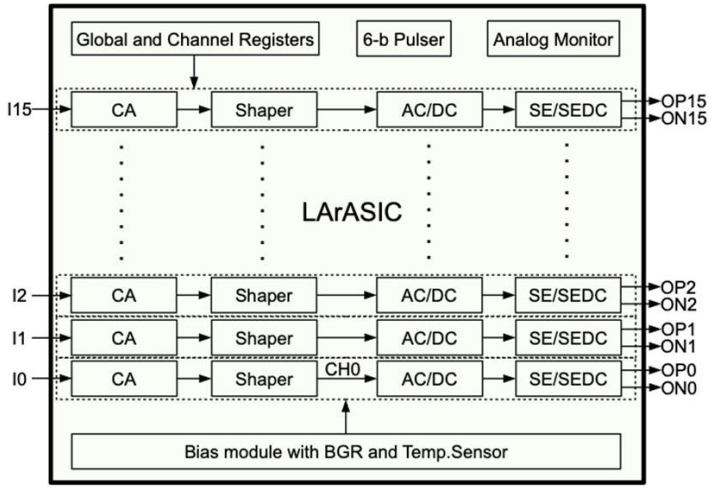
Measured at RT with the P5 FE + P2 ADC + P3 COLDATA		
Power Rails	Measured Voltage / V	Measured Current / mA for 2x COLDATA chips on board
CD_VDDIO (2.25V)	2.236	111
CD_VDDA (1.20)	1.197	19
CD_VDDD & CD_VDDC (1.1V)	1.095	64
Power Consumption per chip	171 mW	
Power Consumption per CH	2.7 mW	

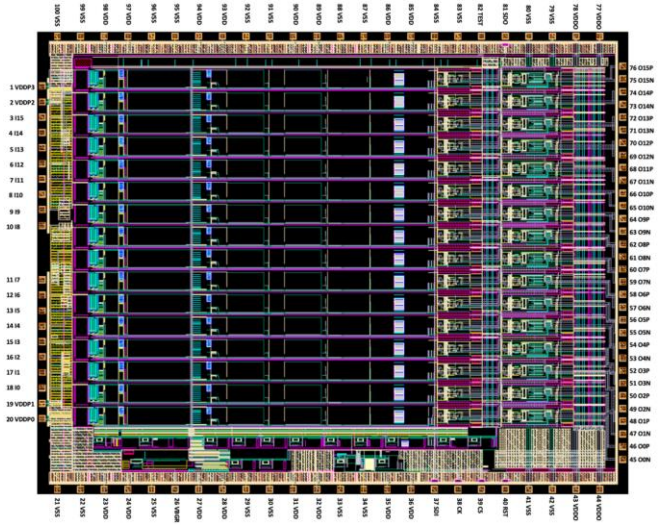
Top level PTC v4 block diagram



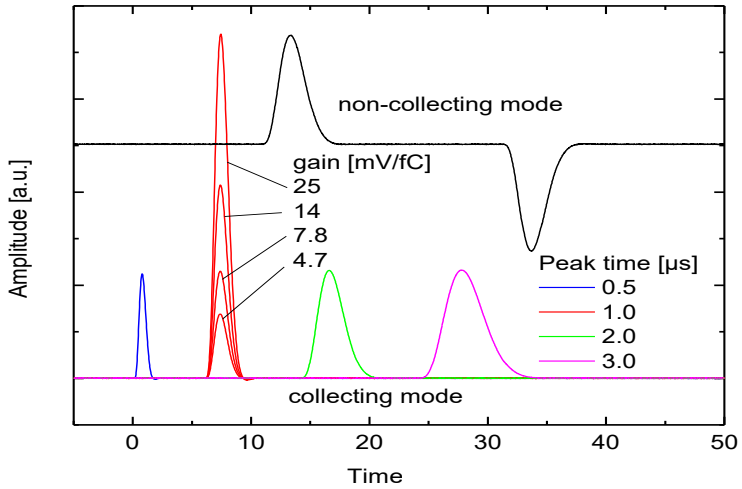
LArASIC P5B

16x ch programmable charge amplifier working at 77-300K



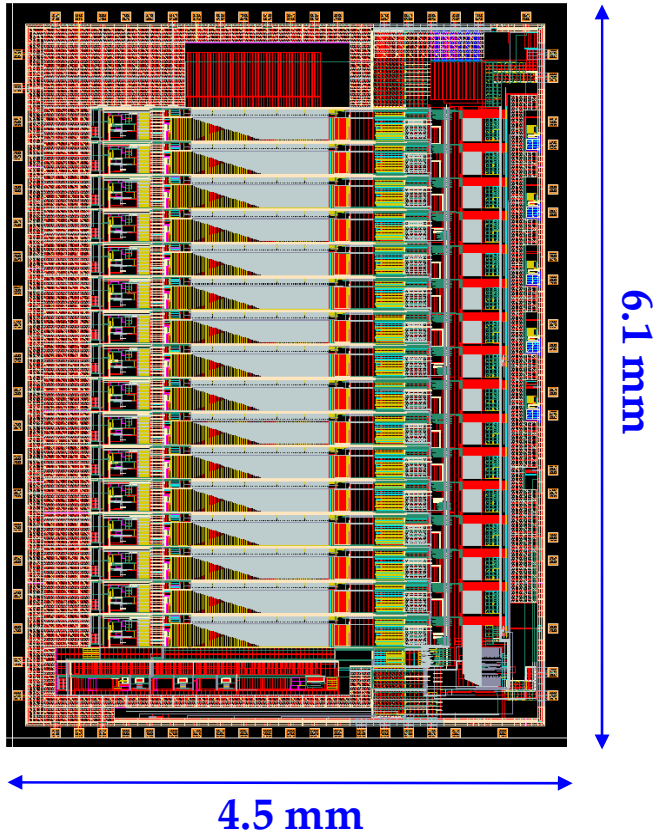


Technology	180 nm CMOS – 1-poly, 6-metal, MiM cap, sil blk resistors			
Supply Voltage	1.8 V			
Temperature Range	77 – 300 K (-196 – 27 °C) optimized for 87k (-186 °C)			
Number of Channels	16			
Max Single-Ended Output Swing	1.4 V peak to peak (0.2 – 1.6 V)			
Gain Selection (mV/fC)	4.7	7.8	14	25
Full-Scale Input Charge (fC)	300	180	100	56
Baseline selection	200 mV (collection mode)		900 mV (induction mode)	
Charge Preamplifier Polarity	Negative (collection mode)		Bipolar (induction mode)	
Adaptive-Reset Current Selection (nA)	0.1	0.5	1	5
Shaper Peaking Time Selection (µs)	0.5	1	2	3
Output Coupling	AC (100 µs HPF time-constant)		DC	
Output Selection	Shaper		SE buffer	SEDC buffer
Total Channel Settings	1024			
Integrated Test Capacitor	200 fF			
Temperature Sensor	0.8728 V @ 25°C + 2.868 mV/°C			
Integrated Pulse Generator	6-bit DAC based			
Configuration Control	SPI interface with 144 register bits			

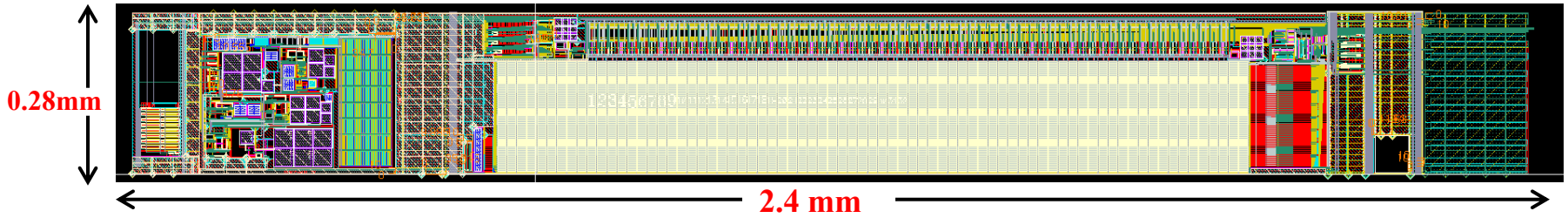


Cold ADC ASIC for ProtoDUNE-SP

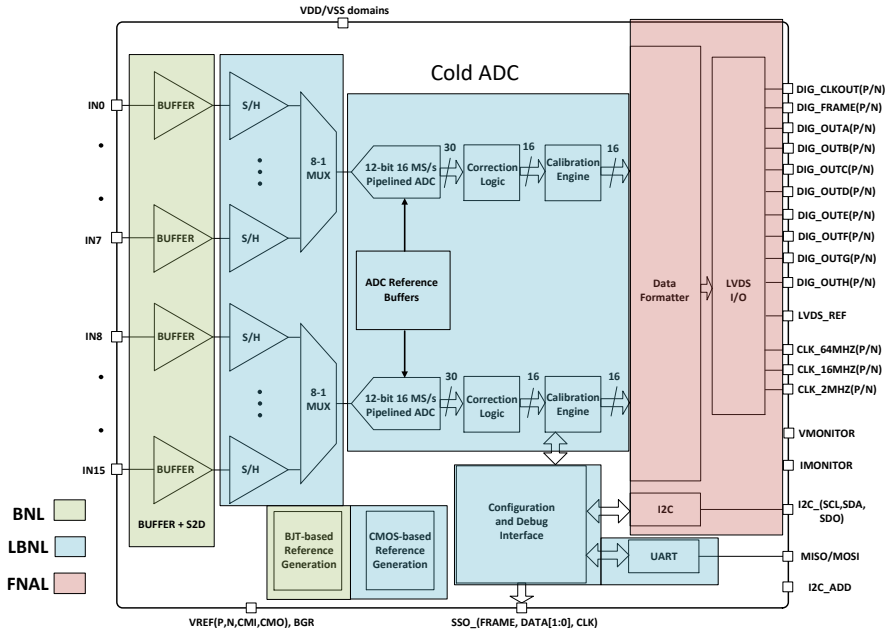
Development discontinued after ProtoDUNE-SP

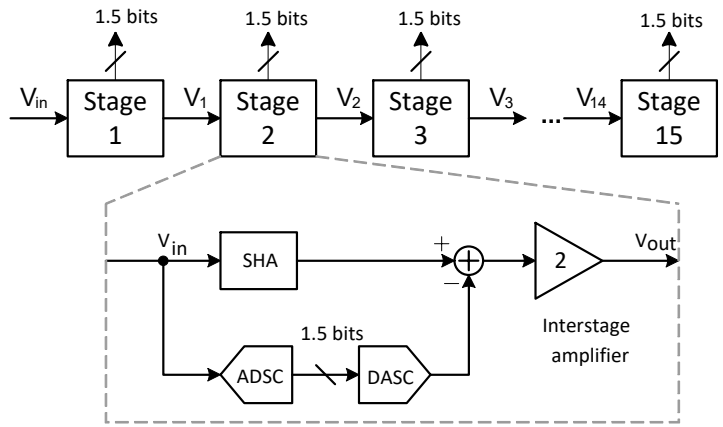


- 16 channels, programmable
- sample/hold
- 12-bit ADC at 2MS/s sampling rate
- current-mode domino architecture
- FIFO 192s bit wide x 32 bits deep
- multiplexer 8:1 or 16:1
- serializer 12:1
- adjustable offsets
- ~4.5 mW/ch.
- power-down modes
- ~ 300,000 MOSFETs
- designed for 77-300K operation
- designed for long lifetime
- tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES



ColdADC ASIC for DUNE



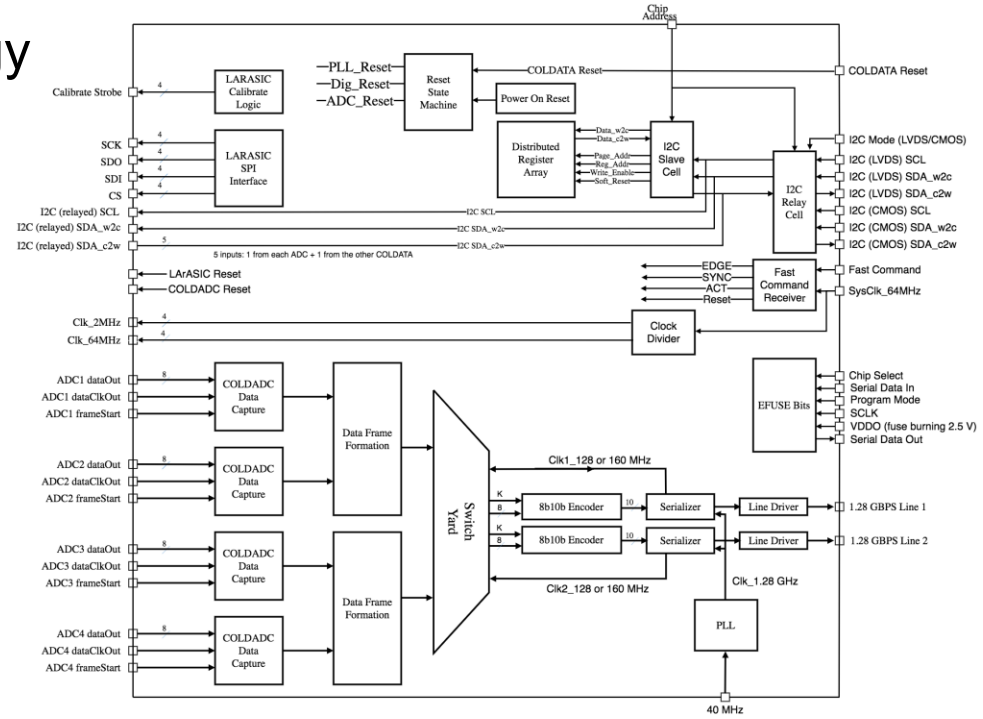


ADC block diagram

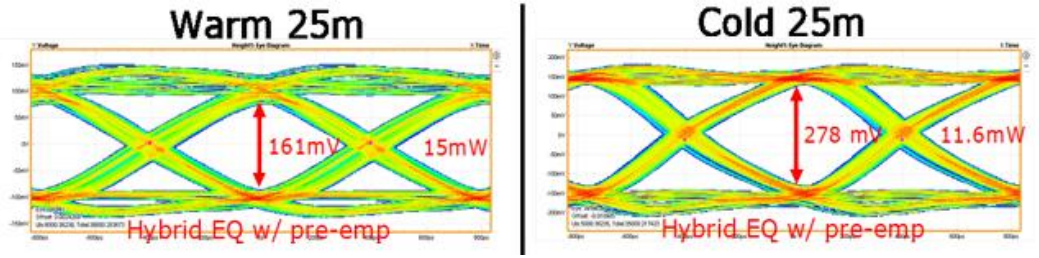
- Designed by joint team from LBNL, FNAL, and BNL
- Cold ADC is a 16-channel, 12-bit, 2 MS/s Digitizer ASIC for the DUNE Far Detector
- Cold ADC uses a conservative, industry-standard design with digital self-calibration
- Besides functionality and reliability, design goal is low-noise and cryogenic operation
- Digital-On-Top Design Methodology
  - 65nm CMOS process, 9 metal stack
    - leverages existing FNAL cold models
    - facilitates potential future integration with COLDATA
  - Chip size: 6860 µm x 7610 µm
- P1 was fully characterized with few issues have been addressed in P2
- P2 was characterized

COLDATA ASIC for DUNE

- Digital-On-Top Design Methodology
  - 65nm CMOS process, 9 metal stack
    - Leverages existing FNAL cold models
- Functions
  - Configure and control 4 COLDADCs and 4 LArASICs
  - Accept data from 4 COLDADCs
  - Format ADC data (truncate to 12 or 14 bits) & pack into an array of 8-bit words
  - Combine packed arrays from pairs of ADCs into 2 output data frames
  - Encode the output data using 8b10b
  - Drive the output data to a WIB at 1.28 Gbps
- P2 was characterized
  - 2 minor known issues
  - 4 requests for modification
- P4 is chosen for DUNE

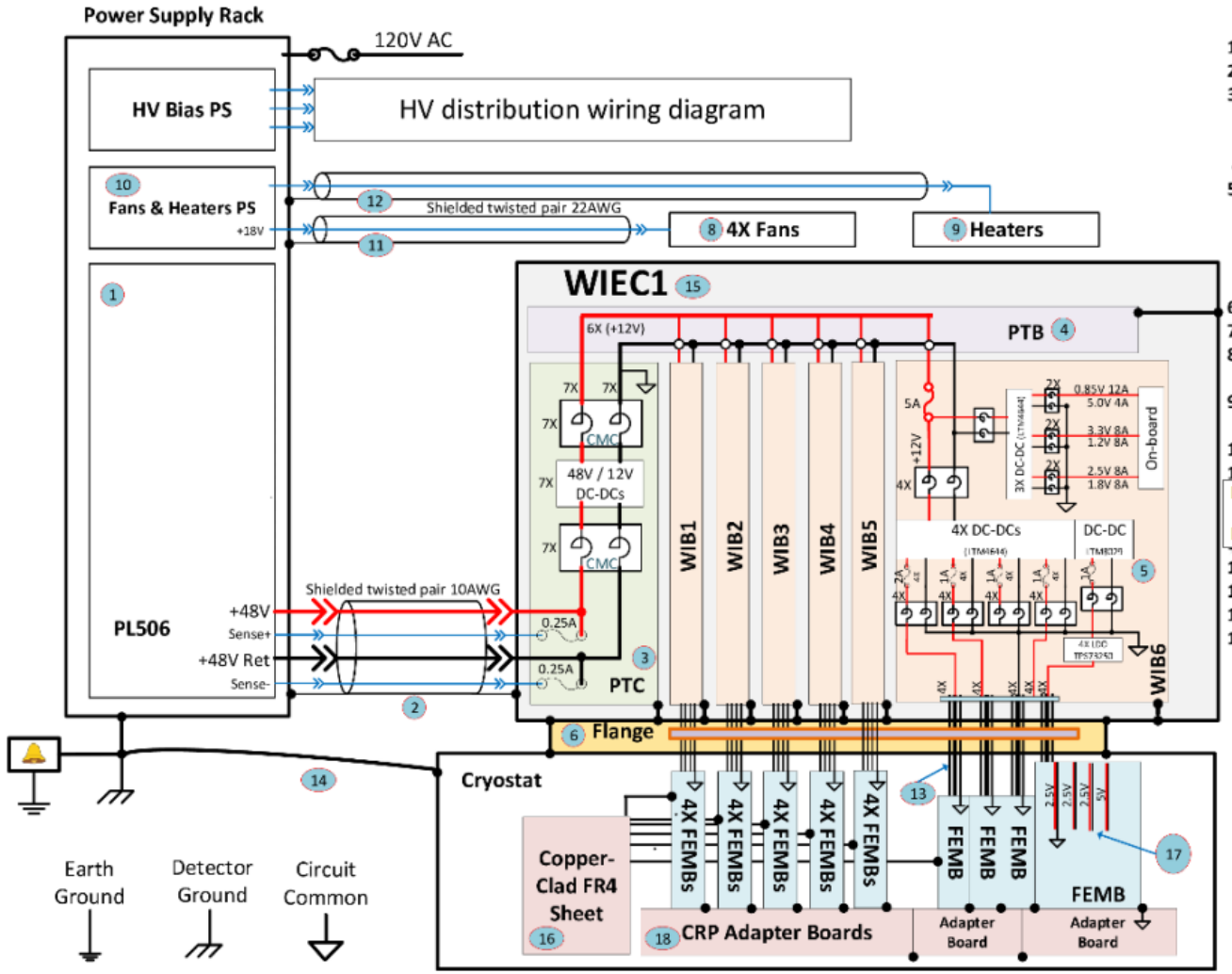


BER < 10^{-15}



Line Driver eye diagram measurement result

Power Distribution



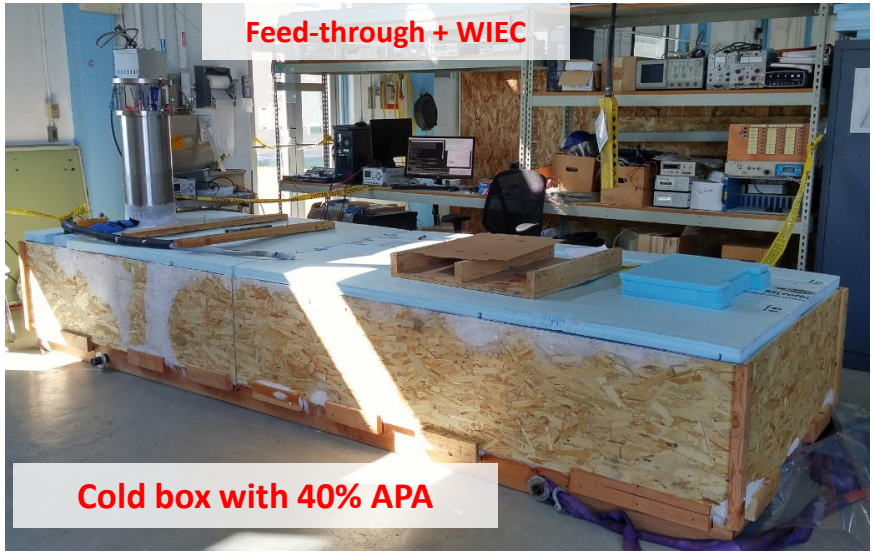
1: Weiner PL506 Power Supply
2: 48V power cable
3: PTC (Power and Timing Card)
0.25A Fuse P/N: 3404.0006.11
Choke P/N: PLT10HH501100PNL
4. PTB (Power and Timing Backplane)
5: WIB (Warm Interface Board Version 3.0)
5A Fuse P/N: 3404.0017.11
2A Fuse P/N: 0468002.NR
1A Fuse P/N: 0468001.NR
Choke P/N: PLT5BPH5013R1SNL
6: Flange Board
7: FEMB (Monolithic Front End Motherboard)
8: Fans box
Fans are electrical isolated from WIEC
9: Heater
Heater is electrical isolated from WIEC
10: Fans & Heater power supply
11: Fans power cable (shielded)

Diagram, schematic
Description automatically generated

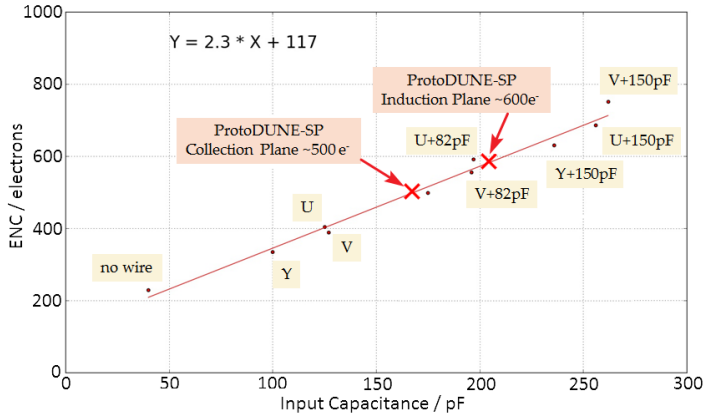
15: Warm Interface Electronics Crate (WIEC)
16: Copper sheet underneath the CRP composite frame
17: Voltage measured at FEMB
18: Adapter boards for the FEMBs to plug into
Note: Each adapter board takes 1 or 2 FEMBs, but adjacent boards are electrically and mechanically interconnected

Notes
(1) Fans and heaters are isolated from WIEC
(2) PTB is mounted with the brass standoffs as a grounding connection
(3) The grounding connection between WIBs and WIEC is through front panels and side bars
(4) The grounding connection between PTB and WIEC is through front panels and side bars
(5) Flange (and flange board) is the place that the FEMB circuit common is referenced to the cryostat (detector ground)

40% APA Integration Test at BNL



40% APA: 2.8m x 1.0m, 1024 wires



Note: 82pF and 150pF mica capacitors are added on some wires

- **40% APA**
  - **U/V wire: 4.0 m**
  - **Y wire: 2.8 m**
- ProtoDUNE APA
  - U/V wire: 7.39m
  - Y wire: 6.0m

- **DUNE Far Detector (FD1)**
  - Same APA as ProtoDUNE-SP
  - Threshold: 1,000 e-
  - Goal: as low as possible