H2GCROC testing stand for DAQ

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Special thanks for Miklos Czeller, Gabor Nagy, Shihai Jia and Martin Purschke

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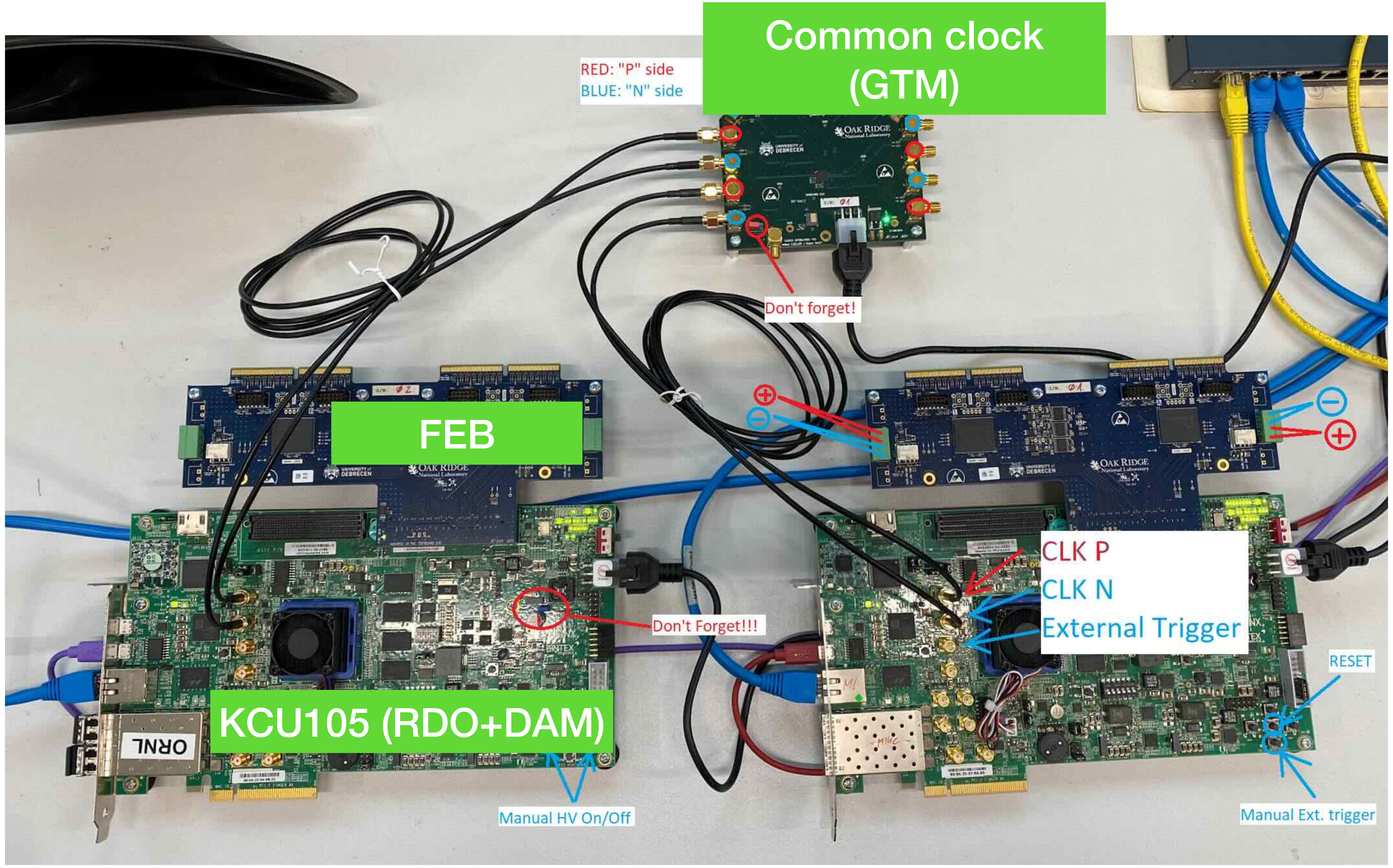
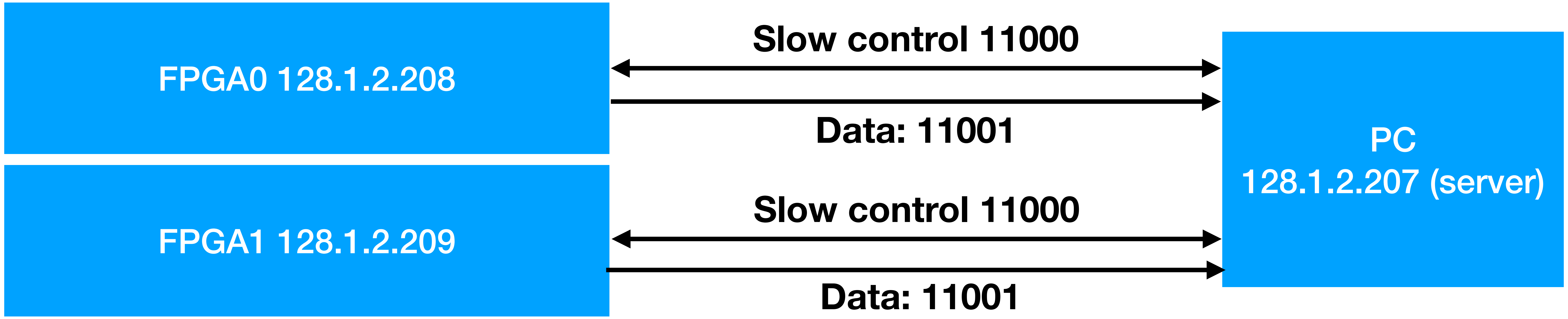
What do we have



We made a test setup to run H2GCROC setup:

- Using the KCU105 (Kintex Ultrascale) evaluation board for communicating with the ASIC and sending UDP packages (also provide low voltage power)
- KCU could service up to 8 H2GCROCs, we choose 2 because of the CAEN interface board swap
- KCU can accept external LVDS clock in order to synchronize different KCU boards (when you have multiple)



FPGA0 128.1.2.208

Slow control 11000

Data: 11001

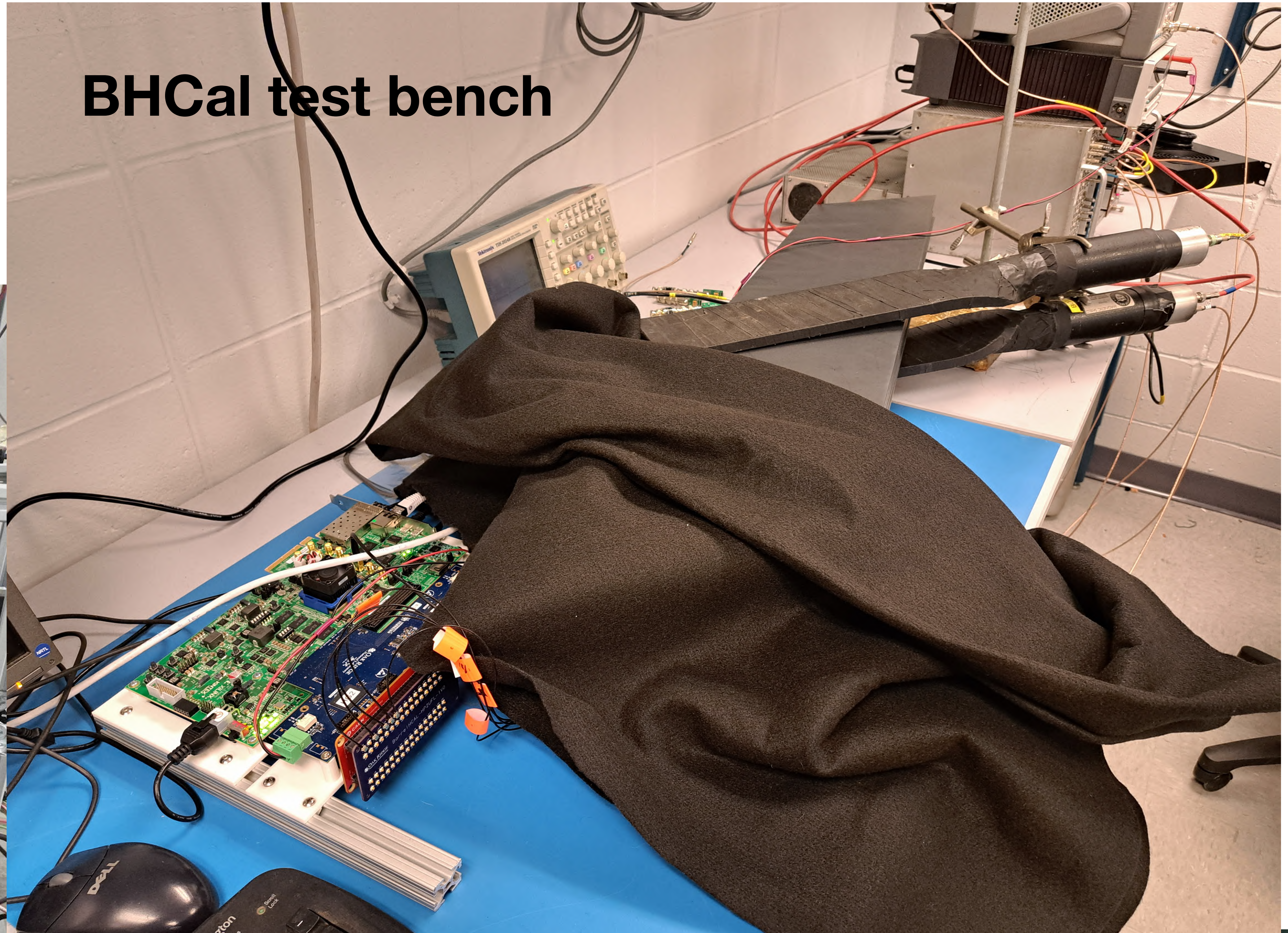
FPGA1 128.1.2.209

Slow control 11000

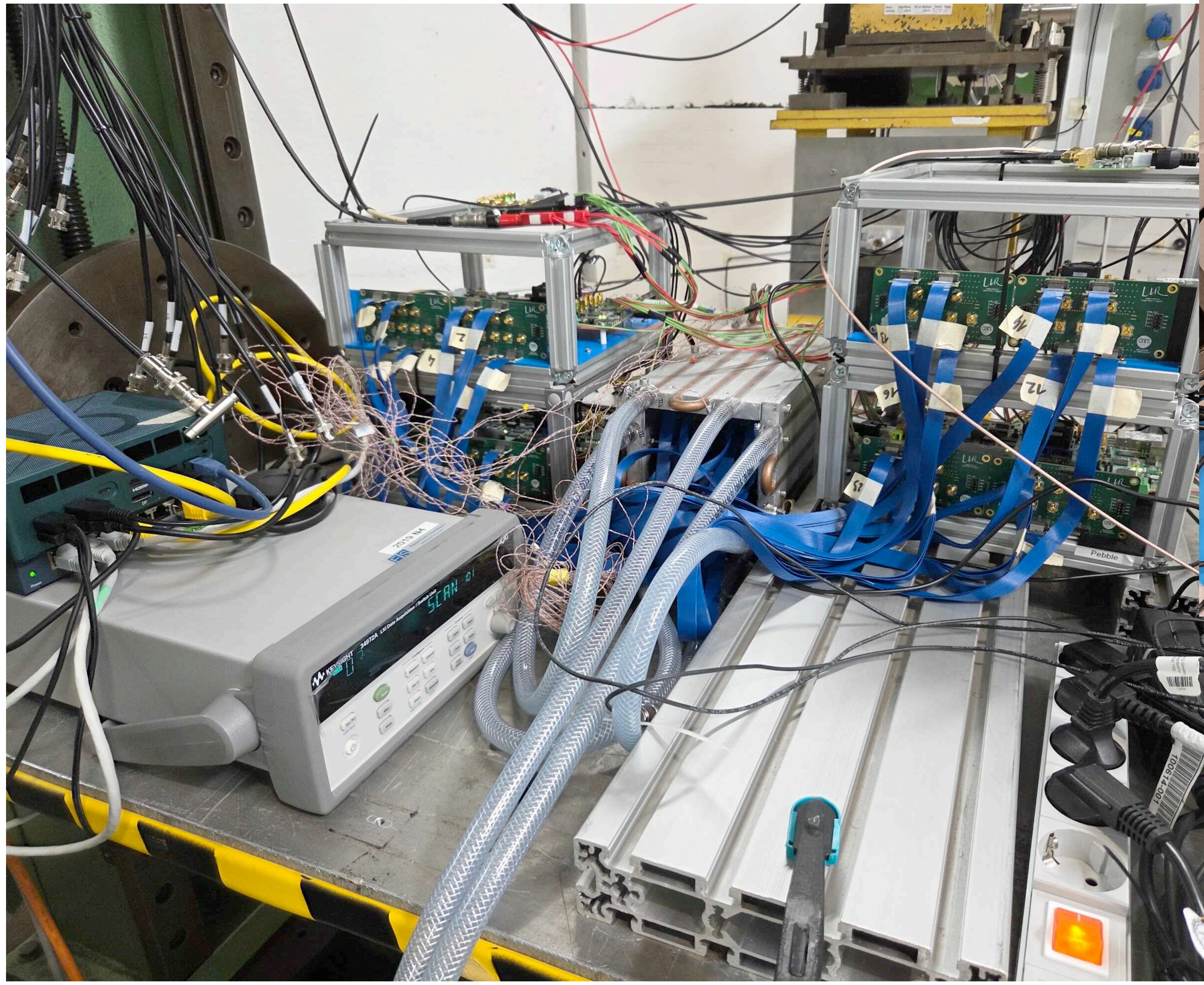
Data: 11001

PC
128.1.2.207 (server)

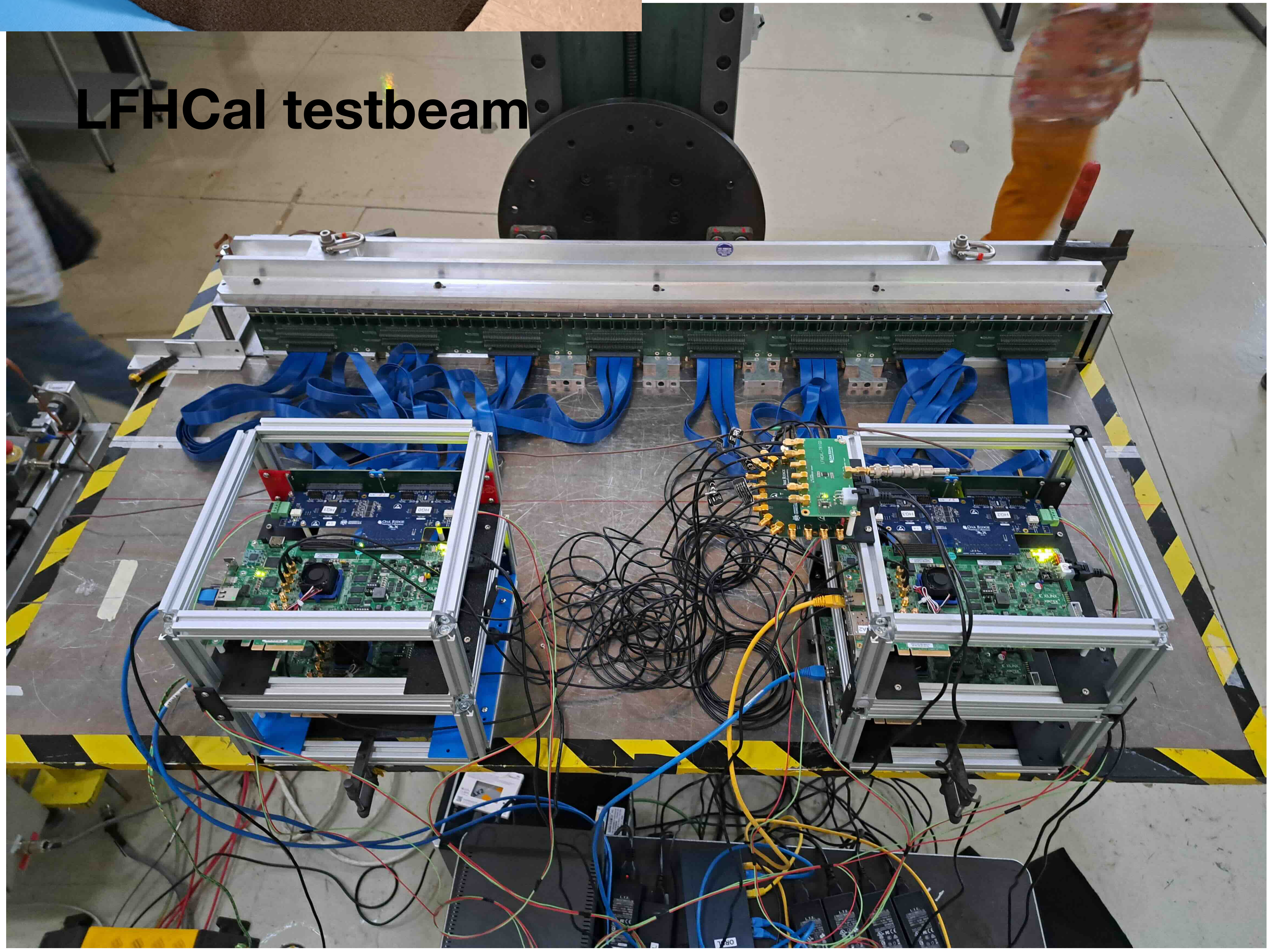
Couple of pictures



BHCal test bench

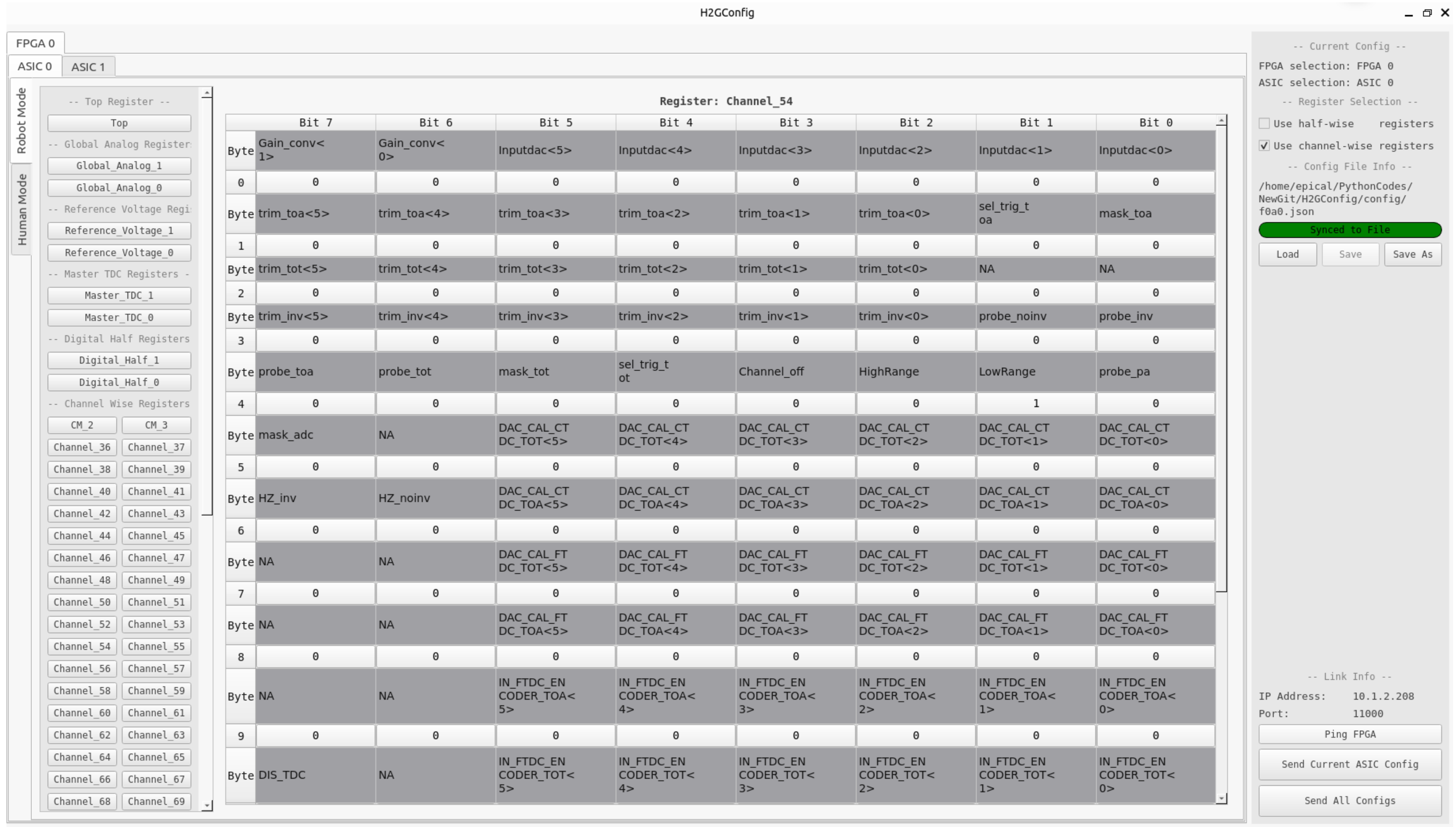


EEMCal testbeam



LFHCal testbeam

Software



H2GConfig

FPGA 0

ASIC 0 | ASIC 1

Robot Mode | Human Mode

-- Top Register --
Top
-- Global Analog Register
Global_Analog_1
Global_Analog_0
-- Reference Voltage Regi
Reference_Voltage_1
Reference_Voltage_0
-- Master TDC Registers -
Master_TDC_1
Master_TDC_0
-- Digital Half Registers
Digital_Half_1
Digital_Half_0
-- Channel Wise Registers
CM_2 CM_3
Channel_36 Channel_37
Channel_38 Channel_39
Channel_40 Channel_41
Channel_42 Channel_43
Channel_44 Channel_45
Channel_46 Channel_47
Channel_48 Channel_49
Channel_50 Channel_51
Channel_52 Channel_53
Channel_54 Channel_55
Channel_56 Channel_57
Channel_58 Channel_59
Channel_60 Channel_61
Channel_62 Channel_63
Channel_64 Channel_65
Channel_66 Channel_67
Channel_68 Channel_69

Register: Channel_54

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte	Gain_conv<1>	Gain_conv<0>	Inputdac<5>	Inputdac<4>	Inputdac<3>	Inputdac<2>	Inputdac<1>	Inputdac<0>
0	0	0	0	0	0	0	0	0
Byte	trim_toa<5>	trim_toa<4>	trim_toa<3>	trim_toa<2>	trim_toa<1>	trim_toa<0>	sel_trig_toa	mask_toa
1	0	0	0	0	0	0	0	0
Byte	trim_tot<5>	trim_tot<4>	trim_tot<3>	trim_tot<2>	trim_tot<1>	trim_tot<0>	NA	NA
2	0	0	0	0	0	0	0	0
Byte	trim_inv<5>	trim_inv<4>	trim_inv<3>	trim_inv<2>	trim_inv<1>	trim_inv<0>	probe_noinv	probe_inv
3	0	0	0	0	0	0	0	0
Byte	probe_toa	probe_tot	mask_tot	sel_trig_tot	Channel_off	HighRange	LowRange	probe_pa
4	0	0	0	0	0	0	1	0
Byte	mask_adc	NA	DAC_CAL_CTDC_TOT<5>	DAC_CAL_CTDC_TOT<4>	DAC_CAL_CTDC_TOT<3>	DAC_CAL_CTDC_TOT<2>	DAC_CAL_CTDC_TOT<1>	DAC_CAL_CTDC_TOT<0>
5	0	0	0	0	0	0	0	0
Byte	HZ_inv	HZ_noinv	DAC_CAL_CTDC_TOA<5>	DAC_CAL_CTDC_TOA<4>	DAC_CAL_CTDC_TOA<3>	DAC_CAL_CTDC_TOA<2>	DAC_CAL_CTDC_TOA<1>	DAC_CAL_CTDC_TOA<0>
6	0	0	0	0	0	0	0	0
Byte	NA	NA	DAC_CAL_FTDC_TOT<5>	DAC_CAL_FTDC_TOT<4>	DAC_CAL_FTDC_TOT<3>	DAC_CAL_FTDC_TOT<2>	DAC_CAL_FTDC_TOT<1>	DAC_CAL_FTDC_TOT<0>
7	0	0	0	0	0	0	0	0
Byte	NA	NA	DAC_CAL_FTDC_TOA<5>	DAC_CAL_FTDC_TOA<4>	DAC_CAL_FTDC_TOA<3>	DAC_CAL_FTDC_TOA<2>	DAC_CAL_FTDC_TOA<1>	DAC_CAL_FTDC_TOA<0>
8	0	0	0	0	0	0	0	0
Byte	NA	NA	IN_FTDC_ENCODER_TOA<5>	IN_FTDC_ENCODER_TOA<4>	IN_FTDC_ENCODER_TOA<3>	IN_FTDC_ENCODER_TOA<2>	IN_FTDC_ENCODER_TOA<1>	IN_FTDC_ENCODER_TOA<0>
9	0	0	0	0	0	0	0	0
Byte	DIS_TDC	NA	IN_FTDC_ENCODER_TOT<5>	IN_FTDC_ENCODER_TOT<4>	IN_FTDC_ENCODER_TOT<3>	IN_FTDC_ENCODER_TOT<2>	IN_FTDC_ENCODER_TOT<1>	IN_FTDC_ENCODER_TOT<0>

-- Current Config --
FPGA selection: FPGA 0
ASIC selection: ASIC 0
-- Register Selection --
□ Use half-wise registers
☑ Use channel-wise registers
-- Config File Info --
/home/epical/PythonCodes/NewGit/H2GConfig/config/f0a0.json
Synced to File
Load | Save | Save As

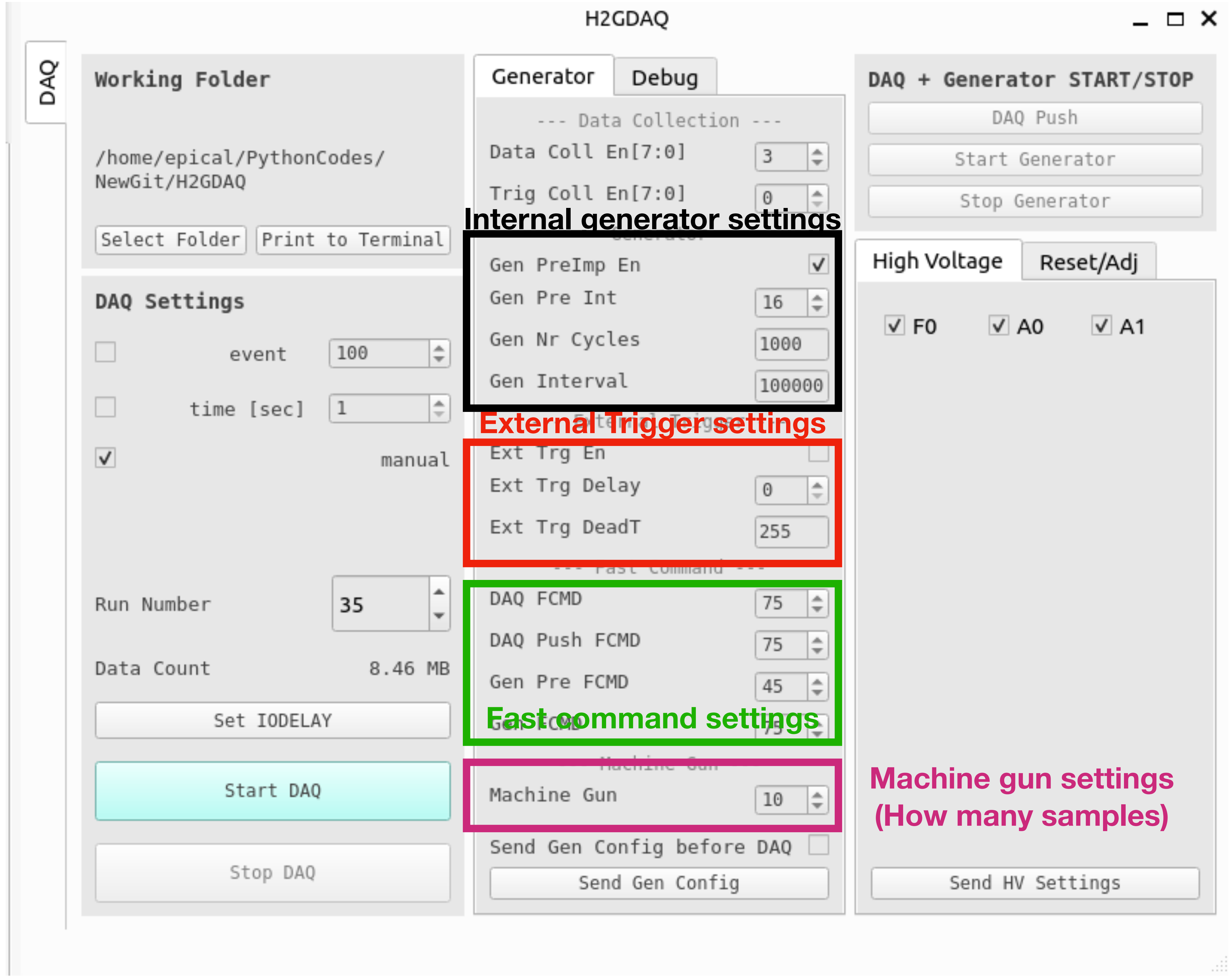
-- Link Info --
IP Address: 10.1.2.208
Port: 11000
Ping FPGA
Send Current ASIC Config
Send All Configs

Slow Control for the H2GCROC:

- N FPGA with 2 H2GCROC setup (1x2 in this case)
- All registers are settable and working

DAQ is very simple:

- Generator settings - all in 40MHz
- External trigger
  - Ext. trigger delay - needs to avoid the UDP packet loss
- Daq push - 1 event
- HV on/off for the board
- Adjustment if there is a misalignment, debugging



H2GDAQ

DAQ

Working Folder

/home/epical/PythonCodes/NewGit/H2GDAQ

Select Folder | Print to Terminal

DAQ Settings

□ event 100
□ time [sec] 1
☑ manual

Run Number 35

Data Count 8.46 MB

Set IODELAY

Start DAQ

Stop DAQ

Generator | Debug

--- Data Collection ---
Data Coll En[7:0] 3
Trig Coll En[7:0] 0

Internal generator settings

--- Generator ---
Gen PreImp En ☑
Gen Pre Int 16
Gen Nr Cycles 1000
Gen Interval 100000

External Trigger settings

--- External Trigger ---
Ext Trg En □
Ext Trg Delay 0
Ext Trg DeadT 255

--- Fast Command ---
DAQ FCMD 75
DAQ Push FCMD 75
Gen Pre FCMD 45
Gen FCMD 75

Fast command settings

--- Machine Gun ---
Machine Gun 10

Send Gen Config before DAQ □
Send Gen Config

DAQ + Generator START/STOP

DAQ Push
Start Generator
Stop Generator

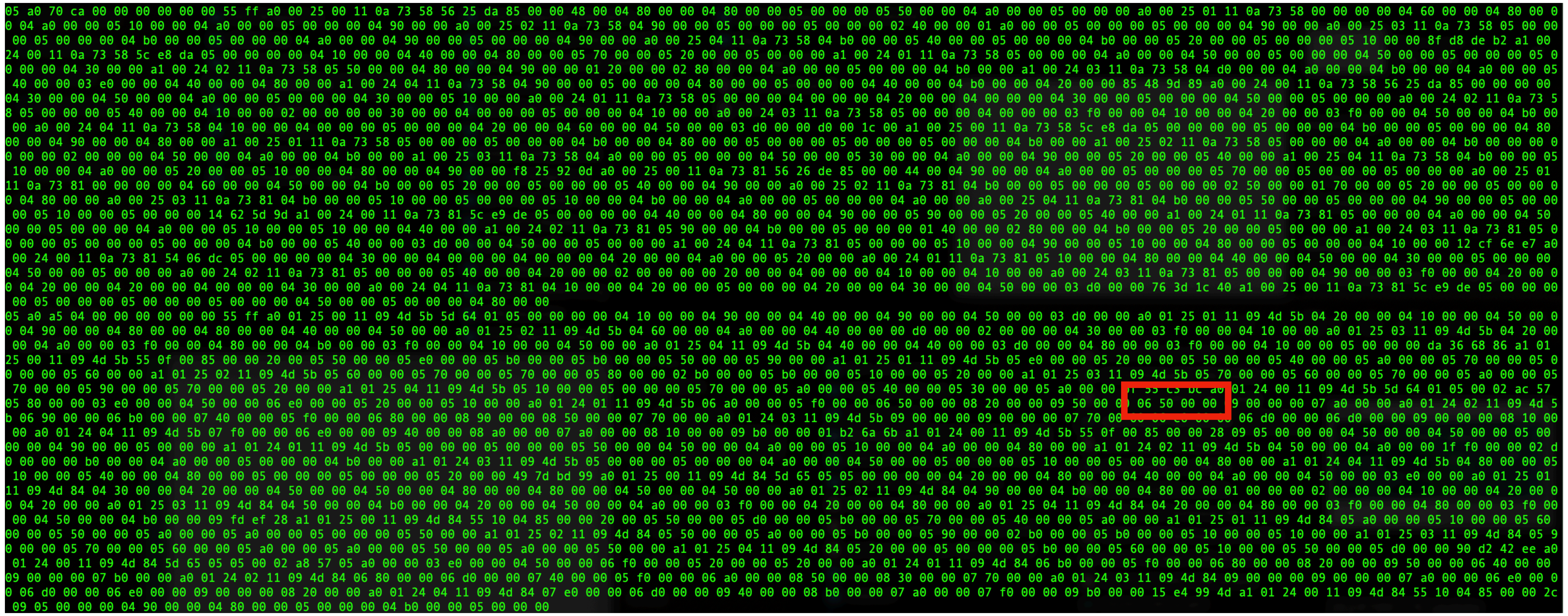
High Voltage | Reset/Adj

☑ F0 ☑ A0 ☑ A1

Send HV Settings

Machine gun settings (How many samples)

Data and data format



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0 04 a0 00 00 05 10 00 00 04 a0 00 00 05 00 00 00 04 90 00 00 a0 00 25 02 11 0a 73 58 04 90 00 00 05 00 00 00 05 00 00 00 02 40 00 00 01 a0 00 00 05 00 00 00 05 00 00 00 04 90 00 00 a0 00 25 03 11 0a 73 58 05 00 00
 00 05 00 00 00 04 b0 00 00 05 00 00 00 04 a0 00 00 04 90 00 00 05 00 00 00 04 90 00 00 a0 00 25 04 11 0a 73 58 04 b0 00 00 05 40 00 00 05 00 00 00 04 b0 00 00 05 20 00 00 05 00 00 00 05 10 00 00 8f d8 de b2 a1 00
24 00 11 0a 73 58 5c e8 da 05 00 00 00 00 04 10 00 00 04 40 00 00 04 80 00 00 05 70 00 00 05 20 00 00 05 00 00 00 a1 00 24 01 11 0a 73 58 05 00 00 00 04 a0 00 00 04 50 00 00 05 00 00 00 04 50 00 00 05 00 00 00 05 0
0 00 00 04 30 00 00 a1 00 24 02 11 0a 73 58 05 50 00 00 04 80 00 00 04 90 00 00 01 20 00 00 02 80 00 00 04 a0 00 00 05 00 00 00 04 b0 00 00 a1 00 24 03 11 0a 73 58 04 d0 00 00 04 a0 00 00 04 b0 00 00 04 a0 00 00 05
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 00 05 00 00 00 05 00 00 00 05 00 00 00 04 50 00 00 05 00 00 00 04 80 00 00
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0 04 90 00 00 04 80 00 00 04 80 00 00 04 40 00 00 04 50 00 00 a0 01 25 02 11 09 4d 5b 04 60 00 00 04 a0 00 00 04 40 00 00 00 d0 00 00 02 00 00 00 04 30 00 00 03 f0 00 00 04 10 00 00 a0 01 25 03 11 09 4d 5b 04 20 00
 00 04 a0 00 00 03 f0 00 00 04 80 00 00 04 b0 00 00 03 f0 00 00 04 10 00 00 04 50 00 00 a0 01 25 04 11 09 4d 5b 04 40 00 00 04 40 00 00 03 d0 00 00 04 80 00 00 03 f0 00 00 04 10 00 00 05 00 00 00 da 36 68 86 a1 01
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09 00 00 00 07 b0 00 00 a0 01 24 02 11 09 4d 84 06 80 00 00 06 d0 00 00 07 40 00 00 05 f0 00 00 06 a0 00 00 08 50 00 00 08 30 00 00 07 70 00 00 a0 01 24 03 11 09 4d 84 09 00 00 00 09 00 00 00 07 a0 00 00 06 e0 00 0
0 06 d0 00 00 06 e0 00 00 09 00 00 00 08 20 00 00 a0 01 24 04 11 09 4d 84 07 e0 00 00 06 d0 00 00 09 40 00 00 08 b0 00 00 07 a0 00 00 07 f0 00 00 09 b0 00 00 15 e4 99 4d a1 01 24 00 11 09 4d 84 55 10 04 85 00 00 2c
 09 05 00 00 00 04 90 00 00 04 80 00 00 05 00 00 00 04 b0 00 00 05 00 00 00
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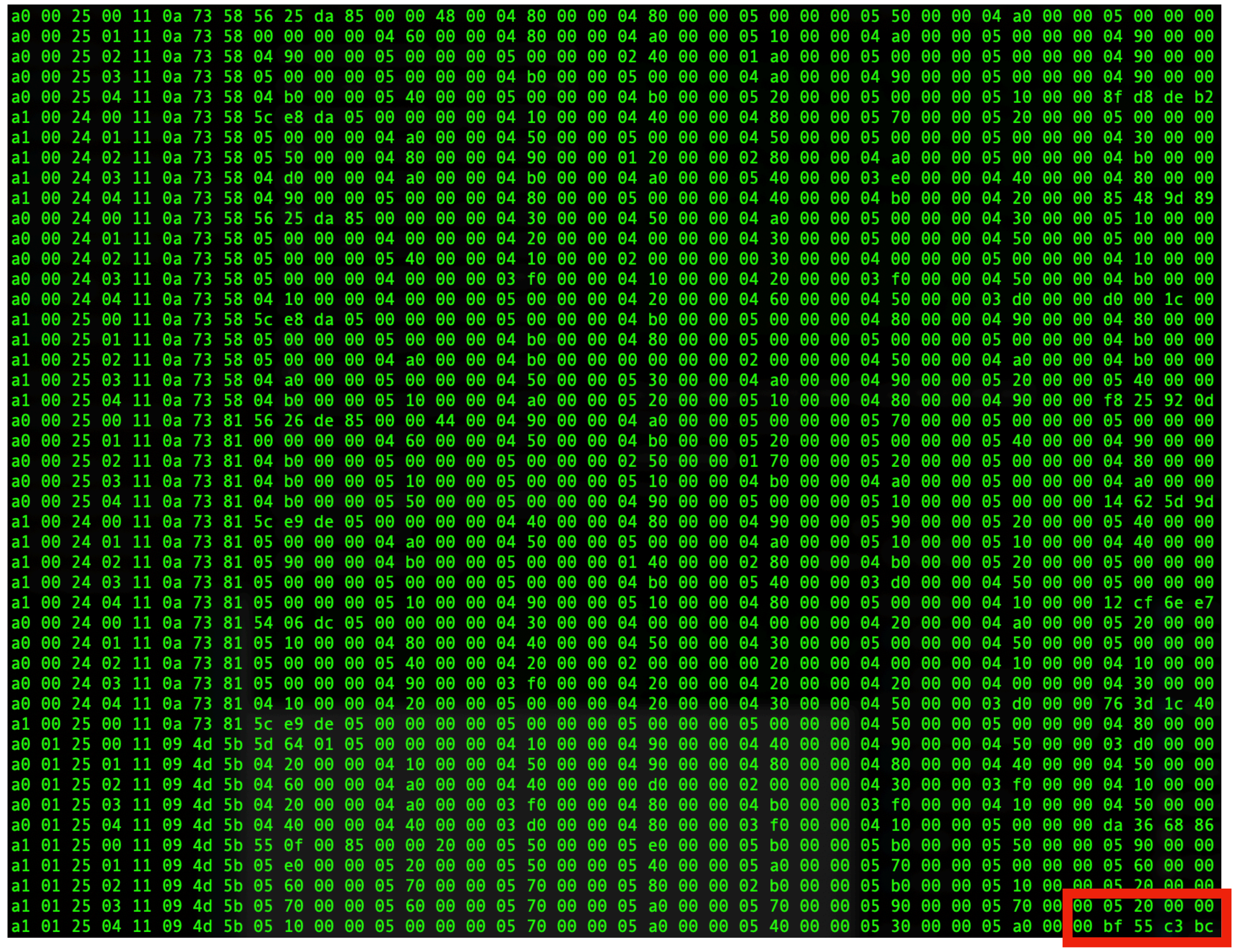
The KCU105 is just packaging the data in full **1454 bytes UDP packages** and dumps them towards the PC:

- First 12 bytes are UDP header - counting the packet number for looking if we lost something
- Data dump from the H2GCROCs

The data is dumped in 40-byte chunks:

- First 32-bit word ASIC ID, FPGA ID, ASIC HalfID, LineID (5 lines is full readout):
  - Always starts with A0—A7 for 8 ASICs per FPGA
- Second 32-bit word is FPGA counter (40MHz):
  - This we use to stitch the events together
  - Also used to synchronize multiple FPGA's together
- H2GCROC data dump:
  - 5 lines, 80x32 bit = 2560 bit in total



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a0 00 25 02 11 0a 73 58 04 90 00 00 05 00 00 00 05 00 00 00 02 40 00 00 01 a0 00 00 05 00 00 00 05 00 00 00 04 90 00 00
a0 00 25 03 11 0a 73 58 05 00 00 00 05 00 00 00 04 b0 00 00 05 00 00 00 04 a0 00 00 04 90 00 00 05 00 00 00 04 90 00 00
a0 00 25 04 11 0a 73 58 04 b0 00 00 05 40 00 00 05 00 00 00 04 b0 00 00 05 20 00 00 05 00 00 00 05 10 00 00 8f d8 de b2
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a1 00 24 03 11 0a 73 58 04 d0 00 00 04 a0 00 00 04 b0 00 00 04 a0 00 00 05 40 00 00 03 e0 00 00 04 40 00 00 04 80 00 00
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a1 00 24 01 11 0a 73 81 05 00 00 00 04 a0 00 00 04 50 00 00 05 00 00 00 04 a0 00 00 05 10 00 00 05 10 00 00 04 40 00 00
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a0 00 24 00 11 0a 73 81 54 06 dc 05 00 00 00 00 04 30 00 00 04 00 00 00 04 00 00 00 04 20 00 00 04 a0 00 00 05 20 00 00
a0 00 24 01 11 0a 73 81 05 10 00 00 04 80 00 00 04 40 00 00 04 50 00 00 04 30 00 00 05 00 00 00 04 50 00 00 05 00 00 00
a0 00 24 02 11 0a 73 81 05 00 00 00 05 40 00 00 04 20 00 00 02 00 00 00 00 20 00 00 04 00 00 00 04 10 00 00 04 10 00 00
a0 00 24 03 11 0a 73 81 05 00 00 00 04 90 00 00 03 f0 00 00 04 20 00 00 04 20 00 00 04 20 00 00 04 00 00 00 04 30 00 00
a0 00 24 04 11 0a 73 81 04 10 00 00 04 20 00 00 05 00 00 00 04 20 00 00 04 30 00 00 04 50 00 00 03 d0 00 00 76 3d 1c 40
a1 00 25 00 11 0a 73 81 5c e9 de 05 00 00 00 00 05 00 00 00 05 00 00 00 05 00 00 00 04 50 00 00 05 00 00 00 04 80 00 00
a0 01 25 00 11 09 4d 5b 5d 64 01 05 00 00 00 00 04 10 00 00 04 90 00 00 04 40 00 00 04 90 00 00 04 50 00 00 03 d0 00 00
a0 01 25 01 11 09 4d 5b 04 20 00 00 04 10 00 00 04 50 00 00 04 90 00 00 04 80 00 00 04 80 00 00 04 40 00 00 04 50 00 00
a0 01 25 02 11 09 4d 5b 04 60 00 00 04 a0 00 00 04 40 00 00 00 d0 00 00 02 00 00 00 04 30 00 00 03 f0 00 00 04 10 00 00
a0 01 25 03 11 09 4d 5b 04 20 00 00 04 a0 00 00 03 f0 00 00 04 80 00 00 04 b0 00 00 03 f0 00 00 04 10 00 00 04 50 00 00
a0 01 25 04 11 09 4d 5b 04 40 00 00 04 40 00 00 03 d0 00 00 04 80 00 00 03 f0 00 00 04 10 00 00 05 00 00 00 da 36 68 86
a1 01 25 00 11 09 4d 5b 55 0f 00 85 00 00 20 00 05 50 00 00 05 e0 00 00 05 b0 00 00 05 b0 00 00 05 50 00 00 05 90 00 00
a1 01 25 01 11 09 4d 5b 05 e0 00 00 05 20 00 00 05 50 00 00 05 40 00 00 05 a0 00 00 05 70 00 00 05 00 00 00 05 60 00 00
a1 01 25 02 11 09 4d 5b 05 60 00 00 05 70 00 00 05 70 00 00 05 80 00 00 02 b0 00 00 05 b0 00 00 05 10 00 00 05 20 00 00
a1 01 25 03 11 09 4d 5b 05 70 00 00 05 60 00 00 05 70 00 00 05 a0 00 00 05 70 00 00 05 90 00 00 05 70 00 00 05 20 00 00
a1 01 25 04 11 09 4d 5b 05 10 00 00 05 00 00 00 05 70 00 00 05 a0 00 00 05 40 00 00 05 30 00 00 05 a0 00 00 bf 55 c3 bc
```

RCDAQ Plugin and work

```
$ daq_status -ll
caloroc2 -  Stopped
  Filerule:      /home/phnxrc/data/junk/junk_ROC-%08d-%04d.evt
  Logging enabled
  Number of buffers/write threads: 2 Buffersize: 64MB
  compression disabled level: 0
  MD5 calculation enabled
  have a trigger object
  Buffer Sizes:      65536 KB adaptive buffering: 15 s
  Web control Port:  8899
  Elog: not defined
  -- defined Run Types:
          cosmics - /home/phnxrc/data/cosmics/cosmics_ROC-%08d-%04d.evt
             junk - /home/phnxrc/data/junk/junk_ROC-%08d-%04d.evt
  List of loaded Plugins:
   - H2GCROC3 Plugin, provides -
 -     device_h2gcroc3 (evttype, subid, IP addr, trigger, nr_packets) - readout an H2GCROC3
```

```
$ daq_list_readlist
File Device  Event Type: 9 Subevent id: 900 reading from /home/phnxrc/ROC/new ROC
firmware/rcdaq_roc.sh
H2GCROC3 Device  Event Type: 1 Subevent id: 12001 IP: 10.1.2.208 nr_packets: 128 trigger
```

The RCDaq in this case is taking over for data taking:

- Slow control and DAQ setup stays with the GUI
- Just need a "start DAQ" script, then just wait for the data to arrive
  - Saved as Packet number 12001

Pro's of using now RCDAQ:

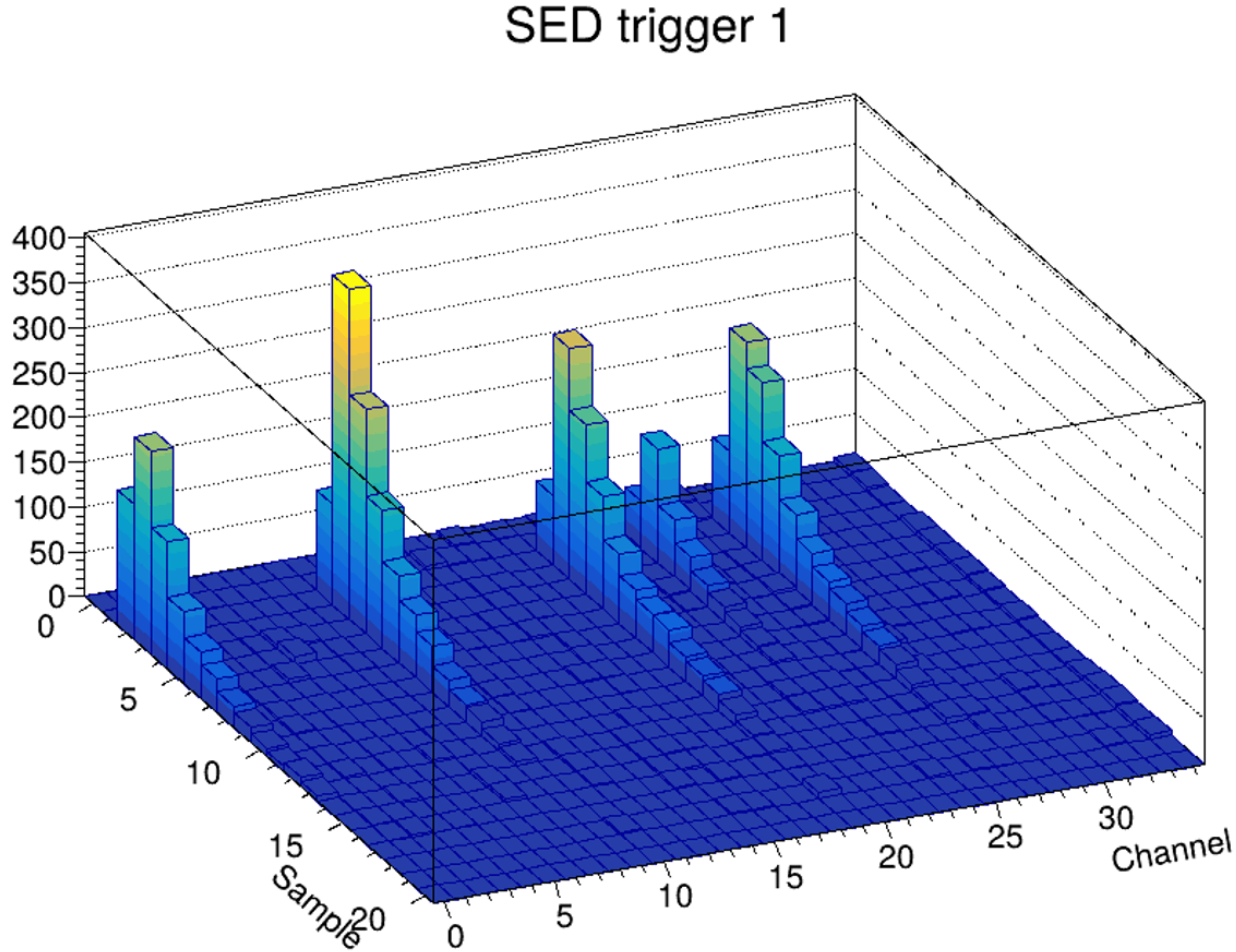
- Built-in online monitoring software (no need to do extra)
  - It decodes the data format already
- Connect multiple devices:
  - Good for testbeams
  - Let's say trigger scintillators can be read out to the data stream
  - Tracking
  - …etc.

```
p->iValue(0,"SAMPLES")  tells you how many samples are present

p->iValue(0,"CHANNELS") tells you how many channels that device has  (here:144)

p->iValue(c,s)          gives you sample s from channel c  (there are faster interfaces available)
```

Eye Candy



5 channels were connected in the Barrel HCal test bench

150 trigger events are reconstructed:

- Full waveform is read out
- Empty events (trigger scintillators does not fully cover the readout scintillators)