ePIC-BIC: Modules and Staves

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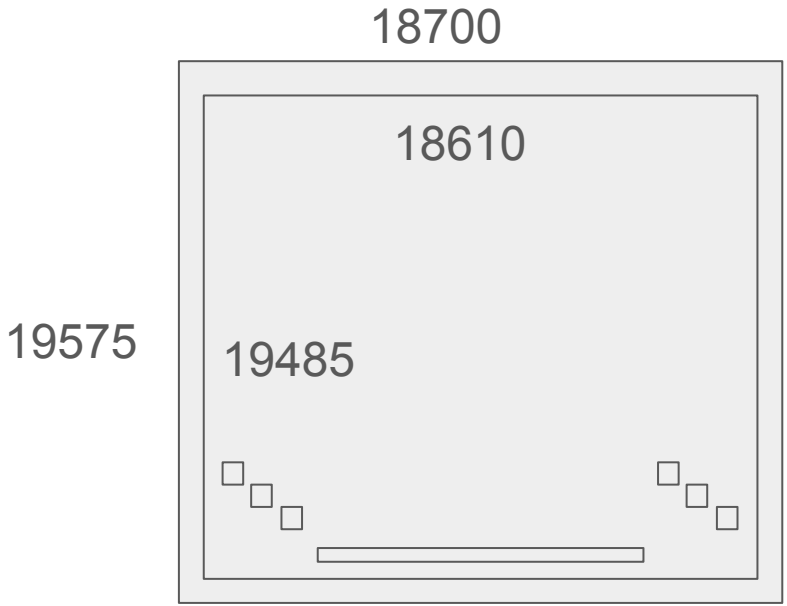
AstroPix Dummies

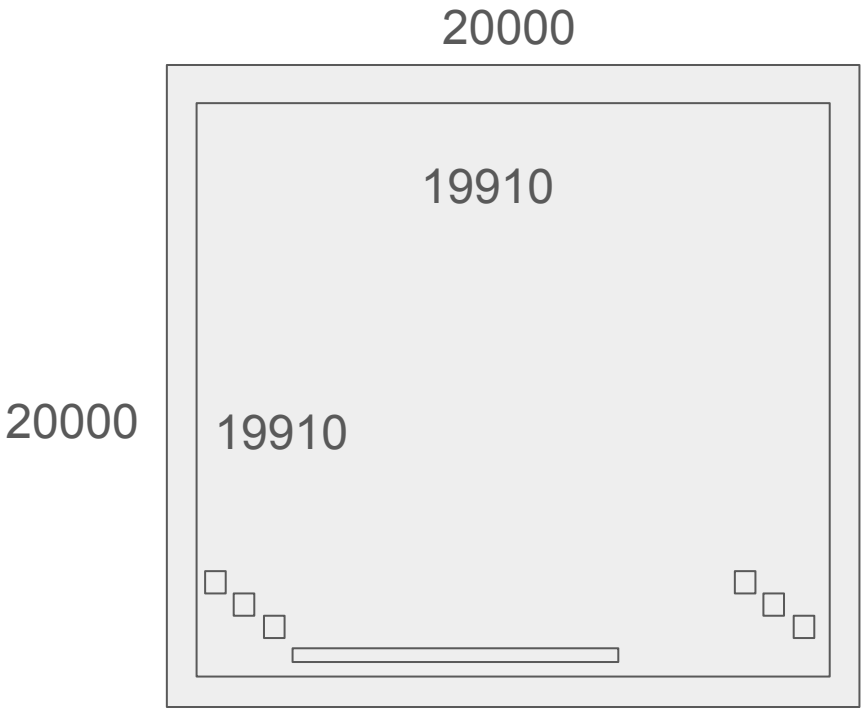
Current V3/V5 design footprint:

- Physical chip size -
  18700 um x 19575 um
- Reticle size -
  18610 um x 19485 um
- Dicing area
  45 um on each side

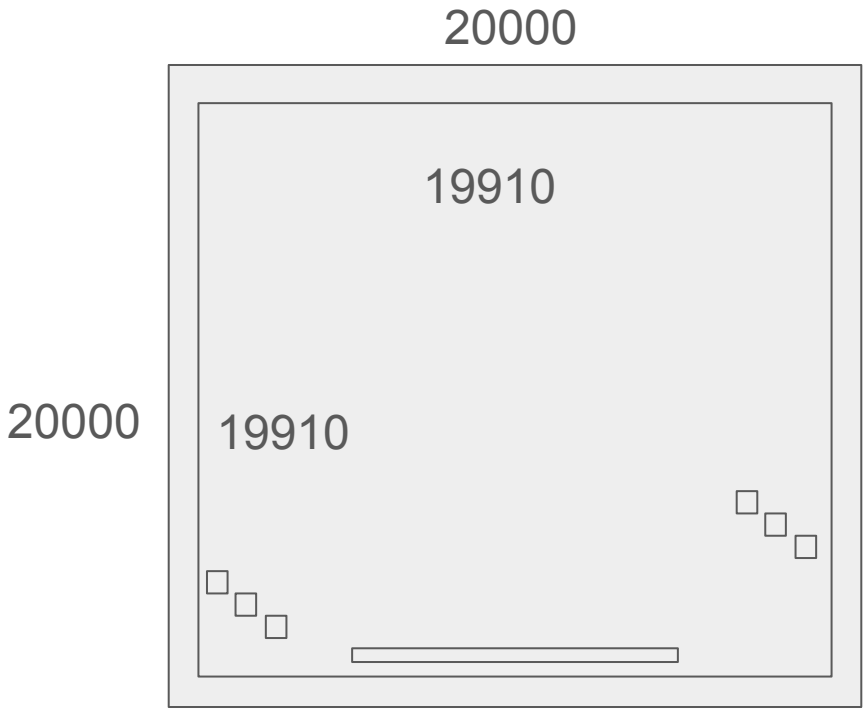


AstroPix Dummies

Two Options to fabricate dummies:

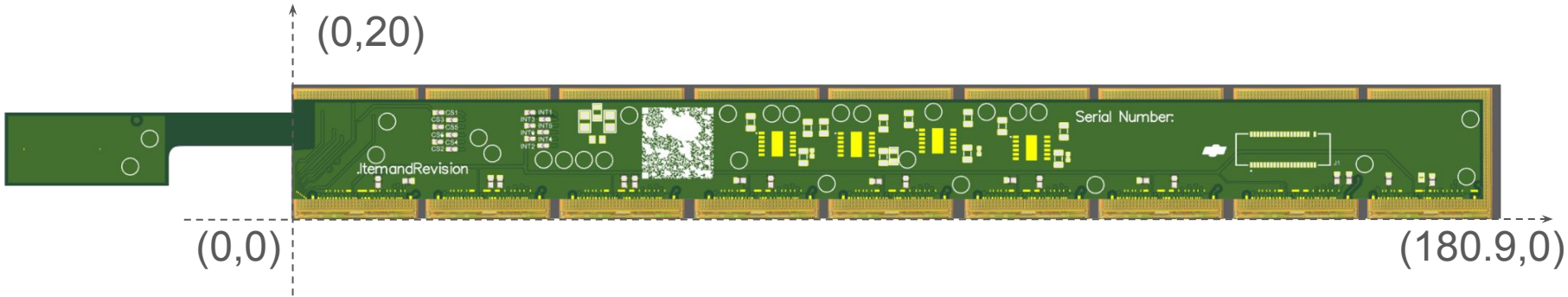


All wirebonds aligned on left edge except SPI right



All wirebonds aligned with center of chip

Coordinate System for Module Assembly



AstroLinx (v3)

Latest version of design file are uploaded to Box folder

- https://anl.box.com/s/l4h16fsao3eqbwn5qsjzo6sqz8h2n6ls

Addresses following topics

- Added 125um silkscreen soldermask clearance
- Total 10 fiducials added
- Alignement with chips - left edge of chip0
  - Tolerance of 300 um to right and 150 um to left of chip edge

Review to be held -

- Two option depending on availability of material
  - Next week (will have a poll to decide time)
  - Next Module/Stave meeting on July 7th
- Need to provide at least a week to Reviewers

To Do list

AstroLinx Review - ASAP

- Quotation
- Order

Coating of PCB? - Sep 2025

- Do we need coating of AstroLinx due small gap in overlap?
  - Conformal coating

Wirebond Potting?

Module Handling toolings

- Design finalization - when?
- Quote and order - Leadtime?
- Decision pick-n-place vs toolings - Aug 2025?

Wirebond program for v3 modules