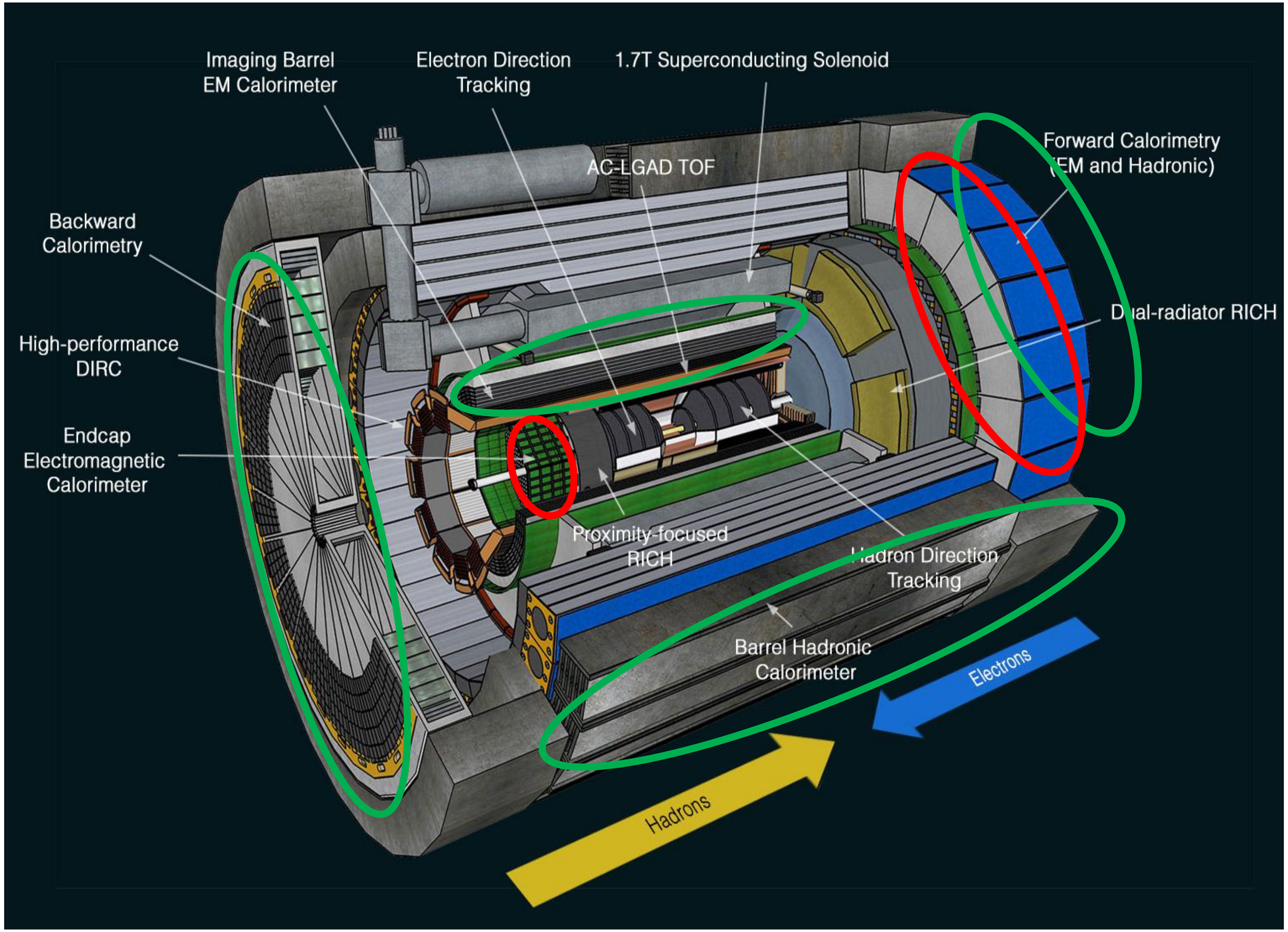
# CALOROC for SiPM readout

## EIC calorimetry

ASIC Meeting - France
2-3 June 2025

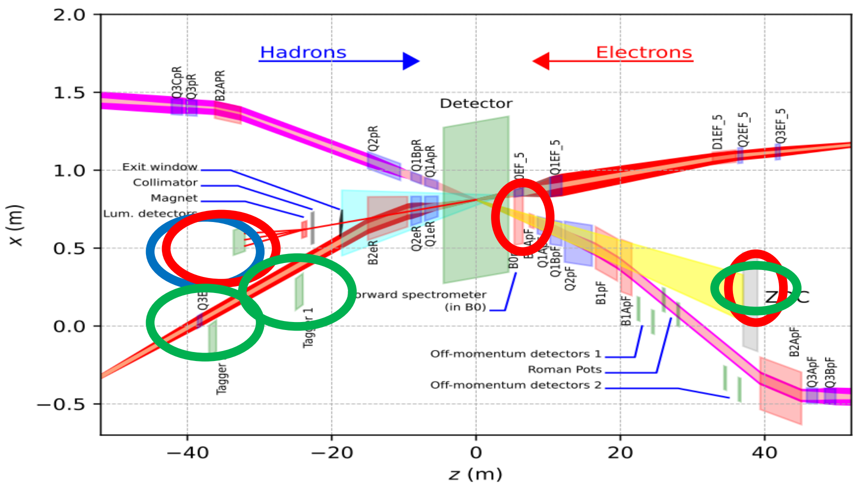
Frederic DULUCQ

Organization for Micro-Electronics desiGn and Applications




13 Calorimeters:

- 7 x SiPM – CALOROC
- 5 x SiPM – Discrete
- 1 x SiPM – Commercial fADC250



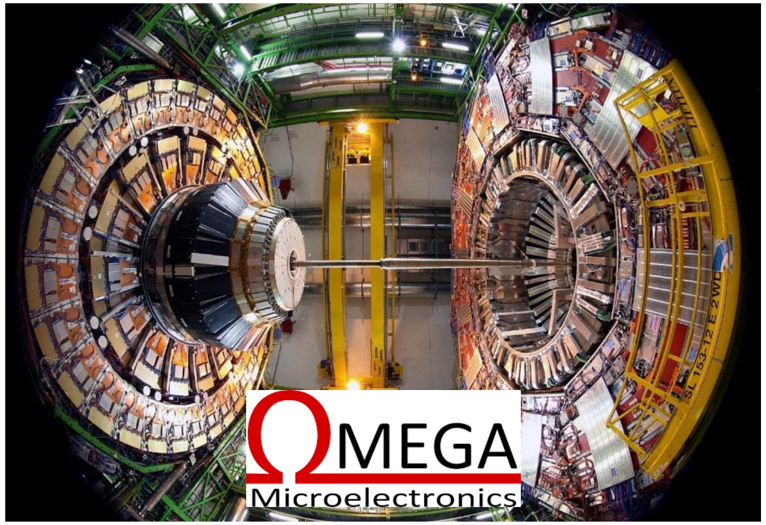

From J. Landgraf

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year




CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

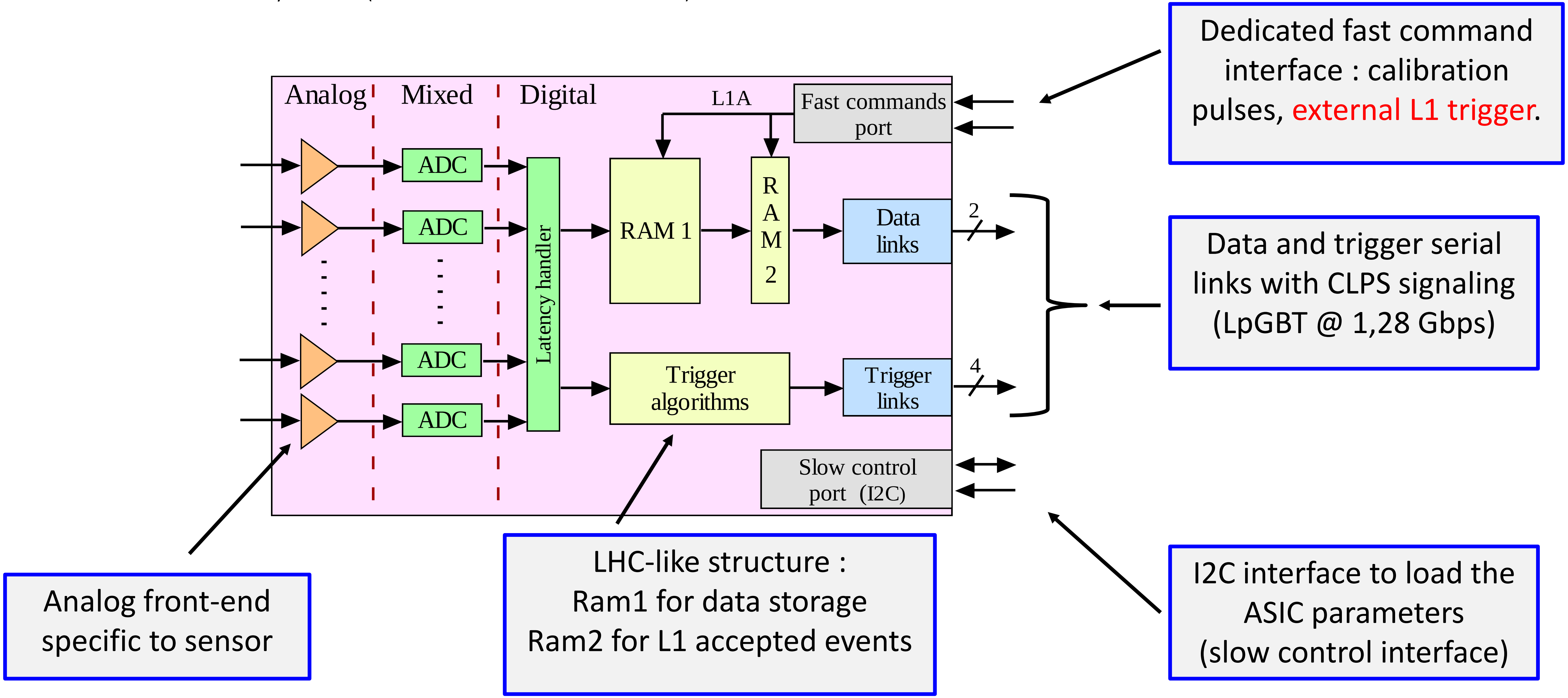
HEP trend => imaging calorimetry

- ❑ High number of channels
- ❑ Charge and precise timing (<100 ps)
- ❑ Low power + System-On-Chip

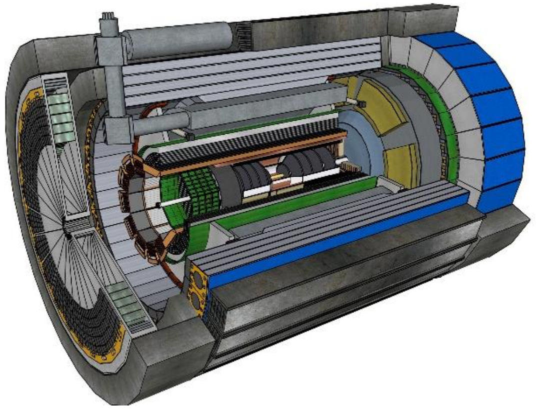
Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

# ROC chips standard structure

- H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (but interfaces for CALOROC will similar)

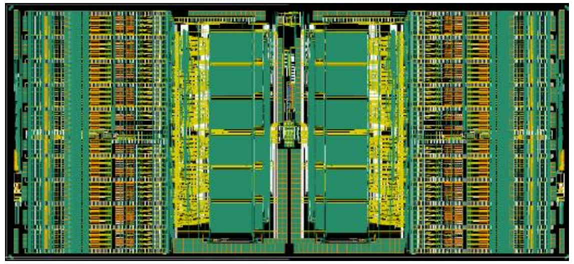


# What is CALOROC ?



- CALOROC will be available in 2 versions for SiPM readout:
  - SiPM range capacitance from 500 pF to 10 nF
  - ~ 10-15 mW / channel
  - Radiation hardening (HL-LHC levels)
    - 200 Mrad and $10^{16}$ $n_{eq}$ / cm² (1 MeV equivalent neutrons)
    - SEE hardening on control logic
  - Charge and time measurement

HGCROC



HKROC

- Streaming readout (no external trigger required)
- Conservative CALOROC1A based on CMS H2GCROC:
  - H2GCROC (ADC, TOT) analog/mixed reuse
  - Back-end compatible with EIC + zero-suppress

CALOROC 1A
CMS front end
EIC readout

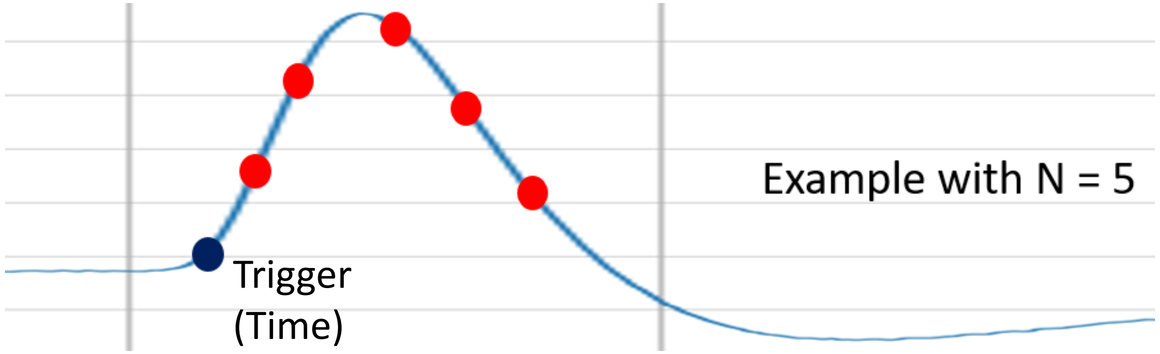
CALOROC 1B
New front end
EIC readout

- New CALOROC1B based on gain switching:
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible

**CALOROCs will share a common backend + pin-pin compatibility**

# CALOROC: waveform digitizer with auto-trigger

- CALOROC is a waveform digitizer working @ 39.4 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)




**CALOROC can accept ~ 50 kHz rate per channel**

Internal HKROC memory writing is without dead time

Hit-rate is only limited by serial link bandwidth (average values above)

A zero-suppress feature can be activated or not

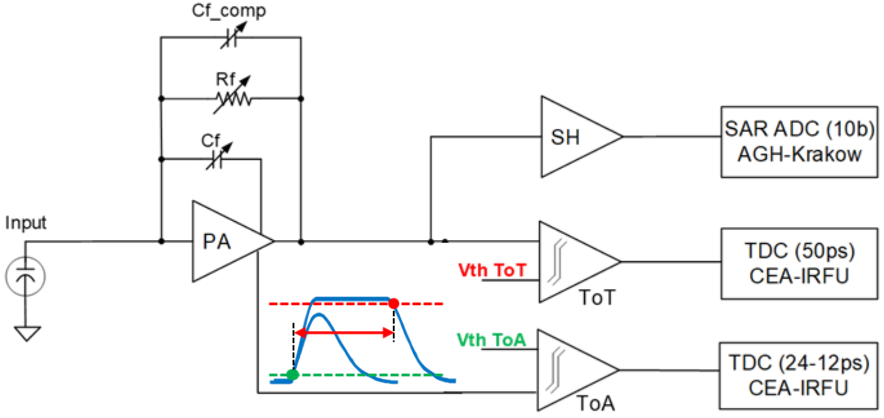
A fast command can trigger an ASIC snapshot

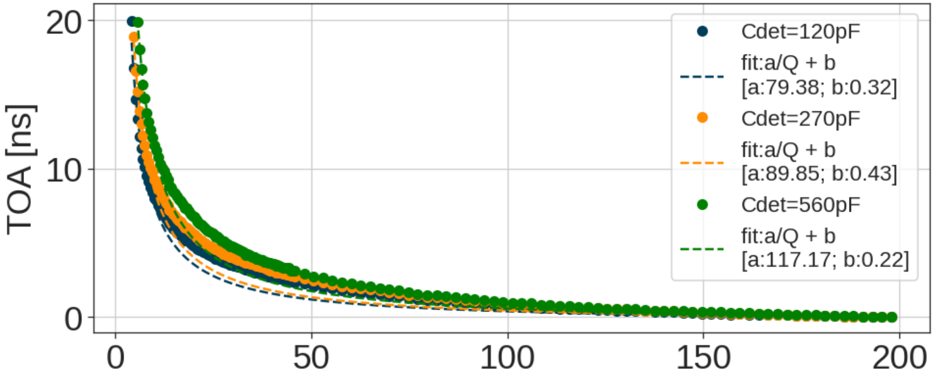
(monitoring, calibration, heartbeat)

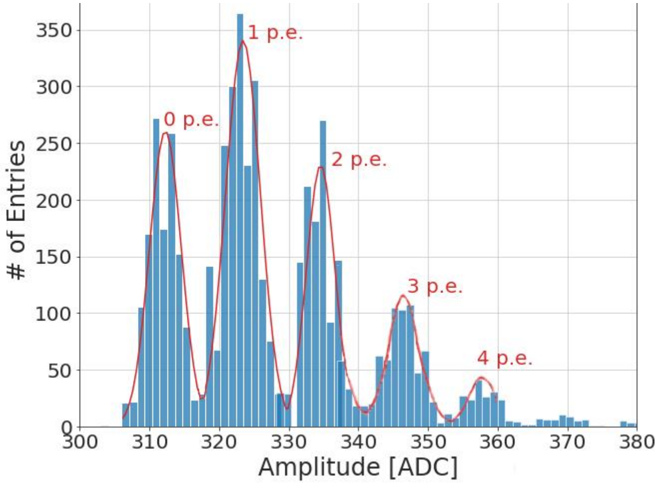
# CALOROC1A (based on H2GCROC)

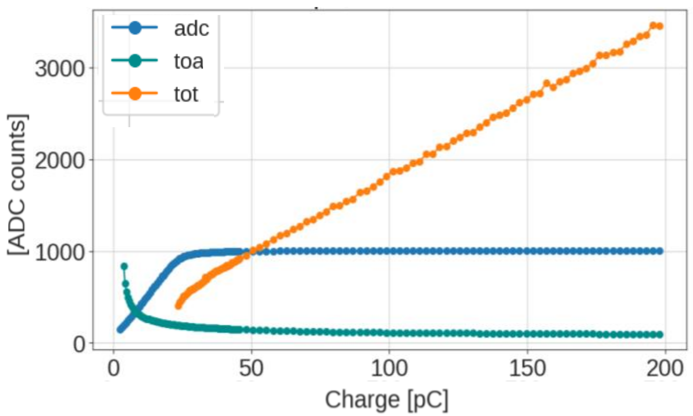
Ωmega

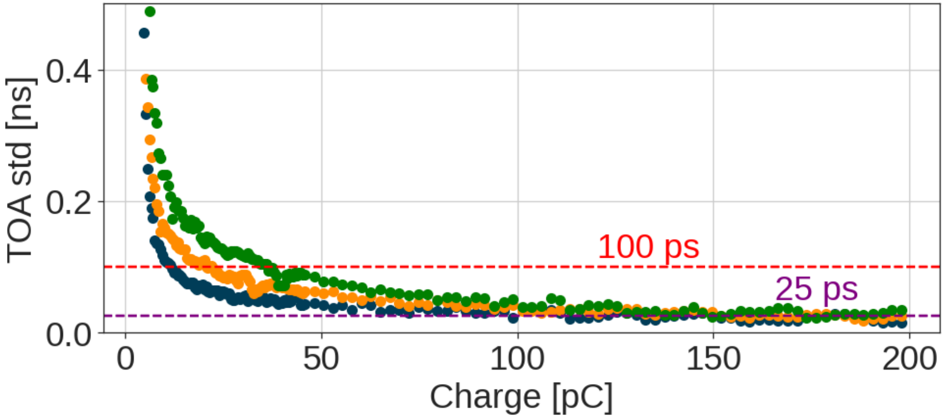
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM range 100-600 pF

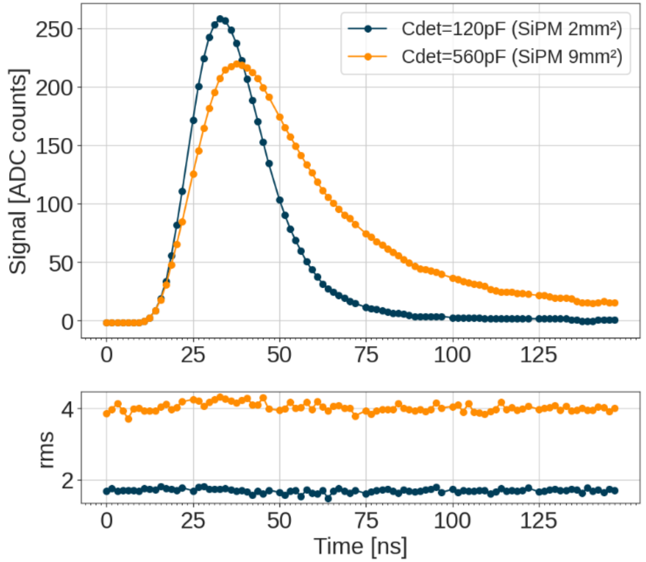


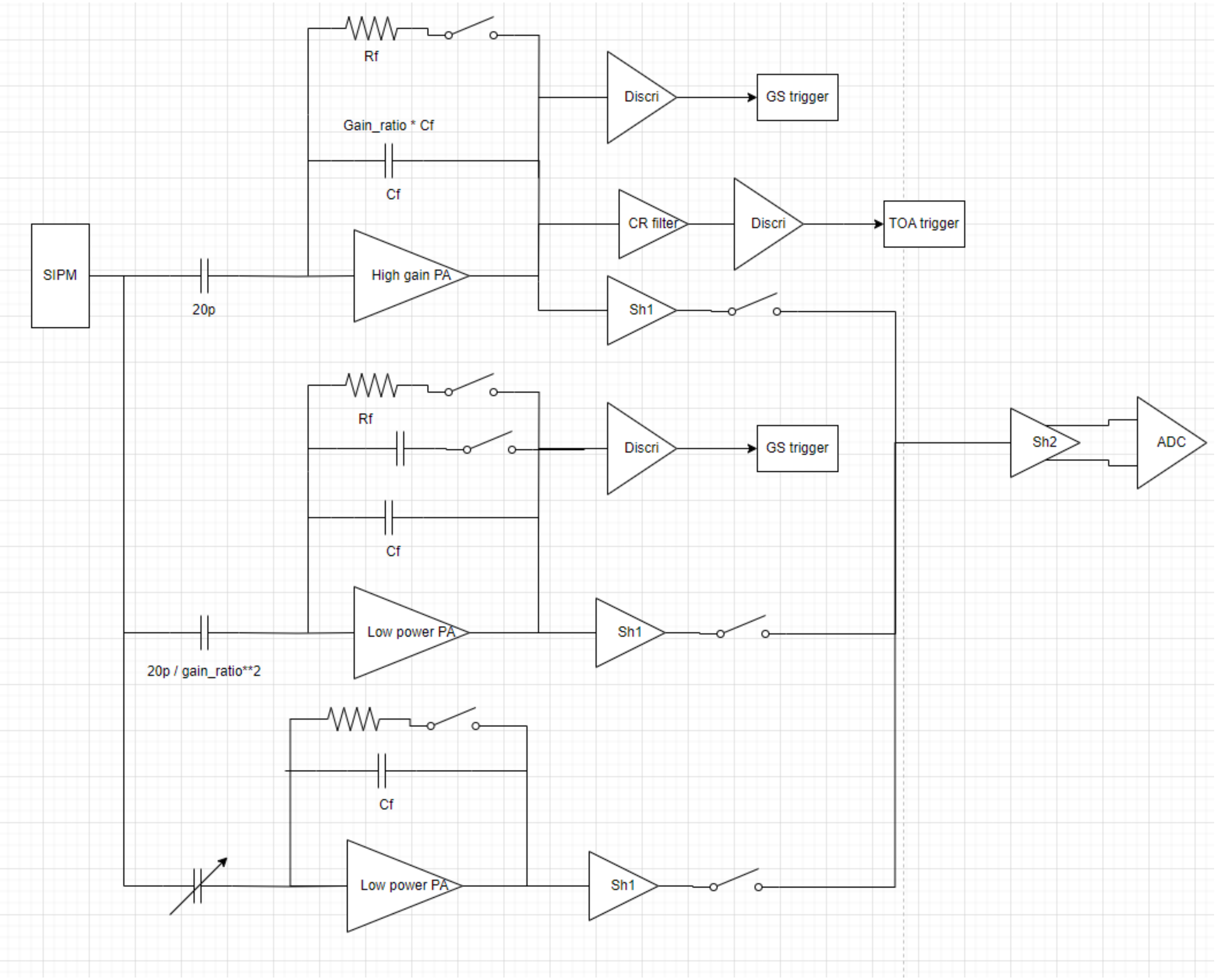




- CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 → https://doi.org/10.1088/1748-0221/19/04/C04005

# CALOROC1B: Chosen architecture

- New dynamic frontend with switched gain:
  - High gain
  - 2x medium gain
  - Low Gain
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10-15 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



# CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

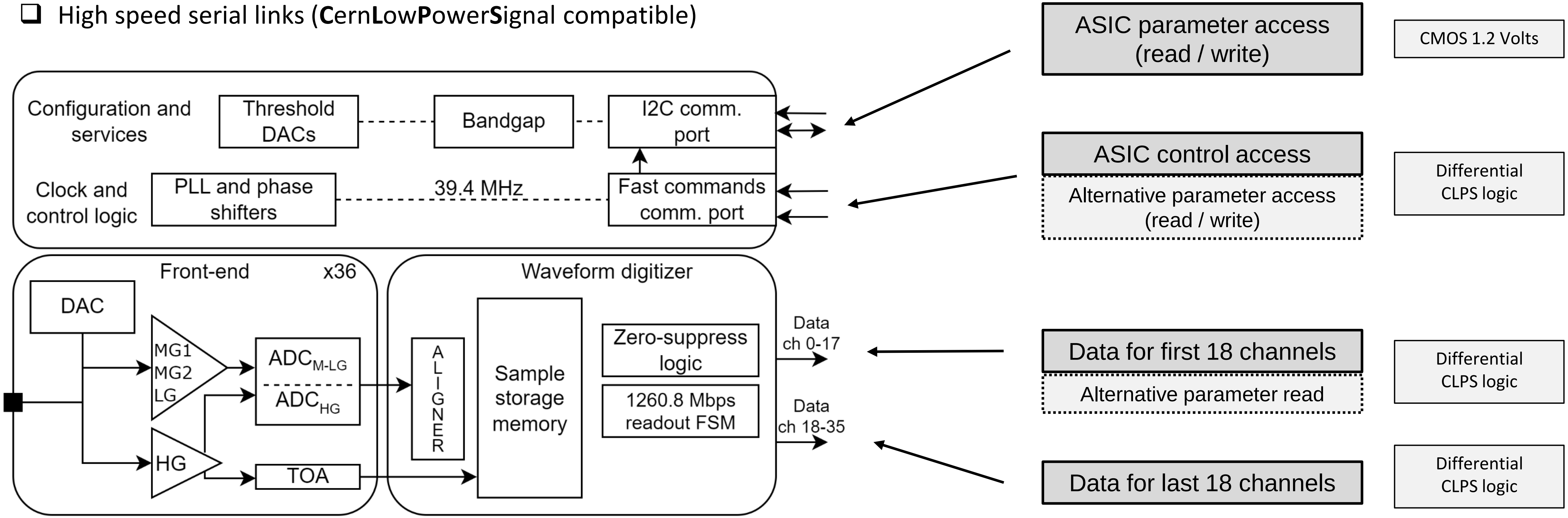
- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

| Operation modes | 1 SiPM of 530pF Caloroc1B | 1 SiPM of 2.5nF Caloroc1B | 4 SiPM of 2.5nF Caloroc1B | 1 SiPM of 530pF Caloroc1A |
|---|---|---|---|---|
| Cin | 530pF | 2.5nF | 10nF | 560pF |
| Dynamic range in charge (Noise - Max) | 2.6fC-190pC | 12fC-770pC | 48fC-3.1nC | 20fC-320pC |
| Input time constant (occupancy related) | 100ns | 500ns | 500ns | 10ns |
| Jitter @ MIP (≈400fC) | 35ps | 110ps | 470ps | 400ps |
| SNR @ 1p.e (≈30fC@gain=1.8e5) | 10 | 2.4 | 0.6 | 1.44 |

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

# CALOROCs: block diagram and interfaces

- CALOROCs will have the same interfaces (comparable to CMS ones):
  - 1 clock @ 315,2 MHz + 2 resets (hard + soft)
  - Fast command to dynamically control the ASIC (differential)
  - I2C to set the parameters (tbc)
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)



# CALOROC fast commands

- Commands to interact dynamically with the ASIC
  - 8 bits commands synchronized with incoming 315,2 MHz clock – MSB first
  - Only Idle really needed – others have a known latency
  - Detailed in the datasheet

| Fast commands | Value | Description |
|---|---|---|
| Idle | 00110110 | Default command inside |
| ChipSync | 11010010 | Reset FSM, buffers and counters |
| BCR | 00011101 | Reset timestamp counter to a default value |
| EBR | 11010001 | Empty readout buffers |
| LinkResetROCD | 10011010 | Transmission of synchronization patterns |
| ROC-Serializer-Reset | 10011100 | Reset serializer link module only |
| L1A | 01001011 | External trigger (all channels) |
| CalPulseInt | 00101101 | 800 ns internal calibration pulse |
| CalPulseExt | 01111000 | 100 ns external calibration pulse |
| SC_0 | 01011010 | Send bit 0 to SLIM |
| SC_1 | 01011100 | Send bit 1 to SLIM |
| SC_Valid_Reset | 10001011 | Send validation to SLIM or<br>a reset transaction (2 consecutives) |

Idle → Default command

ChipSync, BCR, EBR → Resets and synchronization

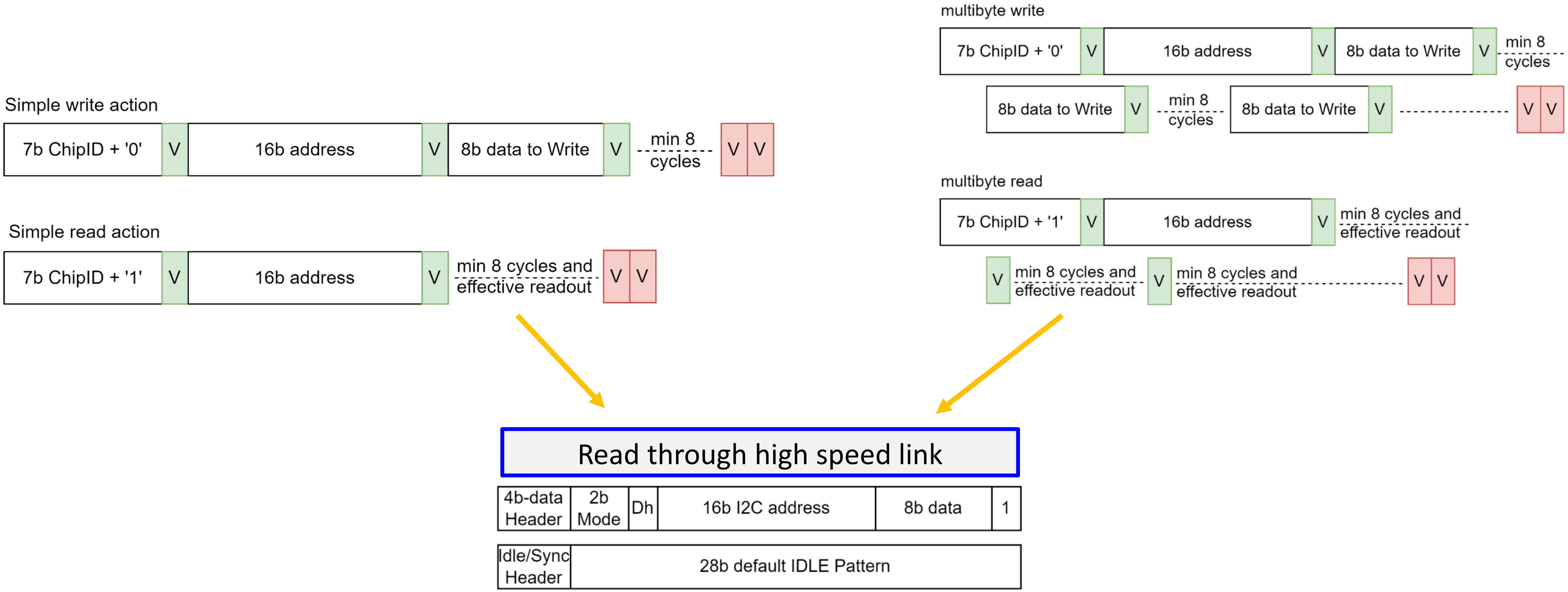
LinkResetROCD, ROC-Serializer-Reset → Serial links recovery

L1A, CalPulseInt, CalPulseExt → Calibration and pseudo-heartbeat

SC_0, SC_1, SC_Valid_Reset → Slow control (I2C) over fast commands

# Slow control – parameter access through fast command

- New feature to read/write parameter through fast command
  - I2C is still the default way to access ASIC parameters
  - Uses 3 dedicated fast command to “recreate” I2C frames
  - Main advantages: x40 speed + use existing serial links
  - Detailed in the datasheet



# Slow control – parameter access through I2C

- Use existing CERN module (used in ALTIROC)
  - I2C is the default way to access parameters
  - Max 1 MHz speed and 30 address available (+1 broadcast)
  - Detailed in the datasheet

S / P: START and STOP condition of a standard I2C protocol
CHIP ADDR: 7-bit chip address (MSB must be set to 1)
SUB-ADR [15:8]: sub-block (cluster) number (from 0 to 255)
SUB_ADR [7:8]: register number (from 0 to 31) – not used bits must be set to 0
DATA[7:0]: data to be written in the parameter
A: Acknowledge bit

**Default write**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | CHIP ADR | W | A | SUB-ADR [15:8] | A | SUB-ADR [7:0] | A | DATA$_{ADR}$ [7:0] | A | P | |

**Default read**

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | CHIP ADR | W | A | SUB-ADR [15:8] | A | SUB-ADR [7:0] | A | RS | CHIP ADR | R | A | … | |

| | | | | |
|---|---|---|---|---|
| … | DATA$_{ADR}$ [7:0] | A | P | |

**Multibyte write**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | CHIP ADR | W | A | SUB-ADR [15:8] | A | SUB-ADR [7:0] | A | DATA$_{ADR}$ [7:0] | A | … |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| … | DATA$_{ADR+1}$ [7:0] | A | DATA$_{ADR+2}$ [7:0] | A | DATA$_{ADR+3}$ [7:0] | A | DATA$_{ADR+4}$ [7:0] | A | … | P |

**Multibyte read**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | CHIP ADR | W | A | SUB-ADR [15:8] | A | SUB-ADR [7:0] | A | RS | CHIP ADR | R | A | … |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| … | DATA$_{ADR}$ [7:0] | A | DATA$_{ADR+1}$ [7:0] | A | DATA$_{ADR+2}$ [7:0] | A | DATA$_{ADR+3}$ [7:0] | A | … | P |

# EIC: CALOROC readout frames

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

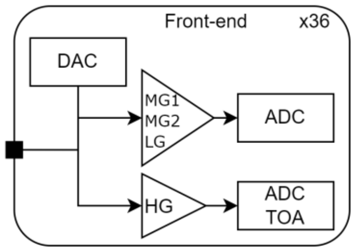
## CALOROCA (CMS-like)

| | | | | | |
|---|---|---|---|---|---|
| 4b-data Header | 2b Mode | Dh | 24b Timestamp | | 1 |
| 4b-data Header | 8b 0 | Dh -d | Dh -h | 18 channels Hit map | |
| Tc | Tp | 10b ADC-1 | 10b ADC or TOT (Tc = 1) | 10b TOA | |
| Tc | Tp | 10b ADC-1 | 10b ADC or TOT | 10b TOA | |
| ⋮ | | | | | |
| Tc | Tp | 10b ADC-1 | 10b ADC or TOT | 10b TOA | |
| CRC | | | | | |
| Idle/Sync Header | 28b default IDLE Pattern | | | | |

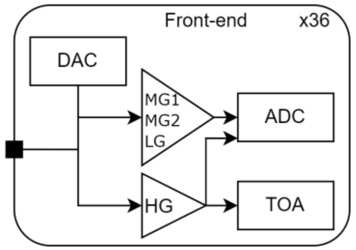
## CALOROCB – 2 ADCs or 1 ADC (4 gains)

| | | | | | |
|---|---|---|---|---|---|
| 4b-data Header | 2b Mode | Dh | 24b Timestamp | | 1 |
| 4b-data Header | 8b 0 | Dh -d | Dh -h | 18 channels Hit map | |
| 2b Gain | 10b ADC - HG or 0s | 10b ADC 3-gain or 4-gain | 10b TOA | | |
| 2b Gain | 10b ADC - HG or 0s | 10b ADC 3-gain or 4-gain | 10b TOA | | |
| ⋮ | | | | | |
| 2b Gain | 10b ADC - HG or 0s | 10b ADC 3-gain or 4-gain | 10b TOA | | |
| CRC | | | | | |
| Idle/Sync Header | 28b default IDLE Pattern | | | | |

## CALOROCB (2 ADCs)

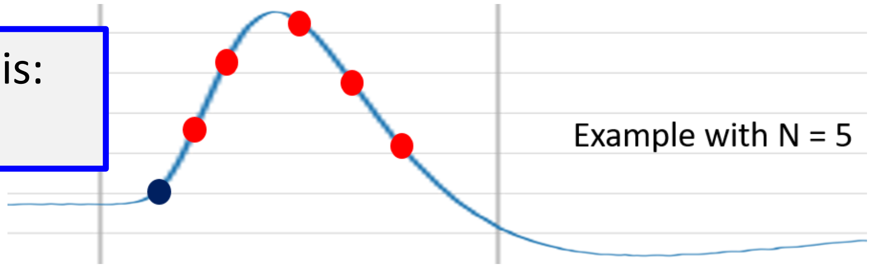



## CALOROCB (1 ADCs)




In ZS mode, for **X** (1-18) hit channels and **N** samples, number of 32-bit words is:

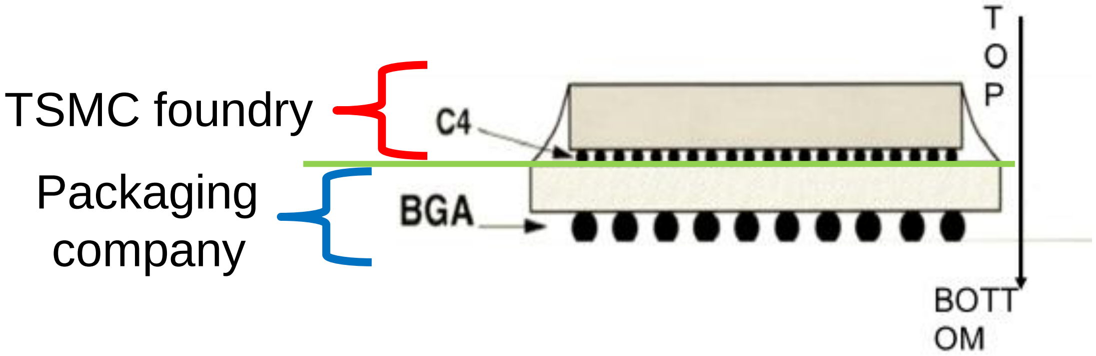
**N** x ( 2Headers + **X** + 2Trailers )




In characterization mode, forced TcTp, ADC, TOT, TOA for all channels

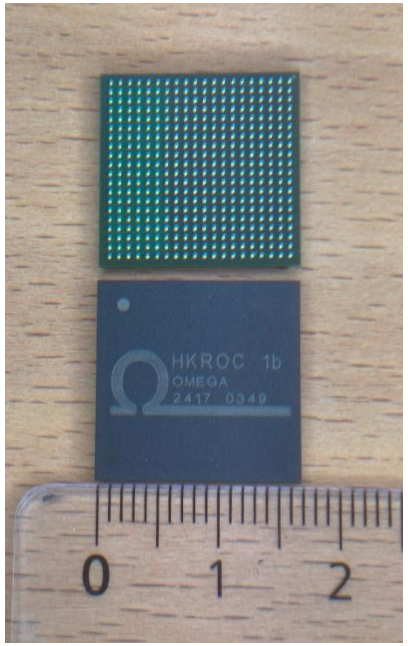
# CALOROC (A or B) packaging

- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0,8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3




| JEDEC SOLID STATE PRODUCT OUTLINE | TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES | ISSUE: E | DATE: AUG 2003 | MO-216 |
|---|---|---|---|---|

| TABLE 3: SQUARE VARIATIONS – 0.80 PITCH | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| D / E | e = 0.80 | | | | | | | |
| | MD/ME | N | SD/SE | VARIATION | MD–1/ME–1 | N | SD/SE | VARIATION |
| 14.00 | 17 | 289 | 0.00 | BAJ–1 | 16 | 256 | 0.40 | BAJ–2 |
| 15.00 | 18 | 324 | 0.40 | BAK–1 | 17 | 289 | 0.00 | BAK–2 |
| 16.00 | 19 | 361 | 0.00 | BAL–1 | 18 | 324 | 0.40 | BAL–2 |
| 17.00 | 20 | 400 | 0.40 | BAM–1 | 19 | 361 | 0.00 | BAM–2 |



# CALOROC packaging – pinout overview

- CALOROC will have the same package as existing HKROC:
  - ~10 signals needed ton control CALOROC (4 diff + 6 single)
  - Around 350 pins for power/static/bias
  - Detailed in the datasheet

| Pin type | # balls (variant) |
|---|---|
| GND | 175 |
| VDD | 102 |
| BIAS / static / debug | 37 (-2+0) |
| Not connected | 36 (-0+2) |
| Analog inputs | 36 |
| Controls | 14 (-2+2) |


MAPPING CALOROC_1 BGA 400 (TOP VIEW)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDA | RSTB_I2C | HARD_RSTB | SOFT_RSTB | ERROR | CK_320_N | CK_320_P | FCMD_P | FCMD_N | ADD<4> | CHIP_R | AGND | AVDD | AGND | AGND | AGND | AGND | AGND | AGND | AGND |
| SCL | GND | GND | GND | GND | GND | VHI10<0> | VHI10<1> | FLAG_AF | ADD<4> | VREF_ADC | AGND | AVDD | AGND | IN<0> | AGND | IN<1> | AGND | NC | VDDA_PAD |
| DAC_ALDO | GND | GND | GND | GND | GND | NC | NC | FLAG_AF | NC | VCM_ADC | AGND | AVDD | AGND | IN<2> | AGND | IN<3> | AGND | NC | VDDA_PAD |
| NC | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<4> | AGND | IN<5> | AGND | NC | VDDA_PAD |
| NC | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<6> | AGND | IN<7> | AGND | NC | VDDA_PAD |
| OUT_TSPFF | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<8> | AGND | IN<9> | AGND | AGND | AGND |
| SIPM_CALIB | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<10> | AGND | IN<11> | AGND | NC | VREF_SK_LP |
| NC | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<12> | AGND | IN<13> | AGND | AGND | AGND |
| STROBE_EXT | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<14> | AGND | IN<15> | AGND | NC | VREF_NOINV_SK |
| EFUSE | NC | GND | DVDD | VDD_PLL | VDD_PLL | AGND_PLL | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<16> | AGND | IN<17> | AGND | NC | VREFINV_VBM3PA |
| TRIG_P | NC | GND | DVDD | VDD_SC | VDD_SC | AGND_PLL | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<18> | AGND | IN<19> | AGND | NC | VREFTOA_VBIPA |
| TRIG_N | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<20> | AGND | IN<21> | AGND | NC | VREFTOT_VBMPA |
| DAQ2_P | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<22> | AGND | IN<23> | AGND | NC | VBG_1V |
| DAQ2_N | PLL_LOCK | GND | DVDD | VDD_SC | VDD_SC | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<24> | AGND | IN<25> | AGND | NC | PROBEPA_VBOPA |
| DAQ3_P | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<26> | AGND | IN<27> | AGND | NC | INCTEST |
| DAQ3_N | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<28> | AGND | IN<29> | AGND | NC | VDDA_PAD |
| ADD<3> | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<30> | AGND | IN<31> | AGND | NC | VDDA_PAD |
| ADD<2> | GND | GND | GND | GND | GND | NC | NC | NC | NC | VCM_ADC | AGND | AVDD | AGND | IN<32> | AGND | IN<33> | AGND | NC | VDDA_PAD |
| ADD<1> | GND | GND | GND | GND | GND | NC | VHI10<2> | NC | NC | VREF_ADC | AGND | AVDD | AGND | IN<34> | AGND | IN<35> | AGND | NC | VDDA_PAD |
| ADD<0> | PROBE_TOT_PA | PROBE_TOA | PROBE_DC2 | PROBE_DC1 | PROBE_INV | VNEG | VHI10<3> | PROBE_NOINV | TRIG2_EXT | TRIG1_EXT | AGND | AVDD | AGND | AGND | AGND | AGND | AGND | AGND | AGND |

# CALOROC integration and power supply consideration

- On the board, CALOROC will need a maximum of 3 power supplies:
  - Analog / Digital + 1 dedicated for CALOROC-A (Preamp)
  - (Not shown here: LED power and HV)

Digital side | Analog side

MAPPING CALOROC_1 BGA 400 (TOP VIEW)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | [illegible] | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDA | RSTB_I2C | HARD_RSTB | SOFT_RSTB | ERROR | CK_320_N | CK_320_P | FCMD_P | FCMD_N | AD[illegible]4> | CHIP_R | AGND | AVDD | AGND | AGND | AGND | AGND | AGND | AGND | AGND |
| SCL | GND | GND | GND | GND | GND | VHI10<0> | VHI10<1> | FLAG_AF | ADD<4> | VREF_ADC | AGND | AVDD | AGND | IN<0> | AGND | IN<1> | AGND | NC | VDDA_PAD |
| DAC_ALDO | GND | GND | GND | GND | GND | NC | NC | FLAG_AF | [illegible] | VCM_ADC | AGND | AVDD | AGND | IN<2> | AGND | IN<3> | AGND | NC | VDDA_PAD |
| NC | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<4> | AGND | IN<5> | AGND | NC | VDDA_PAD |
| NC | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<6> | AGND | IN<7> | AGND | NC | VDDA_PAD |
| OUT_TSPFF | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<8> | AGND | IN<9> | AGND | AGND | AGND |
| SIPM_CALIB | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<10> | AGND | IN<11> | AGND | NC | VREF_SK_LP |
| NC | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<12> | AGND | IN<13> | AGND | AGND | AGND |
| STROBE_EXT | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<14> | AGND | IN<15> | AGND | NC | VREF_NOINV_SK |
| EFUSE | NC | GND | DVDD | VDD_PLL | VDD_PLL | AGND_PLL | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<16> | AGND | IN<17> | AGND | NC | VREFINV_VBM3PA |
| TRIG_P | NC | GND | DVDD | VDD_SC | VDD_SC | AGND_PLL | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<18> | AGND | IN<19> | AGND | NC | VREFTOA_VBIPA |
| TRIG_N | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<20> | AGND | IN<21> | AGND | NC | VREFTOT_VBMPA |
| DAQ2_P | NC | GND | DVDD | DVDD | DVDD | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<22> | AGND | IN<23> | AGND | NC | VBG_1V |
| DAQ2_N | PLL_LOCK | GND | DVDD | VDD_SC | VDD_SC | GND | GND | GND | AGND | AGND | AGND | AGND | AGND | IN<24> | AGND | IN<25> | AGND | NC | PROBEPA_VBOPA |
| DAQ3_P | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<26> | AGND | IN<27> | AGND | NC | INCTEST |
| DAQ3_N | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<28> | AGND | IN<29> | AGND | NC | VDDA_PAD |
| ADD<3> | GND | GND | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | AVDD | AVDD | AVDD | AGND | IN<30> | AGND | IN<31> | AGND | NC | VDDA_PAD |
| ADD<2> | GND | GND | GND | GND | GND | NC | NC | NC | [illegible] | VCM_ADC | AGND | AVDD | AGND | IN<32> | AGND | IN<33> | AGND | NC | VDDA_PAD |
| ADD<1> | GND | GND | GND | GND | GND | NC | VHI10<2> | NC | NC | VREF_ADC | AGND | AVDD | AGND | IN<34> | AGND | IN<35> | AGND | NC | VDDA_PAD |
| ADD<0> | PROBE_TOT_PA | PROBE_TOA | PROBE_DC2 | PROBE_DC1 | PROBE_INV | VNEG | VHI10<3> | PROBE_NOINV | TRIG[illegible]EXT | TRIG1_EXT | AGND | AVDD | AGND | AGND | AGND | AGND | AGND | AGND | AGND |

| GROUND BGA | ALIM BGA |
|---|---|
| AGND | AVDD |
| AGND | AVDD |
| AGND | AVDD |
| AGND | AVDD_PAD |
| AGND | AVDD_PAD |
| GND_PLL | VDD_PLL |
| GND | DVDD |
| GND | DVDD |
| GND | DVDD |
| GND | DVDD |
| GND | DVDD |
| | VDD_SC |

Analog side — Digital side — CALO-A (Preamp)

| Board power | Nominal value | ASIC power | Max ratings |
|---|---|---|---|
| Analog power | 1.2 Volts | AVDD, VDD_PLL | 8 mW / chn |
| Preamp power | 2.5 or 1.2 Volts (CALO-A or CALO-B) | AVDD_PAD | 2 mW / chn |
| Digital power | 1.2 Volts | DVDD | 5 mW / cnn |

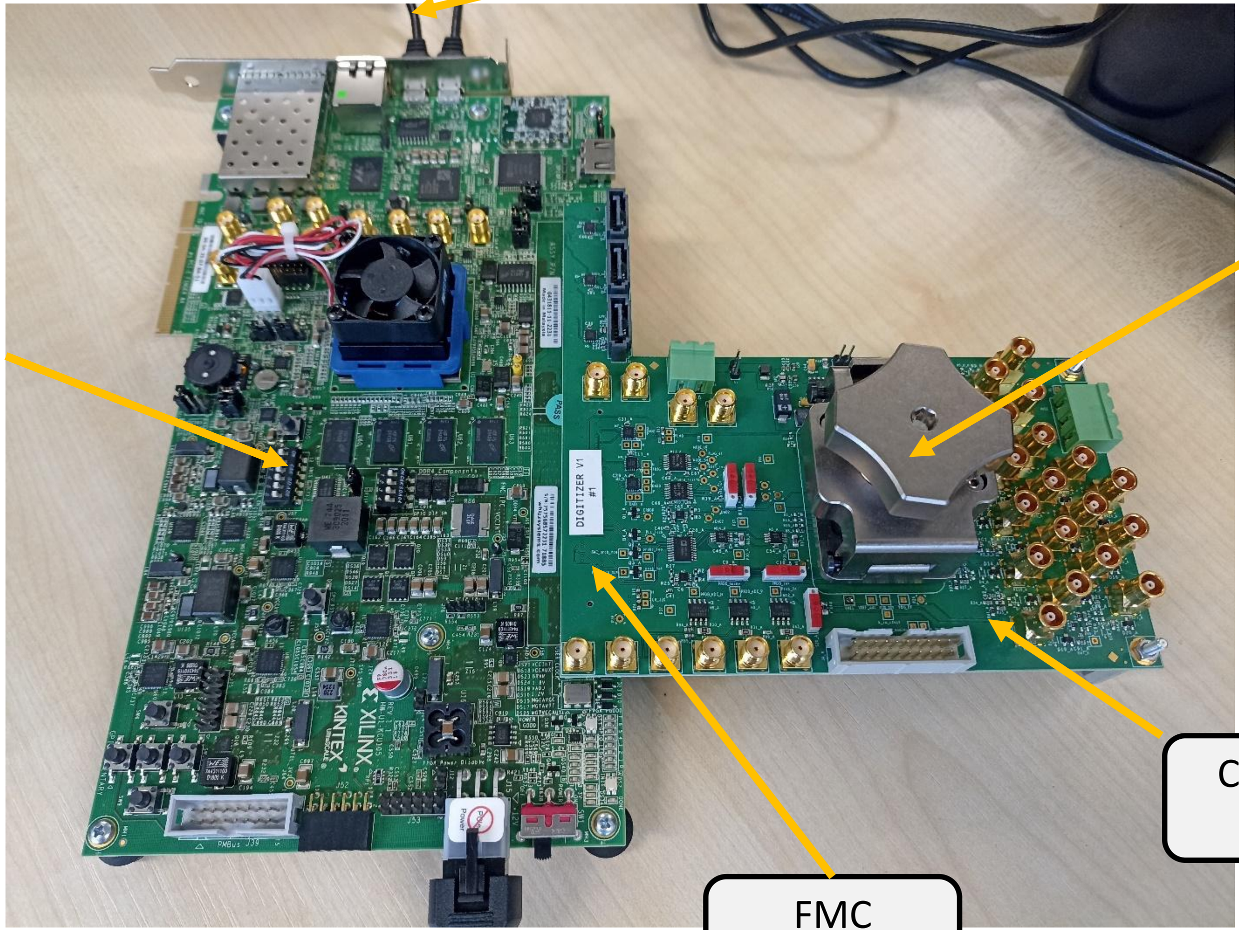
Values will be refined after first measurements

# Test system for characterization

- CALOROC characterization motherboard under design at OMEGA:
  - Originally developed for HGCROC and the HKROC
  - Well-known at OMEGA and LLR (firmware based only)
  - Compatible with KRIA motherboard (CERN) but software + firmware needed

Python scripts

Monitor Program Test

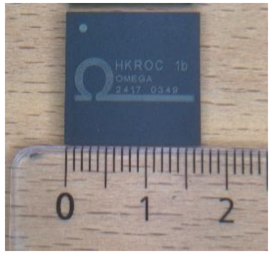


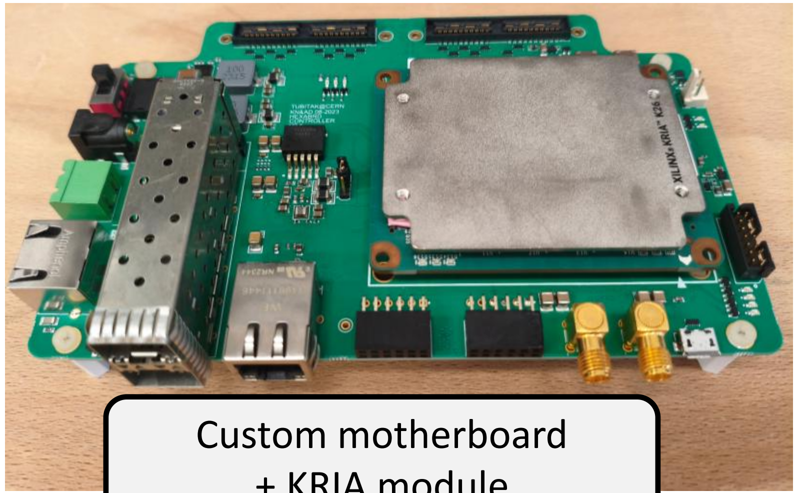
Commercial KCU105 board

CALOROC BGA socket

FMC connector

Custom CALOROC motherboard



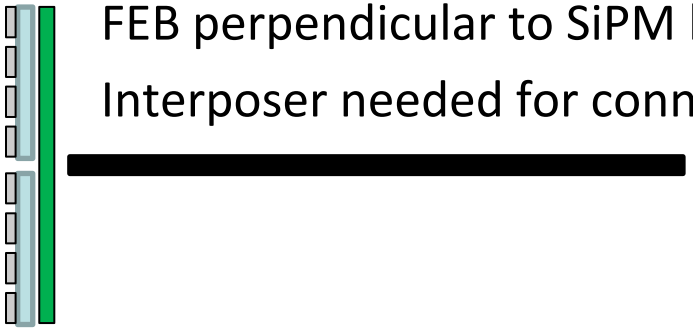
Custom motherboard + KRIA module

# CALOROC integration – preliminary studies (LLR IJCLAB OMEGA)

- Try to find an optimum between CALOROC and LpGBT for the integration
  - Driven by serial links @ 1,26 Gbps
  - CALOROC: 2 serial links for data output (1,26 Gbps)
  - LpGBT has max 7 inputs (1,26 Gbps)

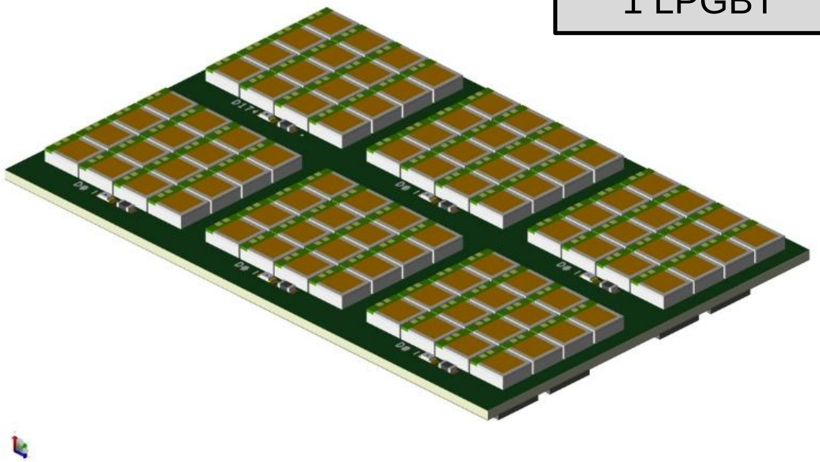
3 CALOROCs
+
1 LPGBT

Side view



FEB perpendicular to SiPM board

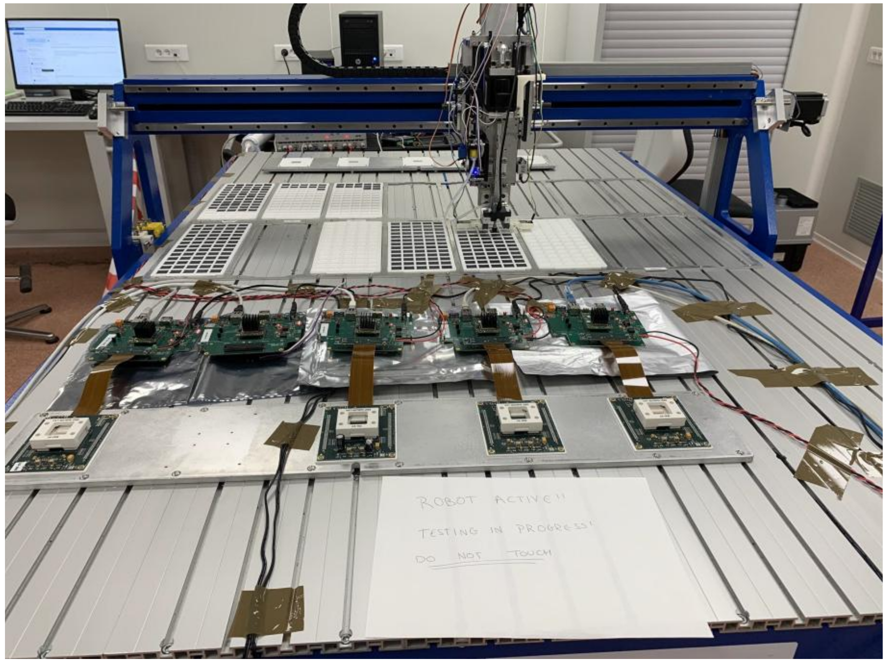
Interposer needed for connectors



| | | | |
|---|---|---|---|
| ASIC # (usage) | 1 (50%) | 1 (100%) | **3** (100%) |
| FEB width | 18 mm | 38 mm | 38 or 58 mm |
| FEB length | ~ not constrained | ~ not constrained | ~ not constrained |
| LpGBT # (usage) | 1 (15%) | 1 (30%) | **1** (100%) |
| Remarks | Need smaller package ? | | optimum |

# Quality assurance and timeline

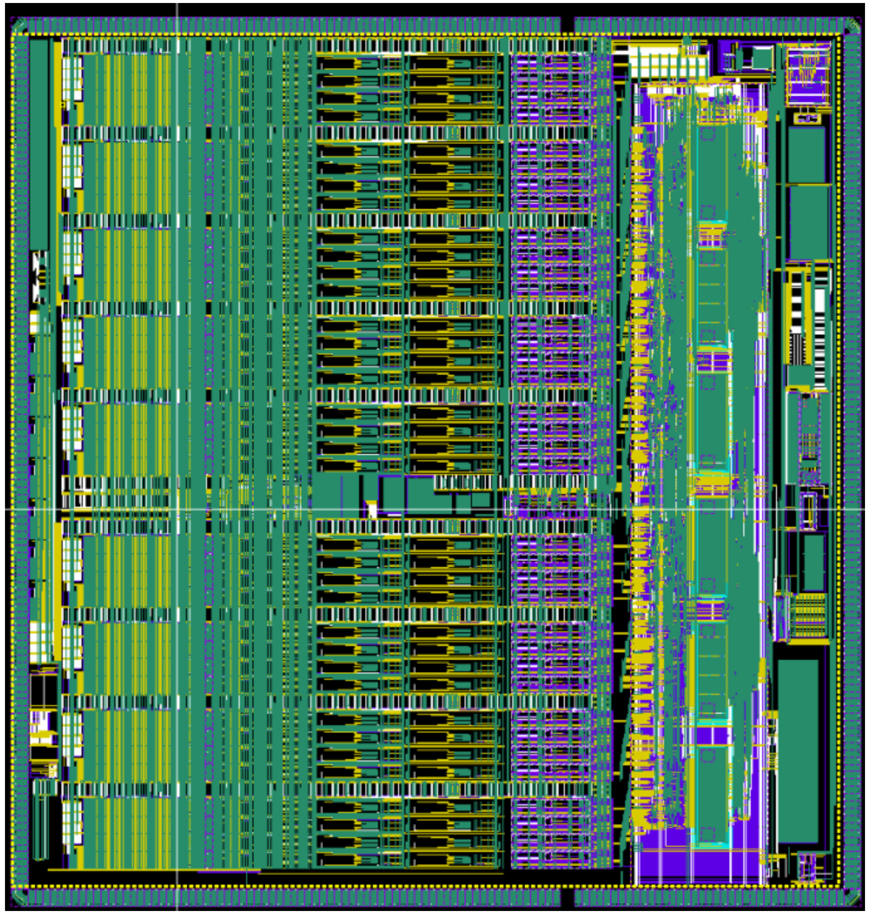
- Expertise in radiation-hardened front-end ASICs for HEP
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL ($10^5$ ASICs)
- Expertise in irradiation testing (dose and displacement)
  - HL-LHC levels 200 Mrad and $10^{16}$ $n_{eq}$ / cm² (1 MeV equivalent neutrons)
- Standard interfaces ensures a full compatibility with our robot
  - 2x 50 ASICs tested per hour (H2GCROC) with QR code scan
- CALOROC timeline – 2025 to 2028
  - Now: submission process start - CALOROCs submission (Eng. Run)
  - Oct 2025: first packaged ASICs back to the lab
    - 2 months to have an overall view of the performances
    - + 6 months for a deeper characterization
  - 2026-2027, irradiation campaigns
  - 2026: Decision for the final number of channels
  - Q1 2027: final submission (same channel count) + 2028 production
    - Schedule need to be refined if channels are doubled





# Conclusion

- Conservative **CALOROC-1A**:
  - Based on CMS SiPM H2GCROC with EIC readout
- New **CALOROC-1B**:
  - New analog front end
  - Higher dynamic range and input capacitance
  - Same backend (and pinout)
- **CALOROC1C** for Si/LAr detectors:
  - Based on CMS Si HGCROC with EIC readout
- All CALOROCs share the same backend + RadHard
  - We **~150 ASICs per each flavor**
  - GIT for back-end designers
  - Datasheet available soon
- Submission process started with IMEC (May 19)
  - Paperwork ongoing on CERN side in parallel of the submission

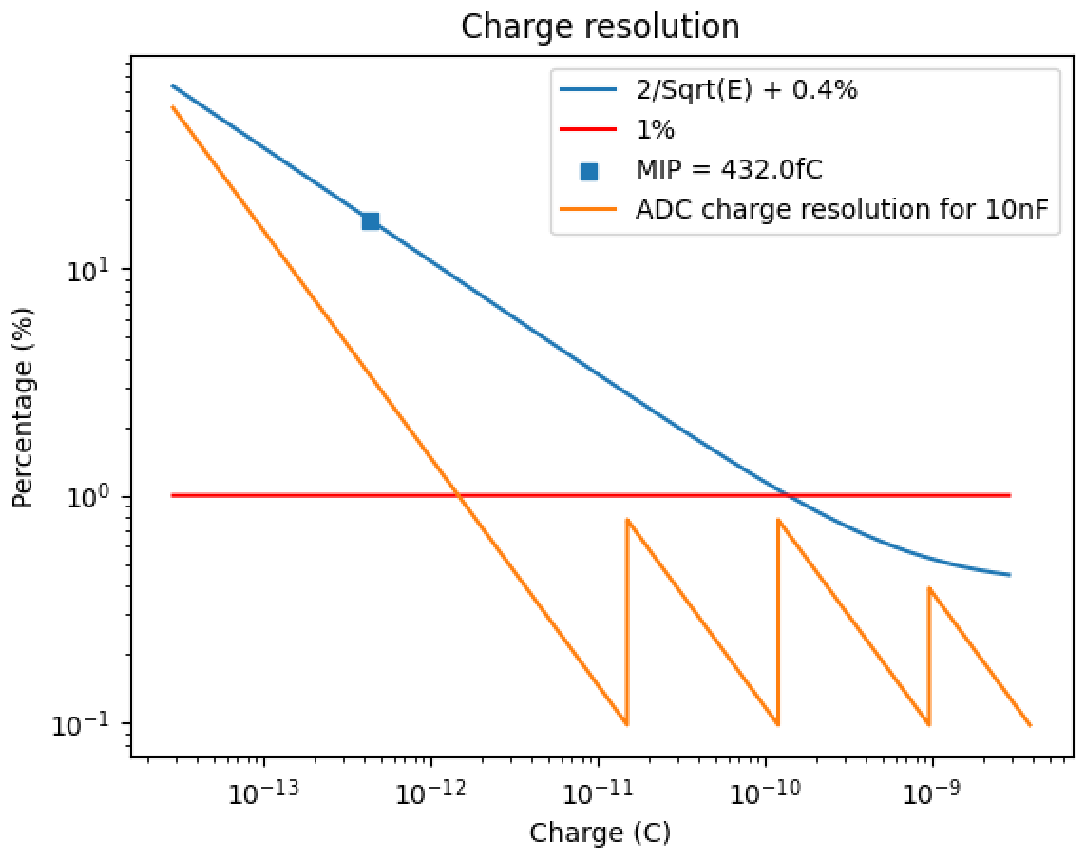


CALOROCs are targeted to include all features + radiation hardness on the first submission

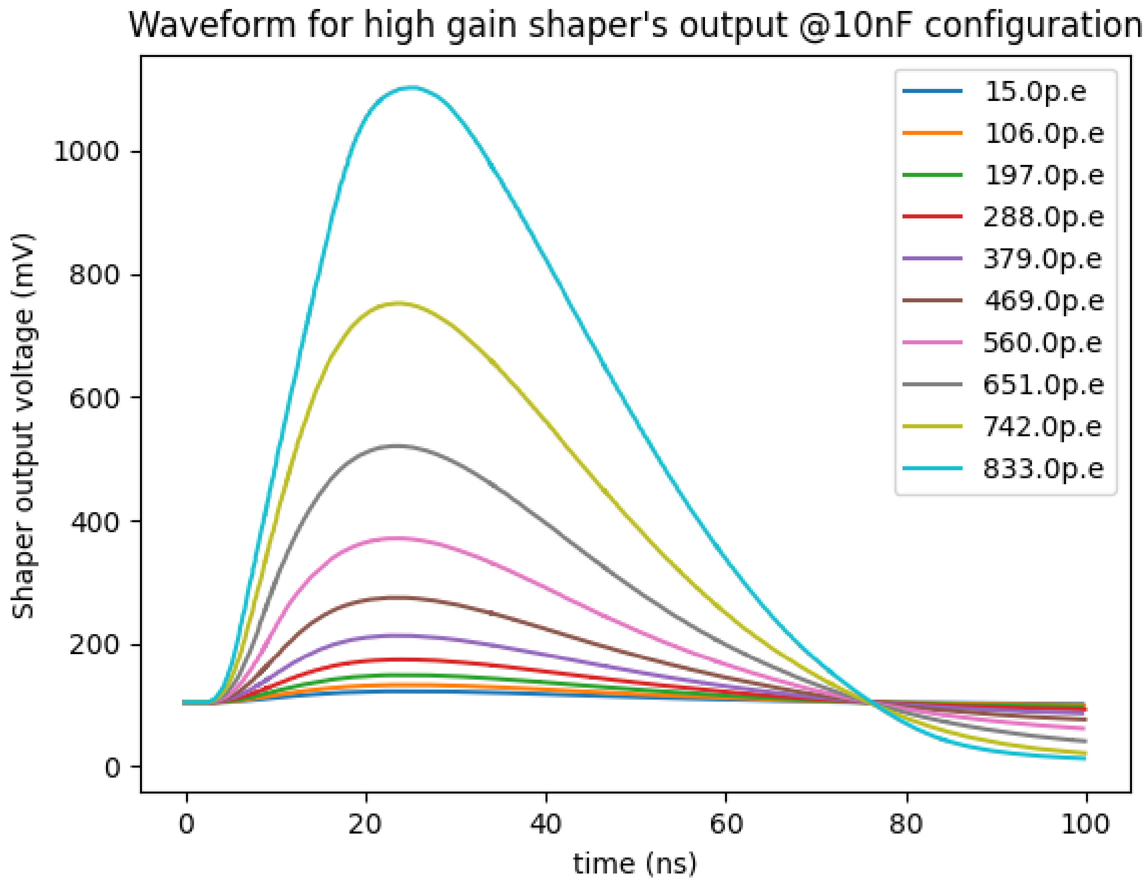
# Backup slides

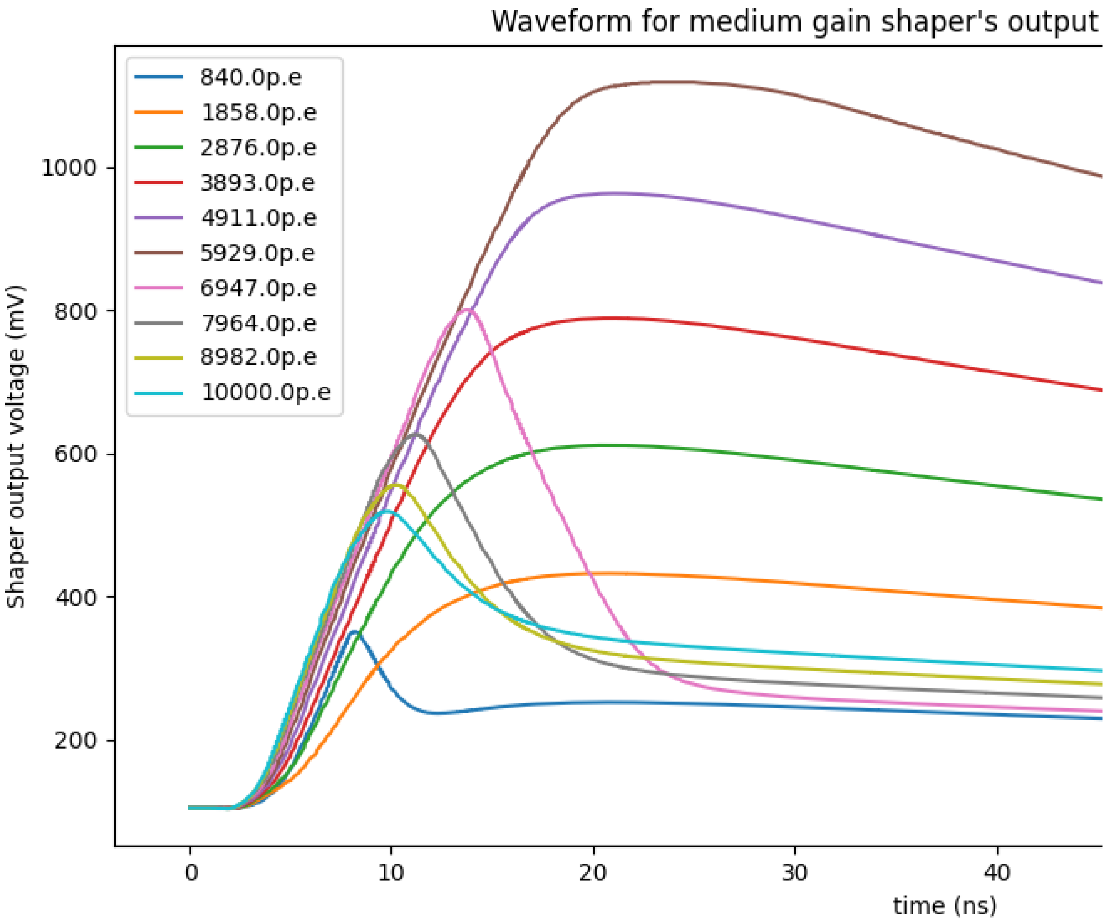
# CALOROC1B: Dynamic range and resolution

- The SiPM configuration has a direct impact on the dynamic range
  - The highest measurable charge is determined by the SiPM input capacitance.
  - The ratio between the highest and the lowest measurable charge is constant.
- 10b resolution and 16b dynamic range
  - With a 10b ADC and 4 gains (2b) we have a resolution of 16b
  - The measured charge is in the format of $10b \ast GainRatio^{2b}$
  - The gain ratio can be adjusted to increase the dynamic range in exchange for a lower resolution.
  - Using the highest resolution the dynamic range is 70k
  - Supposing 1MeV = 1p.e for the 4 SiPM setup this should give us a dynamic range of 1.5MeV (noise floor) to 100GeV

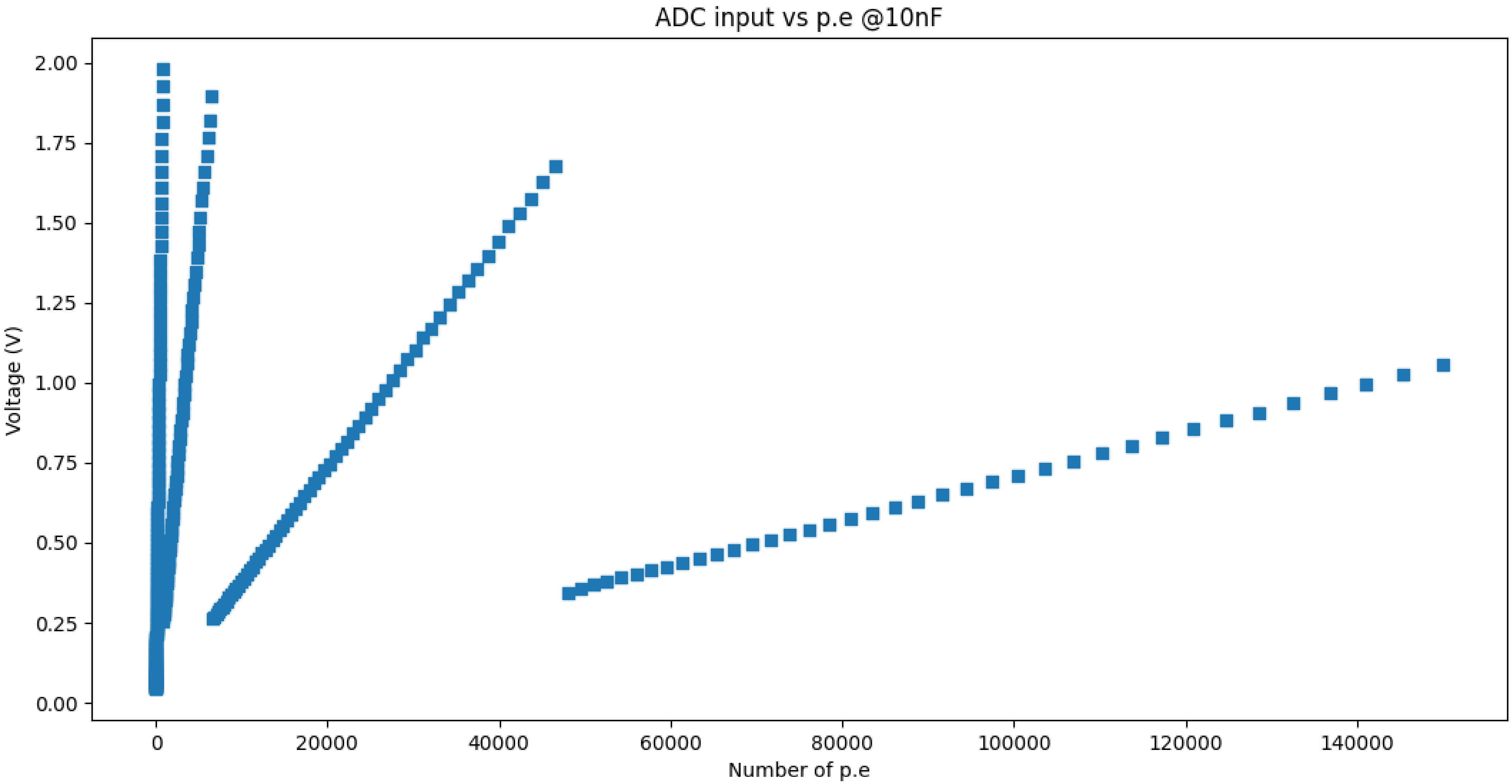


- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 10 nF



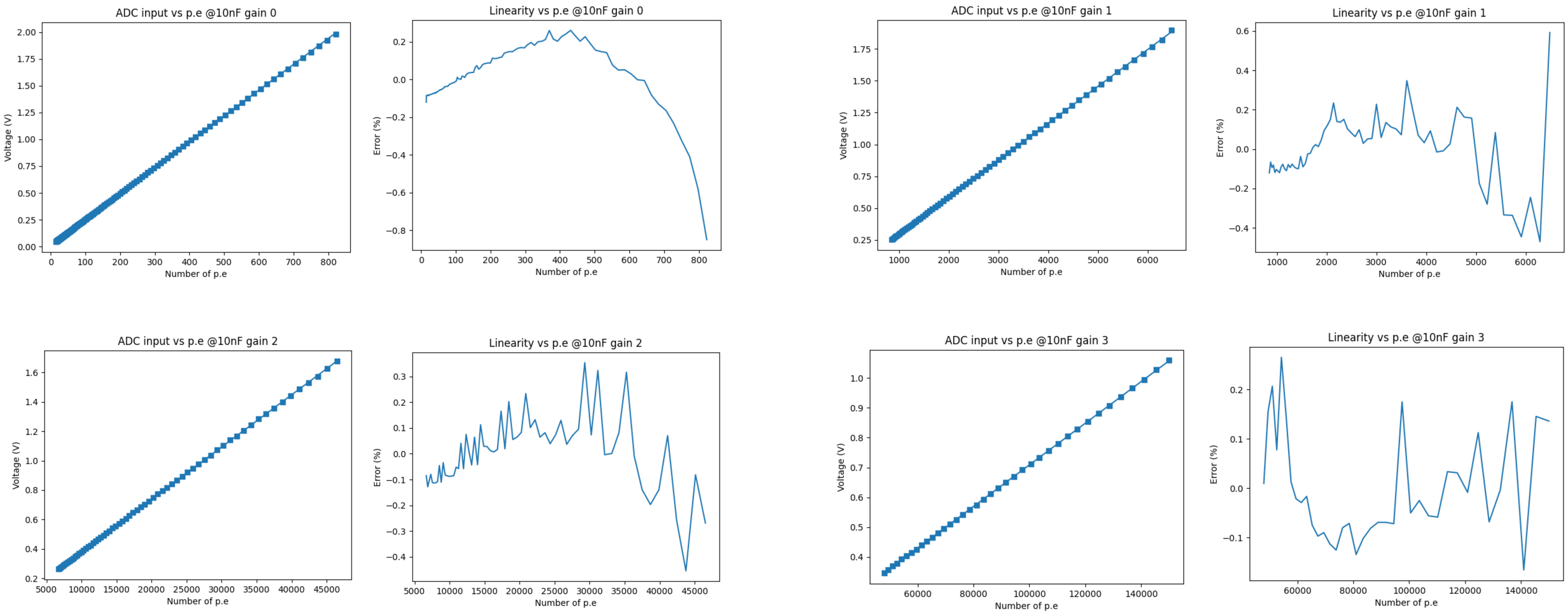



# CALOROC1B: Linearity



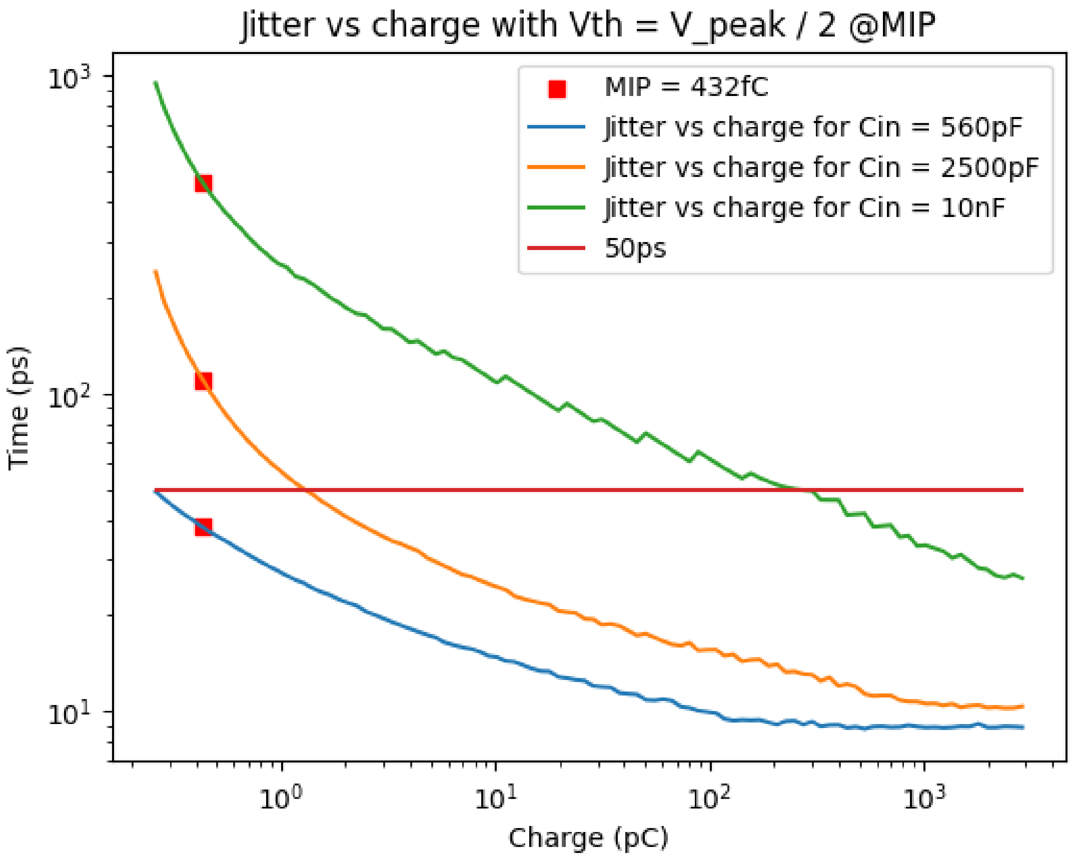
# CALOROC1B: Linearity error

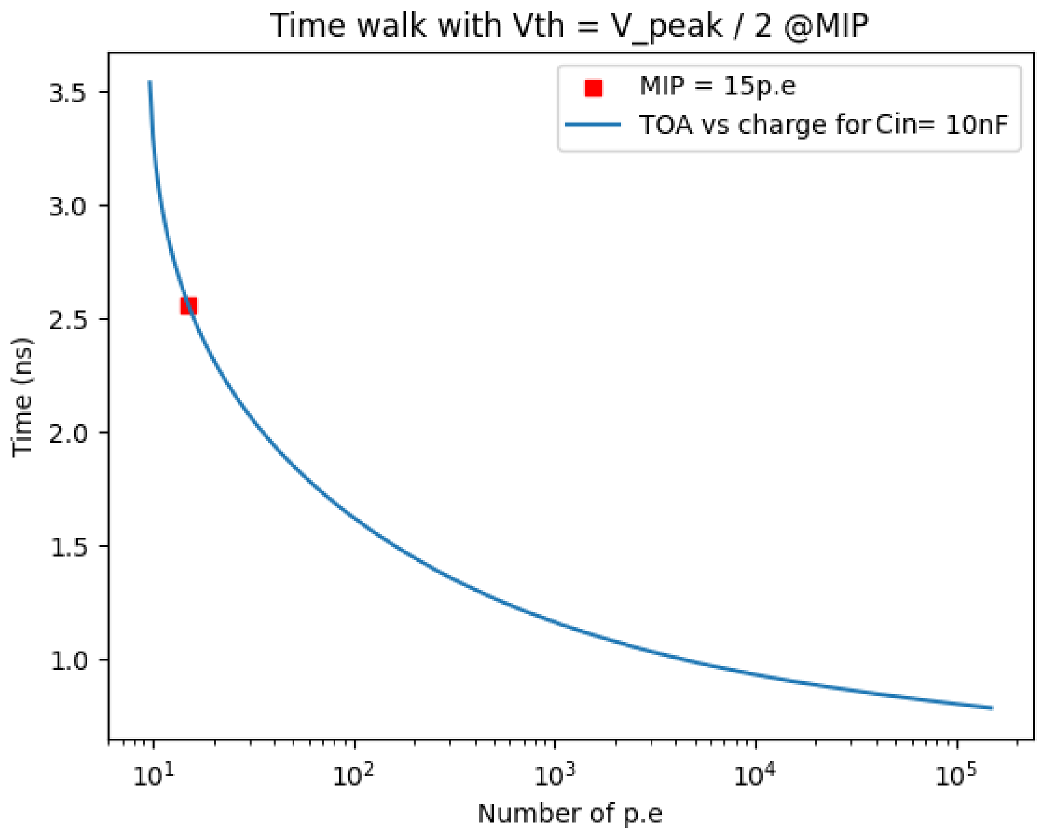
- Less than 1% linearity error



# CALOROC1B: Timing precision

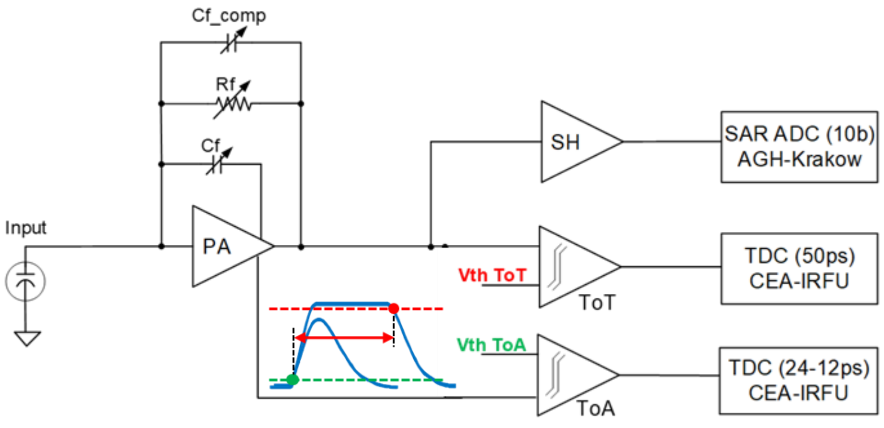
- Simulated time jitter goes down to 20 ps with < 500 ps for a MIP of 432fC @Cin=10nF
- Time walk is below ~2,5 ns

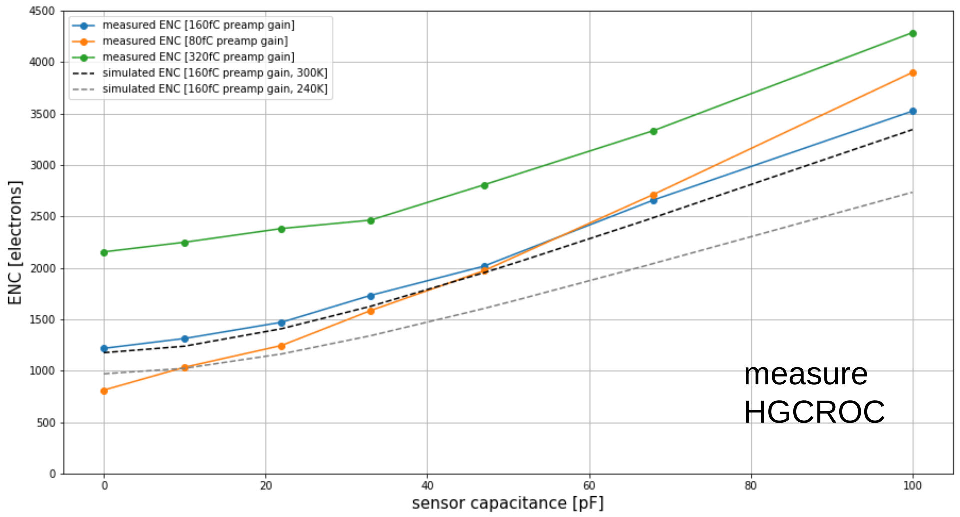


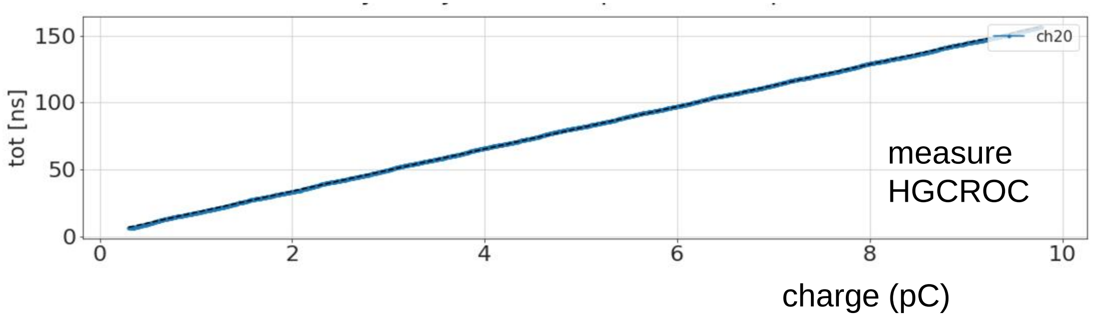



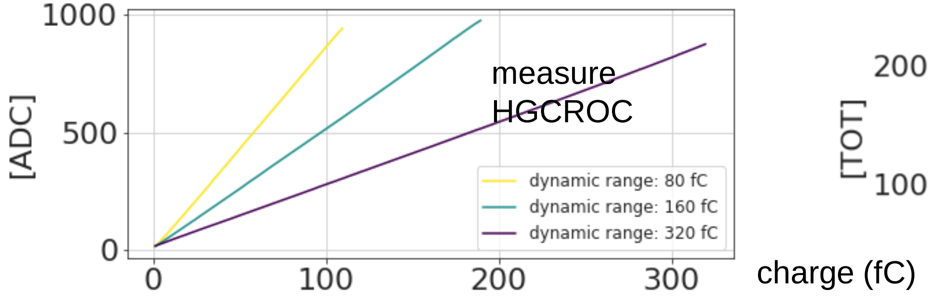
# CALOROC1C (based on HGCROC)

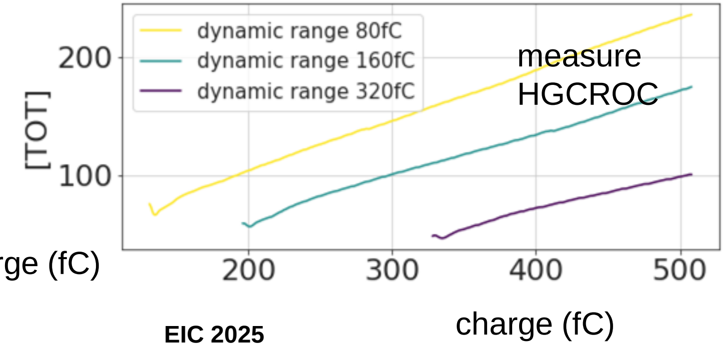
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / Si up to 100 pF

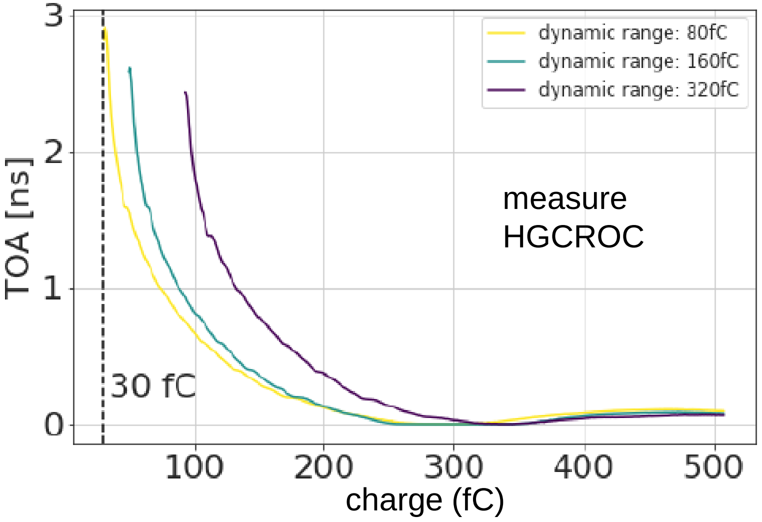



* TWEPP 2023 https://doi.org/10.1088/1748-0221/19/04/C04005

# CALOROC1C (based on HGCROC)

- CALOROC1C will
  - update its back-end (readout streaming)
  - slow down the shaping from 25ns to 100ns