

**EICROC status and plans
ePic ASIC review meeting
3 june 2025**

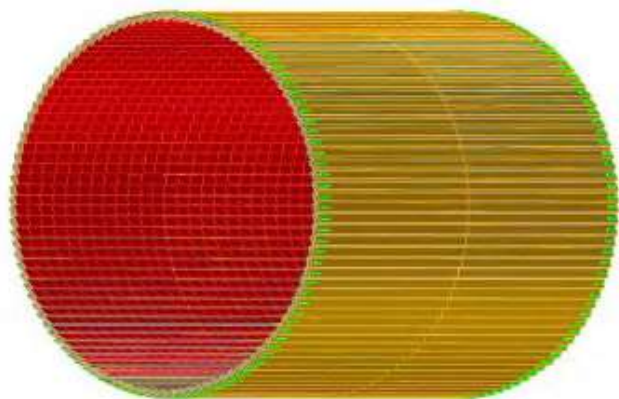
F. Bouyjou, S. Conforti, E. Delagnes, JJ Dormard, F. Dulucq, P. Dumas-Zielhman, M. El Berni, S. Extier, M. Firlej, T. Fiutowski, K. Guillosoy, F. Guilloux, M. Idzik, B.-Y. Ki, A. Laffite, C. de La Taille, O. LeDortz, J. Moron, D. Marchand, C. Munoz, M. Nguyen, N. Seguin-Moreau, L. Serin, A. Shama, A. Soulier, K. Swientek, D. Thienpont, A. Verplanck

ePIC AC-LGAD detectors

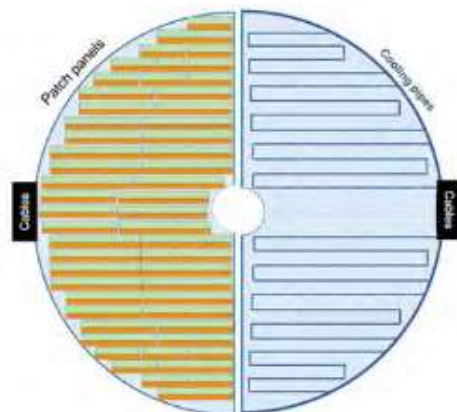


Specifications of ePIC AC-LGAD detectors:

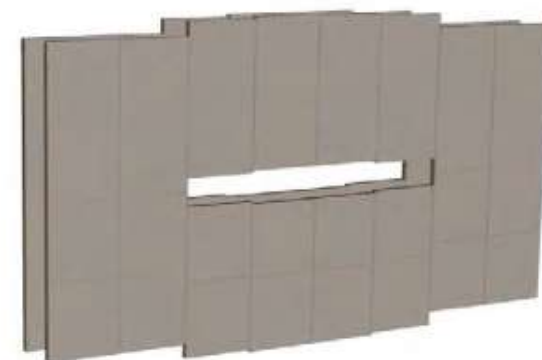
BToF



FToF



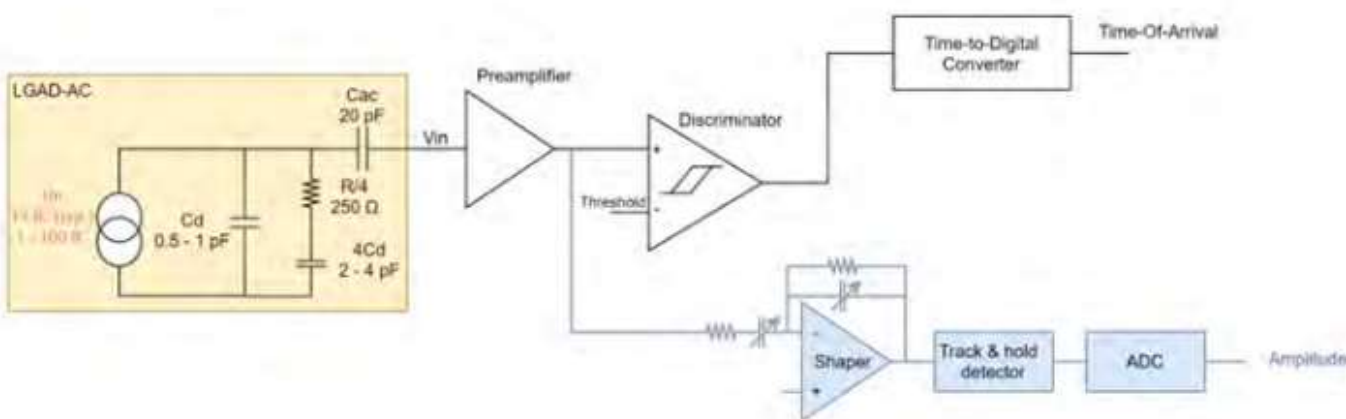
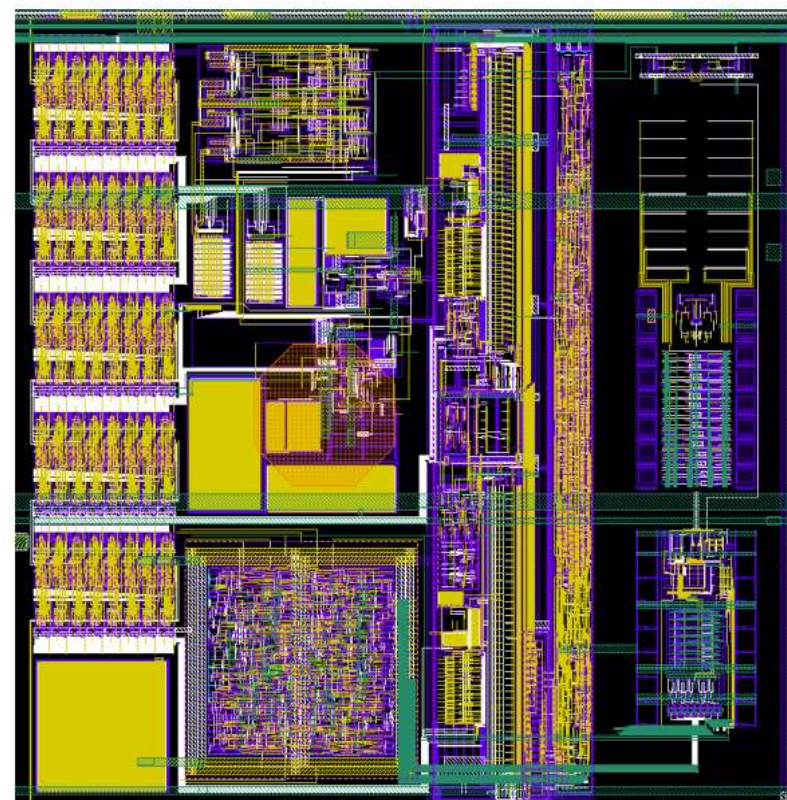
Roman Pots



4D Trackers

	Area (m ²)	Channel size (mm ²)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10 (strips)	2.4M	30 ps	30 μm in φ	0.01 X0
Forward TOF	2.22	0.5*0.5 (pixels)	8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5 (pixels)	0.28M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5 (pixels)	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

- Analog frontend similar to ATLAS ALTIROC
 - Cd = 1 pF (max 3 pF)
- **Need ADC instead of ToT** for charge measurement : 8bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- Simple digital readout but SEE-proof I²C slow control
- ~2 mW/pixel
- Fabricated in spring 2022 in TSMC 130nm

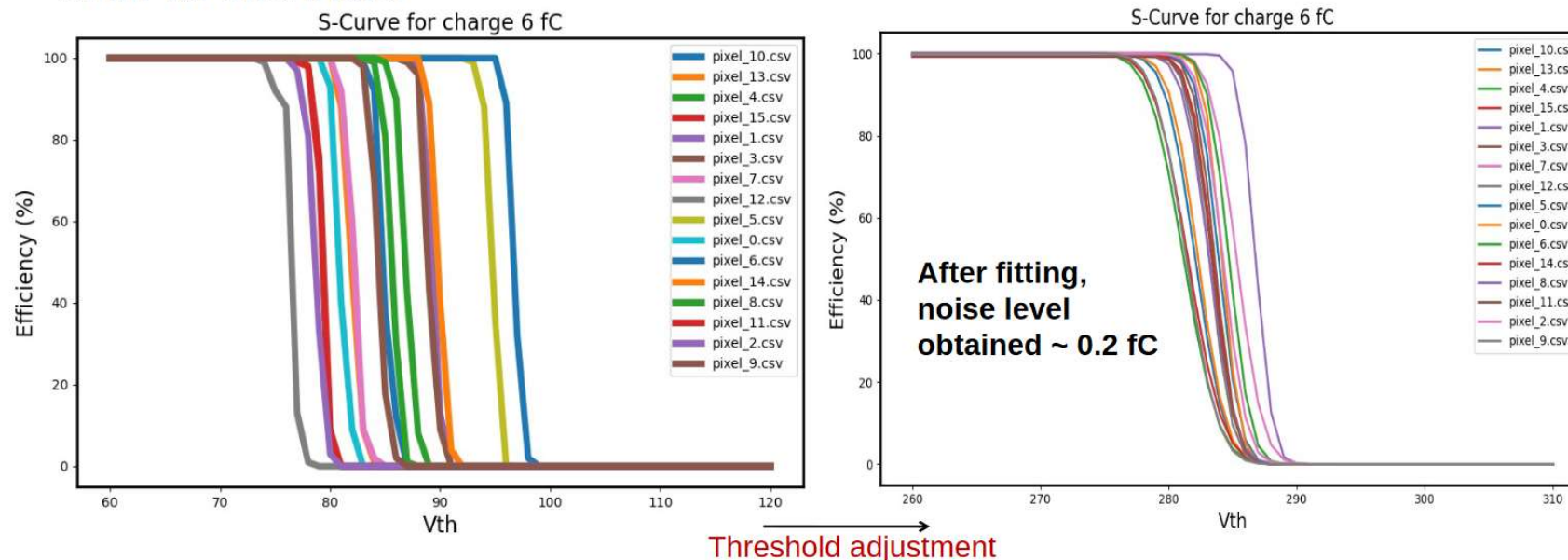


CdLT ePIC ASIC review 3 jun 2025

From A. Sharma : <https://indico.in2p3.fr/event/33456/contributions/144321>

S-curve (Efficiency vs threshold voltage)

- To correct the response of all channels towards the injected charge, discriminator threshold adjustment is done at a specific charge injection to align all channels.

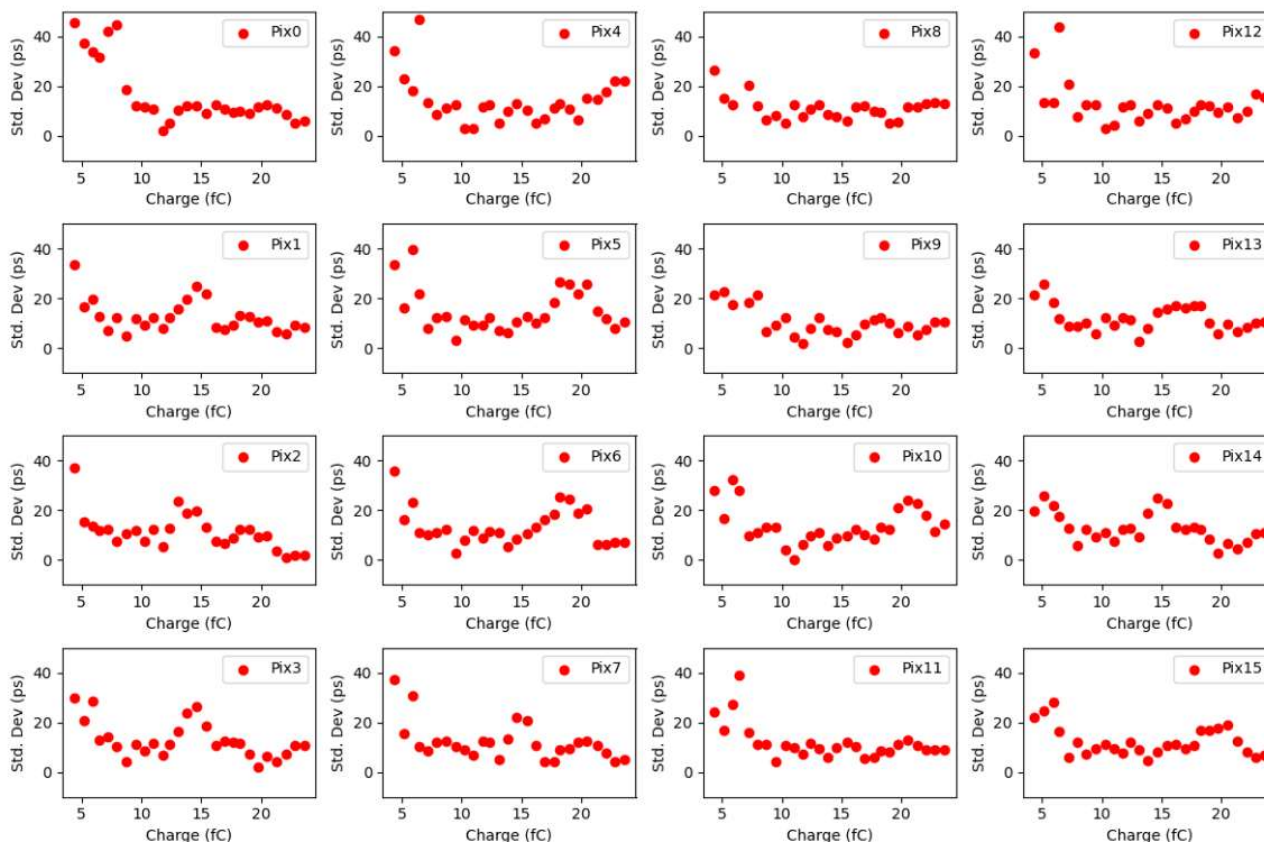


Measurements performed to align all the pulses, and then obtain a minimum threshold to detect a minimum charge: for neighboring charge selection.

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From A. Sharma : <https://indico.in2p3.fr/event/33456/contributions/144321>

TDC Jitter

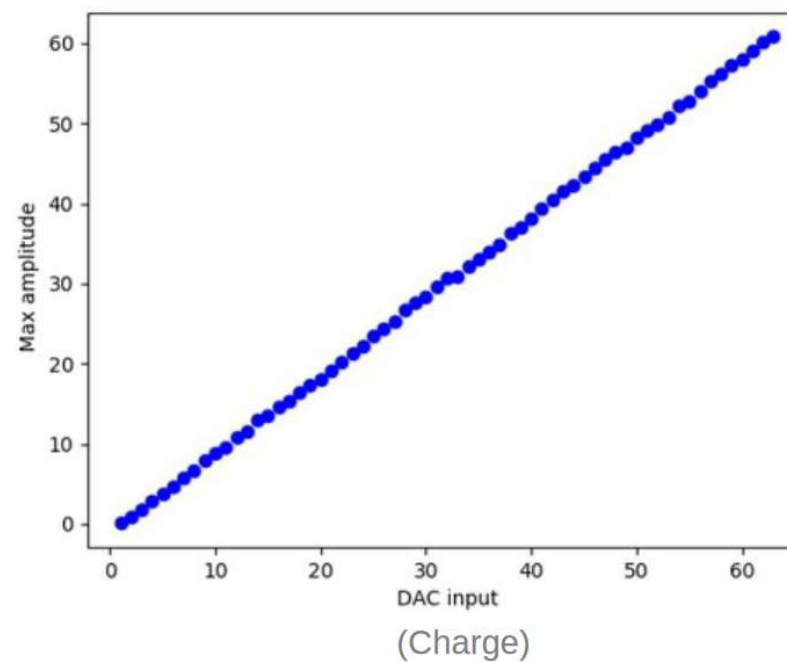
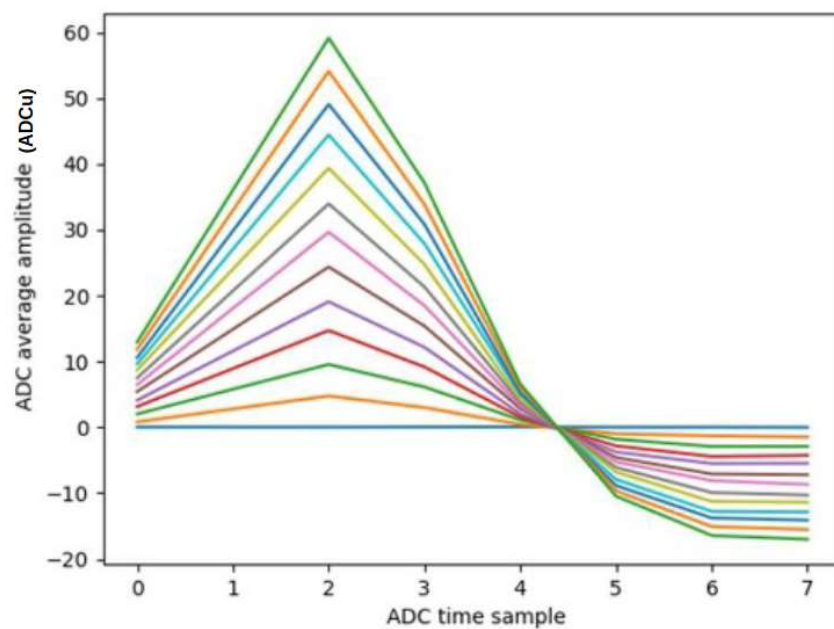


• At 23 fc,
 $\sigma \sim 10$ ps

From A. Sharma :<https://indico.in2p3.fr/event/33456/contributions/144321>

ADC studies: Charge Scan for Pix1

Amplitudes as a function of time with pedestal subtraction (w.r.t. lower charge).

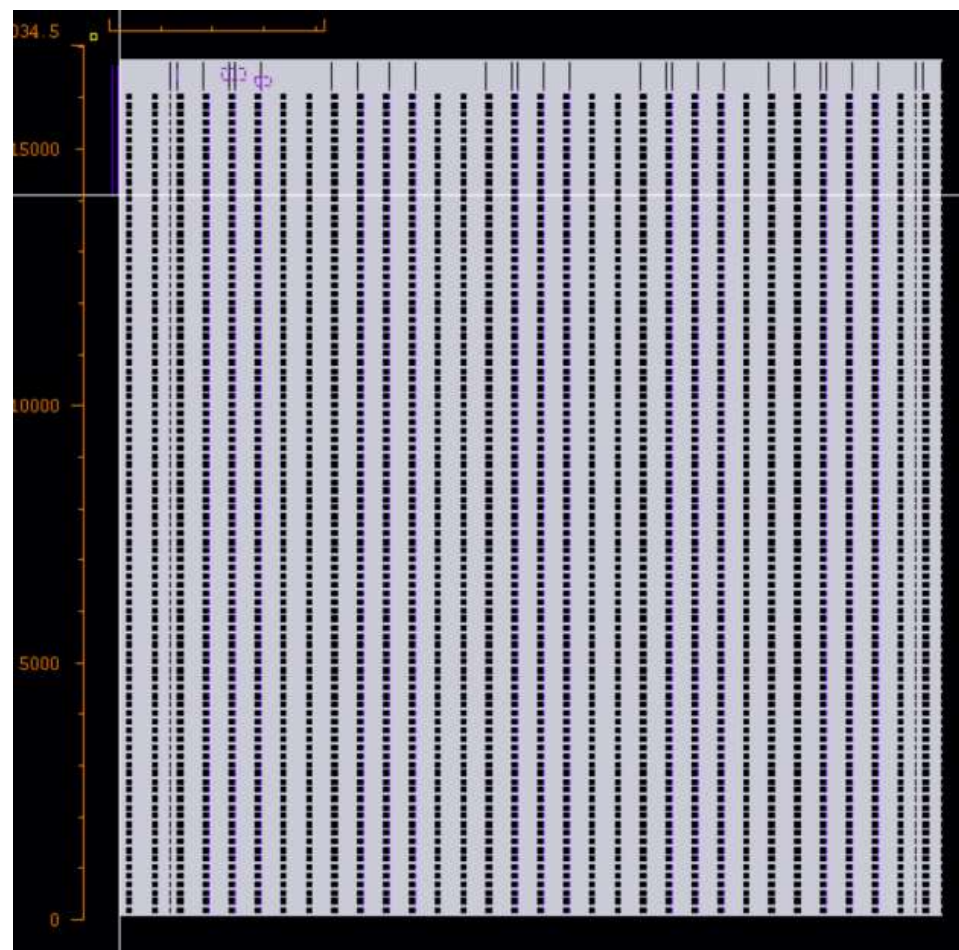


EICROC0 variants

- EICROC0A : same as EICROC0 with more testability
 - Each pixel can be by-passed by SC (clock is then turned off)
 - Buffers in SC to allow extension to 4x32
 - Larger dynamic range in pulse injection
- EICROC0B
 - Same preamp/discr/TDC/integrator
 - ADC and driver replaced by peak sensing and Wilkinson ADC
 - Currently ADC path ~ 1 mW/ch becomes 200 μ W/ch
- Will be fabricated with EICROC1 below

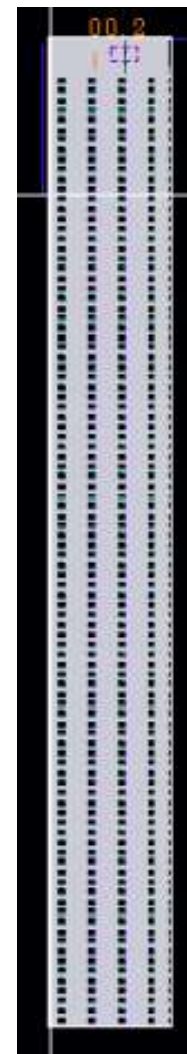


- 32x32 chip : final dimensions
- Goal :
 - test full-scale chip analog performance (IR drops)
 - Allow final sensor characterization
 - Test interface with DAQ : fast commands and 320 Mb/s data output
 - Progress on module/front-end boards
- Caveats ;
 - Not (yet) zero-suppressed data
 - Still 2mW/ch
 - Still analog-on-top



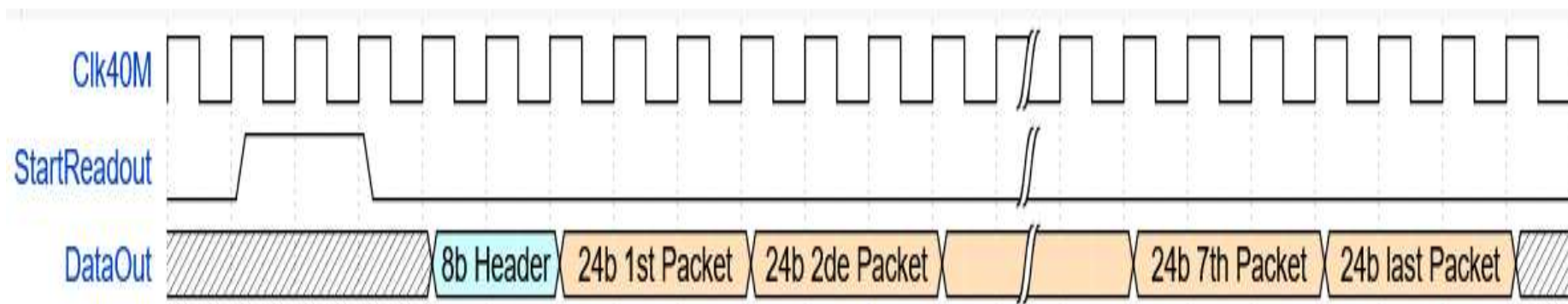
EICROC1 description

- Designed as 8 blocks of 4x32
 - Read out sequentially, like EICROC0
 - Pixel similar to EICROC0A
 - 8 CLPS outputs at 40 MHz
 - Clock tree for isochronous calib_pulse distribution
- Common balcony (End of column)
 - Biases and slow control
 - **New** : fast command decoder (clock, calib_pulse, enable_acquisition, start_readout)
 - Backup clock and cmd_pulse inputs available
 - **New** : 320 MHz serializer for 1 CLPS output



- Digital inputs
 - CLK_320 and FCMD (clock and fast commands) : CLPS
 - RSTb and RSTb_I2C : 1.2 V CMOS active low
 - SDA, SCL and 4b address : I2C slow control 1.2V CMOS
 - SEL_FCMD : 1.2V CMOS to select the backup inputs (below) (default fcmd)
 - Backup inputs : like EICROC0 (clk_160, cmd_pulse, en_acq, start_ro)
 - All unused inputs can be left floating (internal pull-ups/pull-downs)
- Digital outputs
 - 8 x 40 MHz data output (CLPS) by block of 4x32
 - one 320 MHz serialized data output (CLPS)
 - one trigger output (OR of all internal triggers) (CLPS)
 - One digital probe (1.2V CMOS) for debugging
- Analog outputs : for debugging (2 preamp outputs, analog probe, bias probe)

- Same as EICROC0 :
 - Data format : the 8 packets of 24 bits represent 8 successive samples of the data. One packet of 24 formats is ordered as followed : packet[23]=0, packet[22:12]=TDC[10:0], packet[11:9]=0, packet[8:1]=ADC[7:0], packet[0]=hit



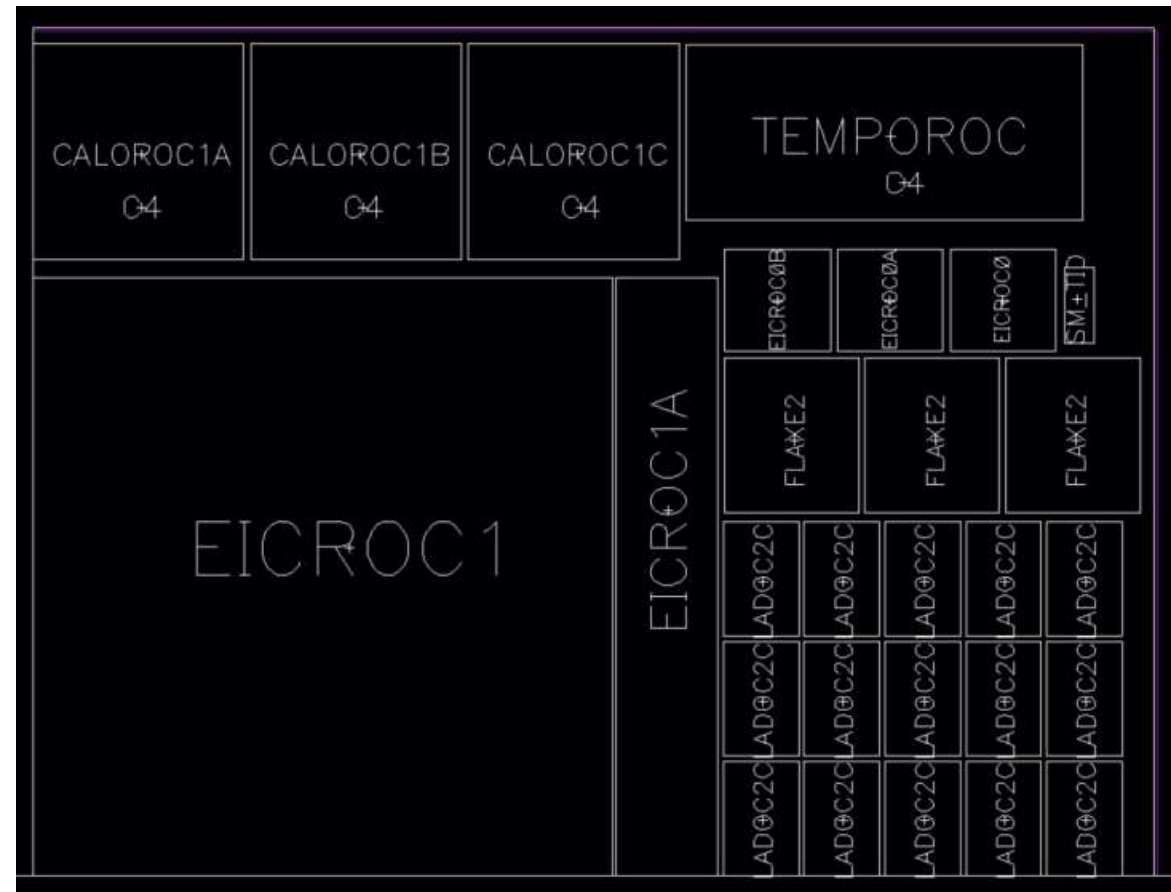
- Payload and readout speed
 - Each pixels provides 8 samples of 24 bits (12b TDC 12b ADC) at 40 MHz + header
 - $200 \text{ bits} * 25 \text{ ns} = 5 \text{ us/pixel}$
 - $128 \text{ pixels} * 5 \text{ us} = 640 \text{ us} \Rightarrow \sim 1.5 \text{ kHz maximum rate}$ per block of $4 \times 32 \sim 10 \text{ Hz/pixel}$
 - Same rate for full chip with serialized 320 MHz output
 - Spec is 15 Hz/pixel (max 28 Hz)
- Future improvements
 - Payload reduction to 12b TD C + 5 samples of 8b ADC = 64 bits $\Rightarrow \sim 30 \text{ Hz/pixel max rate}$
 - Zero-suppression : read only channels with hits and their (4-8) neighbours (for barycenters)
 - With 1 hit/column gives ~ 10 improvement $\Rightarrow \sim 300 \text{ Hz/pixel max rate}$
 - A derandomizer would also be needed

- Full block of 4x32 of EICROC1 with old EICROC0 pinout
 - Same balcony as EICROC0A (same slow control parameters)
 - Same testboard and DAQ as EICROC0
 - Allows to test columns specific effects (IR drops)



EICROC reticle 2025

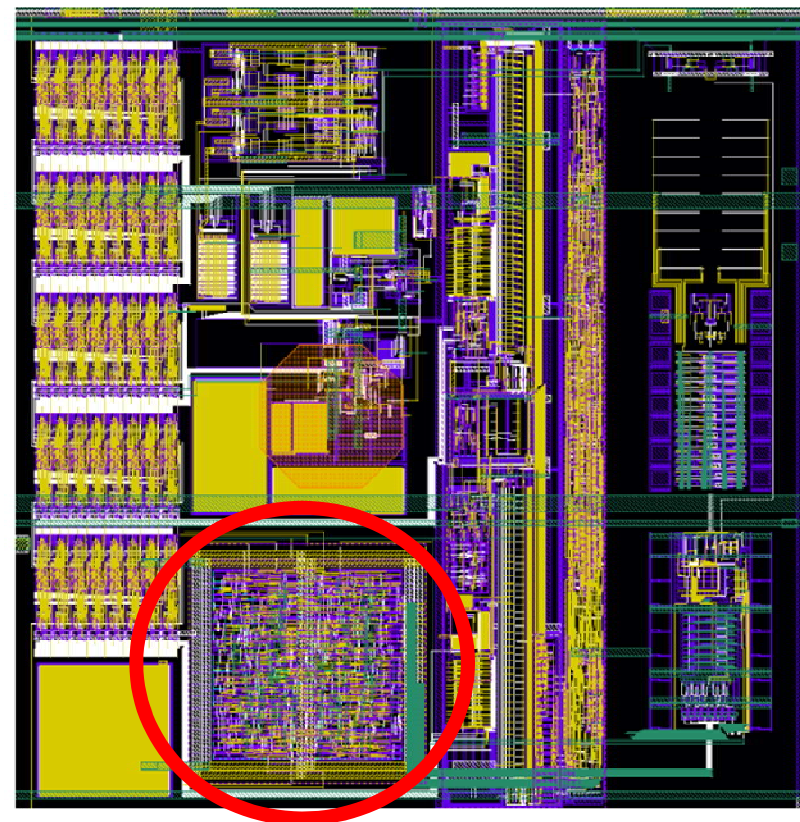
- TSMC now requires to fully populate the reticle of 24x32
 - Cost ~300 k€
- For EIC we have
 - 1 EICROC1 32x32
 - 1 EICROC1A 4x32
 - 3 EICROC0/A/B 4x4
 - 3 CALOROC1A/B/C
 - ~70% of reticle area
 - EICROC1 is 40% of reticle area
 - [gds files loaded end of may](#)
- Still administrative issues delaying the start of fabrication



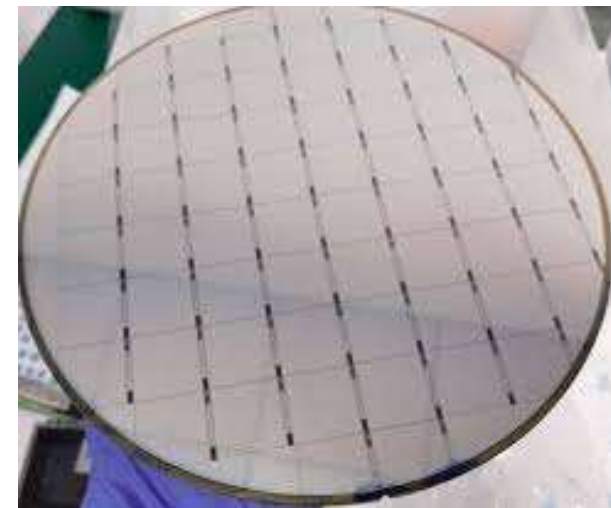
- What is missing in EICROC1 ?
 - Larger rate compatibility ?
 - **Derandomizer** for successive events (how many ?)
 - **Digital on Top** (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
 - Auto-trigger and zero_suppressed data
 - Power reduction if possible down to ~1 mW/ch
- Our colleagues from Clermont Ferrand now joining to help on the DoT
 - Already participated in ATLAS ALTIROC
 - The design **and verification** should take ~1 year from now
- Technology choice ?
 - Depends mostly on rate estimates and complexity of digital

Technology choice 65/130n

- Little impact on analog/digital performance
 - Analog similar in 65/130
 - Possibly more significant on TDC
 - Digital much simpler than LHC chips
- Update of digital part
 - Little space available => main reason for 65 !
- sizeable cost impact : ER 700 k\$ vs 300 k\$
 - But possibly more partners (but EICROC 50% of reticle)
- Prepare for design in 65 nm
 - Make an EICROC0/65n to test analog part and TDC



- For roman pots ~500 chips would be needed (500 k ch) = 6 wafers
 - Small quantity (200 wafers done for ATLAS or CMS)
- Final version would be an EICROC3 to fix possible bugs in EICROC2
 - ~1 year after EICROC2 tests and system tests complete
- Wafer probing station and test setup will be needed
 - Can be inspired from ALTIROC setup



- EICROC now reached full scale 32x32 with EICROC1
 - Important for analog performance and sensor test
 - Also allows to progress on system design
- Small scale EICROCs 4x4 still under test to improve performance and reduce power
 - Foresee also version in 65n in case digital does not fit in 130n
- EICROC2 now needs its digital design : ~1 year design time from now
 - With the most welcome help from Clermont Ferrand lab
 - Main driving specification is the hit rate : 50 Hz/pixel OK ?
- System tests are (as always) an important input for chip(s) finalization

Chip	date	Techno	size	Analog	Digital	goal
EICROC0	Jun 2023	130n	4x4	Conservative	Simple	Study sensor
EICROC0A/B	beg 2025	130n	4x4	Low power	same	Study analog
EICROC1	beg 2025	130n	32x32	Conservative	Same	Study power distribution
EICROC0_65n	end 2025	65n	4x4	final	Simple	Study analog in 65n
EICROC2	End 2026	?	32x32	Low power	Final	First final prototype

Chip	date	Techno	size	Analog	Digital	goal
CALOROC1A	beg 2025	130n	36ch	Conservative	Final	Study sensor
CALOROC1B	beg 2025	130n	36ch	Low noise	final	Study analog
CALOROC2	End 2026	130n	36/72	final	final	First final prototype