

DAC0 scan/ Digital control test

2025/06/13 Takahiro Kikuchi

Commissioning at 6/10 night

- DAC0 scan (by Itsuka)
 - Run66695-66711 (not all)
- Digital control test (me)
 - Run 66712-66716

DAC0 scan

- Took DAC0 = 15, 20, 25, 30, 35, 40
- 2 runs for each value.
- Run66695-66711
- Please see Run sheet
- https://docs.google.com/spreadsheets/d/175Z06nDFWACKIrvqN_R43ABLtRfE6r23u9CZtVuwDHg/edit?gid=1495268696#gid=1495268696
- DSTs are in
- **/sphenix/tg/tg01/commissioning/INTT/data/dst_files/2025/DST_beam_intt-00066689_special.root**
- Will be handed to Nao.

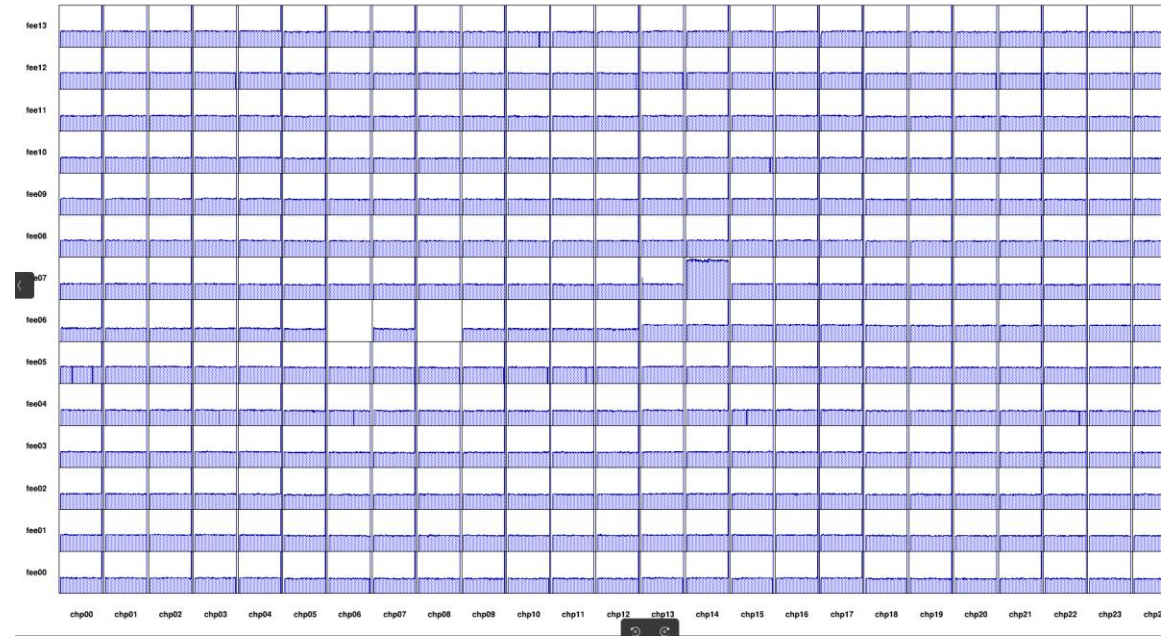
Digital control test

- I took 6 runs:
 - Normal (0xCF5110**7**0)
 - One output serial line (0xCF5110**6**0)
 - Another one output serial line (0xCF5110**E**0)
 - Mask everything (0xCF5110**0**0)
 - Custom setting × 2
- Run 66712-66716
- DSTs are in
- **/sphenix/tg/tg01/commissioning/INTT/data/dst_files/2025/DST_beam_intt-00066712_special.root**
- DST will be handed to Tomoki

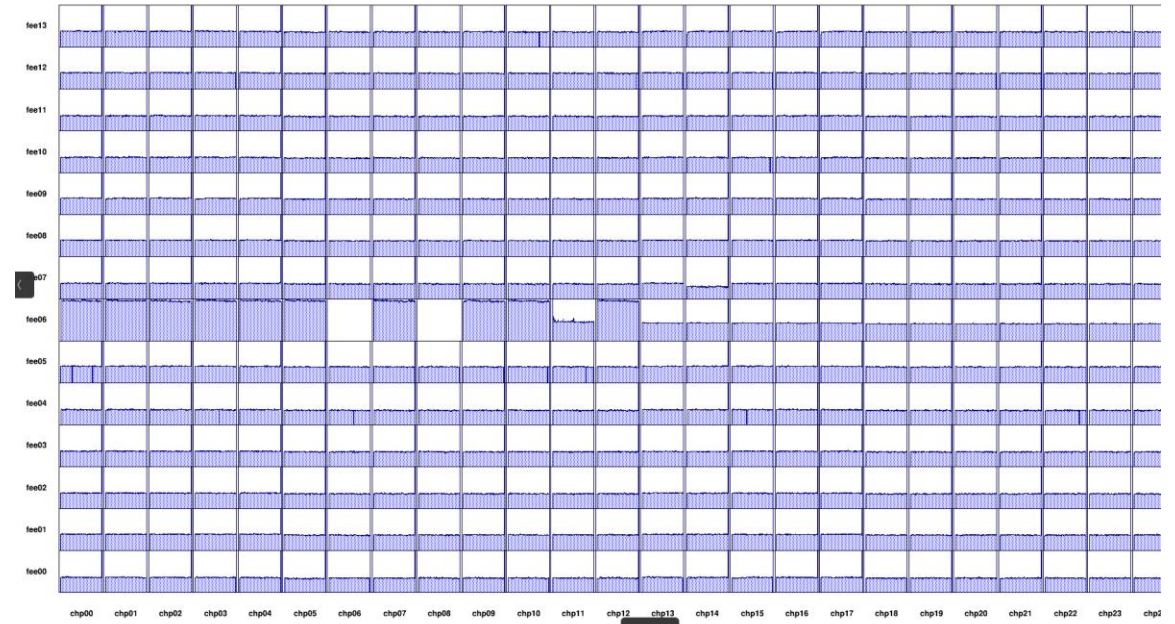
Quick view

- With one serial line, hitmap looks like that.
- I'm not sure what these “**looks half(log scale?) hitmap**” means since I just checked by eye.

intt0 run: 00066713 type: beam



intt0 run: 00066712 type: beam



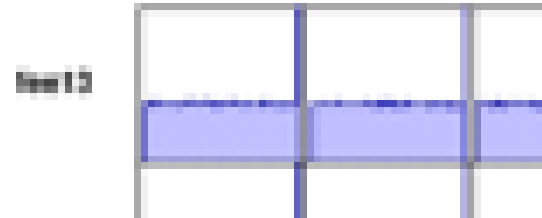
Quick view

- For custom Digital Control setting:
 - I choose some ladders as “mask”, “one serial line”, “another serial line” randomly.

- “mask” must show



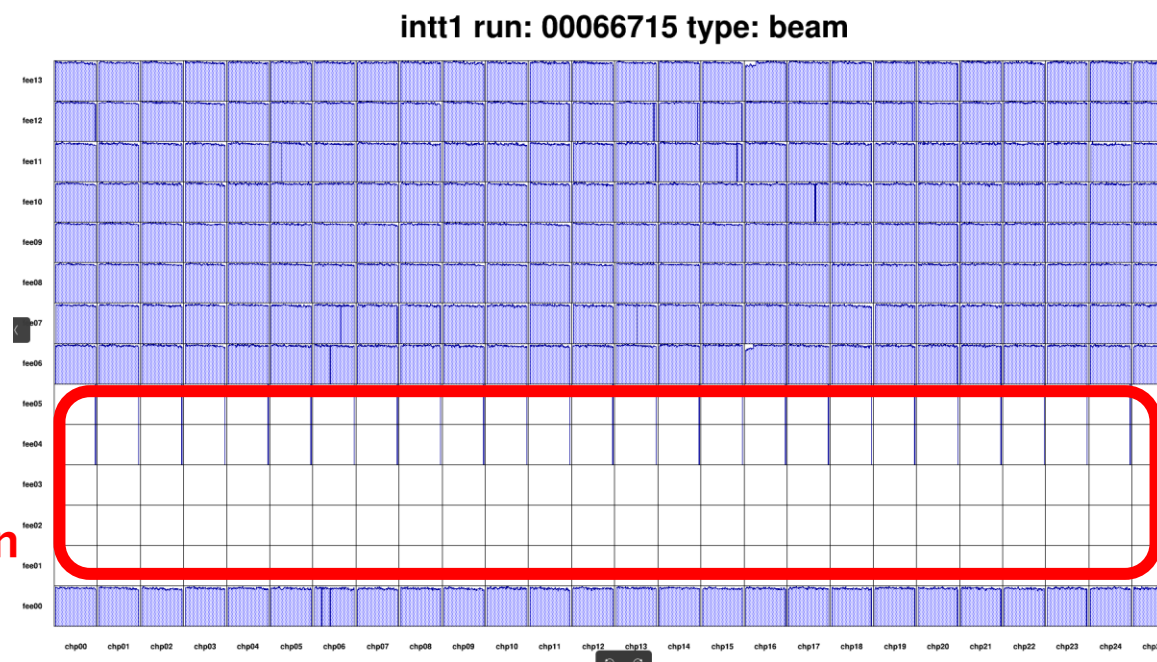
- “one/another serial line” must show



Quick view

- Intt 0
- Ladder 1-5 “mask”
- Looks good

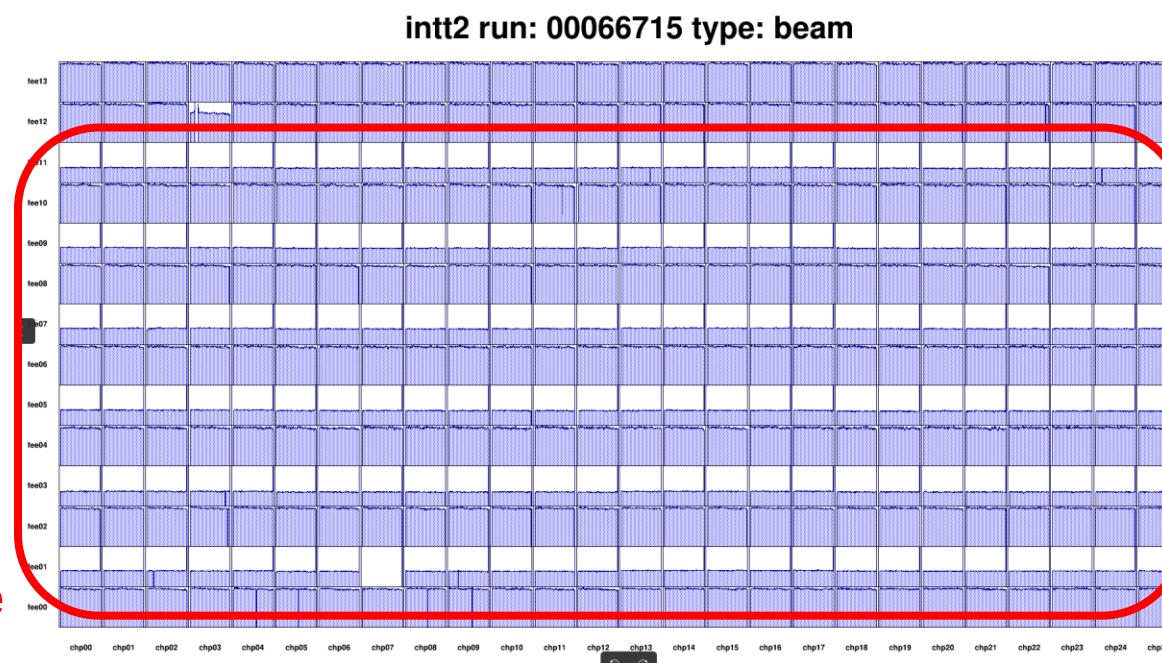
Now masking by DigCon



Quick view

- Intt2
- Ladder 1,3,5,7,9,11 “one serial”
- Looks good

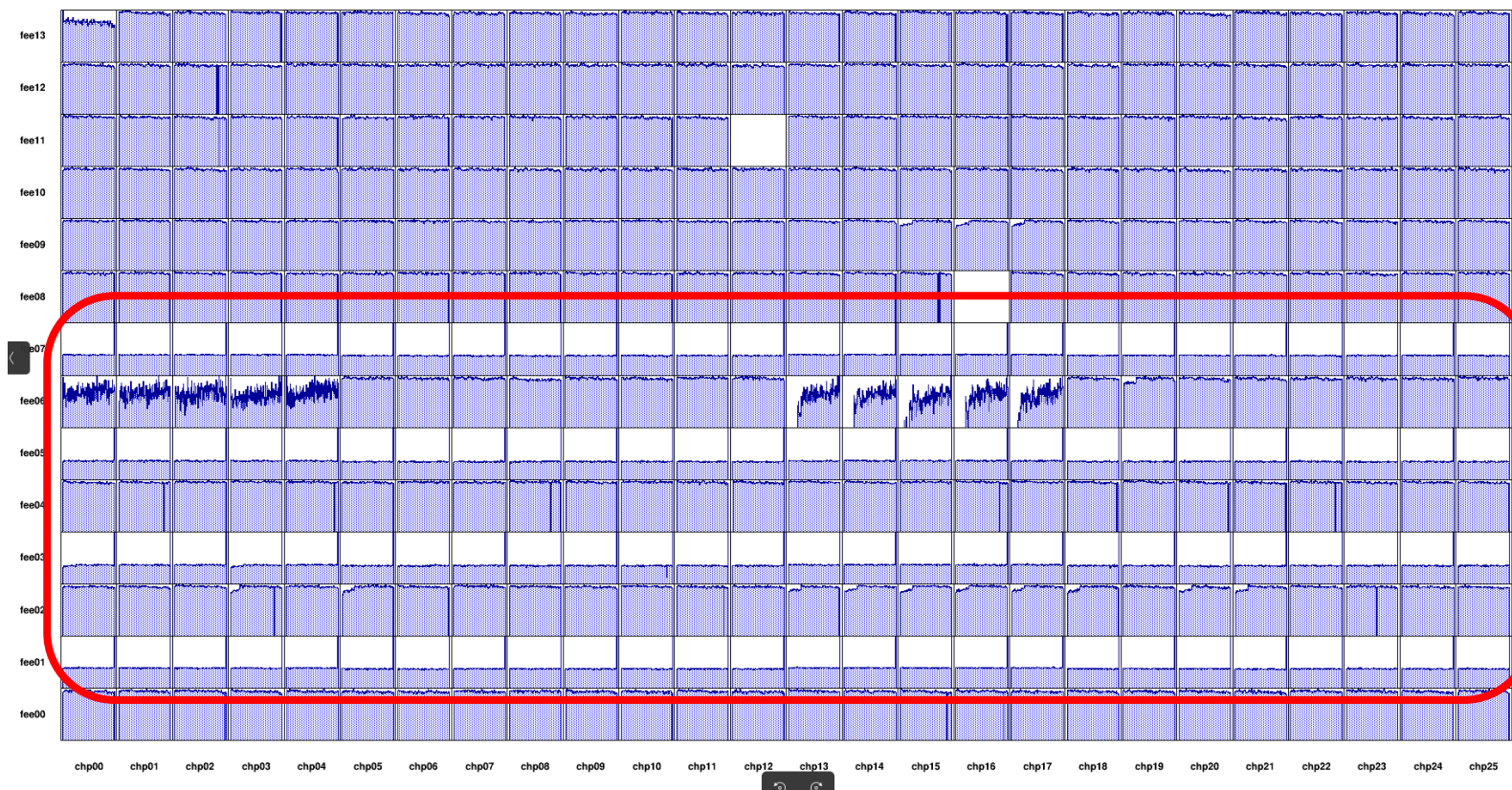
1,3,5,7,9,11
One serial line



Quick view

- Intt3
- Ladder 1,3,5,7 “one serial”
- Looks good

intt4 run: 00066715 type: beam



1,3,5,7
One serial line

DigCon test

- Changing all digital control command looks working.
- Also, Custom Digital Control looks working.
- The clue of Digital control working is the increase of clone hits.
- Tomoki will analyze these run and check
 - “number of hits”
 - “number of clone hits”
 - Which chips have “half entry issue” and make new map

How to apply Custom Digital Control

- Change the symbolic link “intt_ext.py”
in ~/INTT/sphenix_intt.py (ssh intt0)
- /home/phnxrc/INTT/INTT_repository/felix/intt_ext.py
- ↓
- /home/phnxrc/INTT/INTT_repository/felix/intt_ext_takahiro_20250326.py

New function

- I made function
 - “apply_digcon()”
 - “ReadDigConMap()”
- In
/home/phnxrc/INTT/INTT_repository/felix/intt_ext_takahiro_
20250326.py
- And also added “apply_digcon()” in “take_data()” after
running “enable_ro()”.
- Everything is based on Custom DAC0 Value function.

Edit DigCon map

- /home/phnxrc/INTT/map_digcon/latest/digcon_map.txt
- “#” works as comment out
- “*” works as wild card
- DAQ_server: Felix_ch: Chip_id: DigCon

```
1 #DAQ_server Felix_ch Chip_id DigCon
2
3 #data can be 0
4 1 1 * 13
5 1 2 * 13
6 1 3 * 5
7 1 4 * 4
8 1 5 * 0
9
10 #try to cut one serial line
11
12 2 1 * 4
13 2 1 * 6
```