ORNL MOSAIX Mockup Board v1.1

Caution:

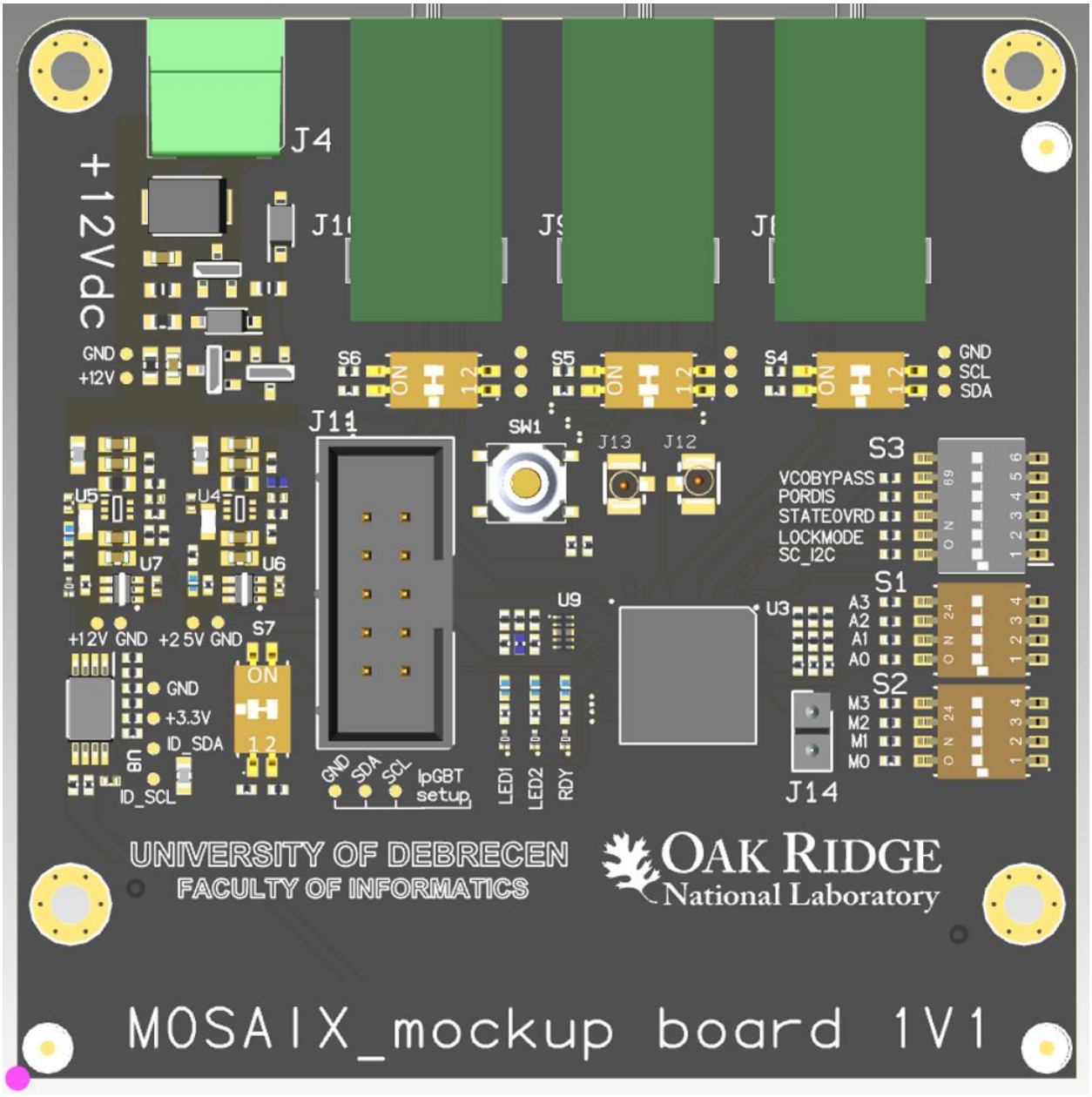
The FMC standard provides two 3.3V supplies on the FMC connector:

1. 3P3V_AUX (pin 32) to power the EEPROM
2. 3P3V (pins C39, D36, D38, and D40) for customer circuits

Connecting these two together can damage or malfunction the FPGA based board in case these two supplies come from two different voltage regulators.

Unfortunately, on the ORNL MOSAIX Mockup board these two supplies have been connected together. However, so far, all the FPGA boards I have checked use the same voltage regulator for these voltage rails, so use of this board with the FPGA boards ZCU104, ZCU102, and KCU105 should be OK.

Board Layout:



VTRx+ Connectors:

J8: VTRx+ module 0. For lpGBT TX and RX (slow controls)

J9: VTRx+ module 1: For high-speed data. Connected to FMC pins DP0 (TX1), DP1 (TX2), DP2 (TX3), DP3 (TX4)

J10: VTRx+ module 2: For high-speed data. Connected to FMC pins DP4 (TX1), DP5 (TX2), DP6 (TX3), DP7 (TX4)

Switches:

Switch S1: lpGBT I2C Address[3:0]; I2C address bits [6:4] are fixed internal to lpGBT to 3b'111; e.g. ADDR = 4b'0100 corresponds to I2C address 7b'1110100 = d'116

Switch S2: MODE[3:0]; e.g. MODE = 4b'1111 corresponds to 10.24Gbps, FEC12, Transceiver mode

Switch S3:

1: SC_I2C/BOOTCNF1 (1)
2: LOCKMODE (1)
3: STATEOVRD/EDINECTERM (0)
4: PORDIS (0)
5: VCOBYPASS/BOOTCNF0 (1)
6: not used

SC_I2C = 1 selects I2C communication to program the lpGBT
For transceiver mode, LOCKMODE should be "1"
STATEOVRD = "StateOverride" should be disabled (0)
PORDIS = "PowerOnResetDisable" should be disabled (0)
EDINECTERM = enable/disable termination for EDINECP/N receiver

BOOTCNF0/1:

00: load register values from fuses if checksum matches
01: Copy values from ROM
10: load register values from fuses without checksum check
11: skip chip initialization

Switch S4: provides pullups for MS0_SDA/SCL lpGBT I2C going to VTRx+ module 0

Switch S5: provides pullups for MS1_SDA/SCL lpGBT I2C going to VTRx+ module 1

Switch S6: provides pullups for MS0_SDA/SCL lpGBT I2C going to VTRx+ module 2

Switch S7: pullups for lpGBT configuration I2C bus. The piGBT dongle has internal pullups, so no pullups should be selected (S7 = off)

Switch SW1: lpGBT reset (RSTB)

Jumper J14: used for fusing the lpGBT, and should be shorted (connected to **GND**) during normal operation

F4: external 12V power supply. +12V is also connected to FMC HPC connector (**FMC pins C35/C37**), do not use external power when HPC is connected

FB3 (NP) can provide 1.2V for external circuit over HPC FMC connector (most FPGA boards use this as an output rather than input)

LEDs

RDY LED: lpGBT "Ready" (pin R2)
LED 1: controlled by GPIO 7
LED 2: controlled by GPIO 10

lpGBT GPIO Assignments

GPIO 0 = MS2_DIS = 0

GPIO 1 = MS1_RSTN = 1

GPIO 2 = MS2_RSTN = 1

GPIO 3 - MS1_DIS = 0

GPIO 7 = LED1

GPIO 8 = PSMUX_A0

GPIO10 = LED2

GPIO11 = PSMUX_A1

ADC Assignments

ADC0	RSSI 0	R1=4k75, R2=1M, R3=470k (VTRx+ AppNote Fig 10 Option B)
ADC1	RSSI 1	R1=4k75, R2=1M, R3=470k (VTRx+ AppNote Fig 10 Option B)
ADC2	RSSI 2	R1=4k75, R2=1M, R3=470k (VTRx+ AppNote Fig 10 Option B)
ADC3	VTRx0 Thermistor	
ADC4	Curr_Mon_1V2	VADC*2.5A/V
ADC5	VTRx1 Thermistor	
ADC6	VTRx2 Thermistor	

For ADC7 there is a PSMUX controlling the input. The MUX is controlled by GPIO 8 (A0) and GPIO11 (A1)

b'00	Curr_Mon_2V5	VADC*2.5A/V
b'01	ADC_Vin	VADC*160k/10k
b'10	ADC_2V5	VADC*40k/10k
b'11	ADC_1V2	VADC*20k/10k

EEPROM

The FMC EDID EEPROM is programmed to set FMC Vadj to 1.2V.

lpGBT Clock connections:

PSCLK 0: FMC GBTCLK0_M2C
PSCLK 1: FMC GBTCLK1_M2C
ECLK0: FMC CLK0_M2C

lpGBT Configuration

J13 is connected like the configuration connector on the VLDB+ board. So, the piGBT translator board attached to the Raspberry Pi can be used to configure, control and monitor the lpGBT.

The lpGBT can also be configured over the FMC connector via the SCL/SDA_SLAVE pins connected to LA06

FMC PIN Assignments

FMC Pin Name	FMC Pin	MOSAIX Mockup
DP3_C2M_P	A30	MS1_TX1_P
DP3_C2M_N	A31	MS1_TX1_N
DP2_C2M_P	A26	MS1_TX2_P
DP2_C2M_N	A27	MS1_TX2_N
DP1_C2M_P	A22	MS1_TX3_P
DP1_C2M_N	A23	MS1_TX3_N
DP0_C2M_P	C2	MS1_TX4_P
DP0_C2M_N	C3	MS1_TX4_N
DP5_C2M_P	A38	MS2_TX1_P
DP5_C2M_N	A39	MS2_TX1_N
DP6_C2M_P	B36	MS2_TX2_P
DP6_C2M_N	B37	MS2_TX2_N
DP4_C2M_P	A34	MS2_TX3_P
DP4_C2M_N	A35	MS2_TX3_N
DP7_C2M_P	B32	MS2_TX4_P
DP7_C2M_N	B33	MS2_TX4_N
LA06_P	C10	SCL_SLAVE
LA06_N	C11	SDA_SLAVE

GBTCLK1_M2C_P	B20	PSCLK0_P
GBTCLK1_M2C_N	B21	PSCLK0_N
GBTCLK0_M2C_P	D4	PSCLK1_P
GBTCLK0_M2C_N	D5	PSCLK1_N
CLK0_M2C_P	H4	ECLK0_P
CLK0_M2C_N	H5	ECLK0_N
LA05_P	D11	EDOUT00_P
LA05_N	D12	EDOUT00_N
LA01_CC_P	D8	EDOUT03_P
LA01_CC_N	D9	EDOUT03_N
LA04_P	H10	EDOUT10_P
LA04_N	H11	EDOUT10_N
LA00_CC_P	G6	EDOUT13_P
LA00_CC_N	G7	EDOUT13_N
LA03_P	G9	EDIN20_P
LA03_N	G10	EDIN20_N
LA02_P	H7	EDIN30_P
LA02_N	H8	EDIN30_N

External Reference Clock

J12, J13 can be used to provide an external reference clock to the lpGBT