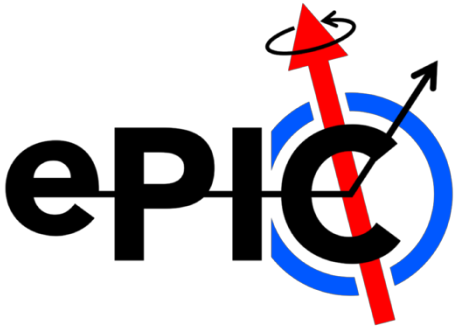
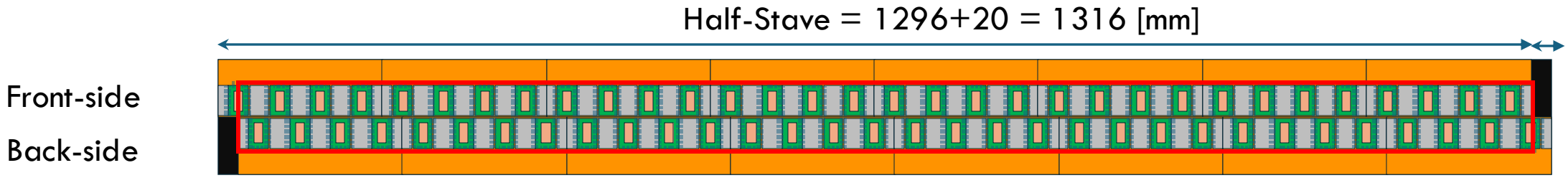


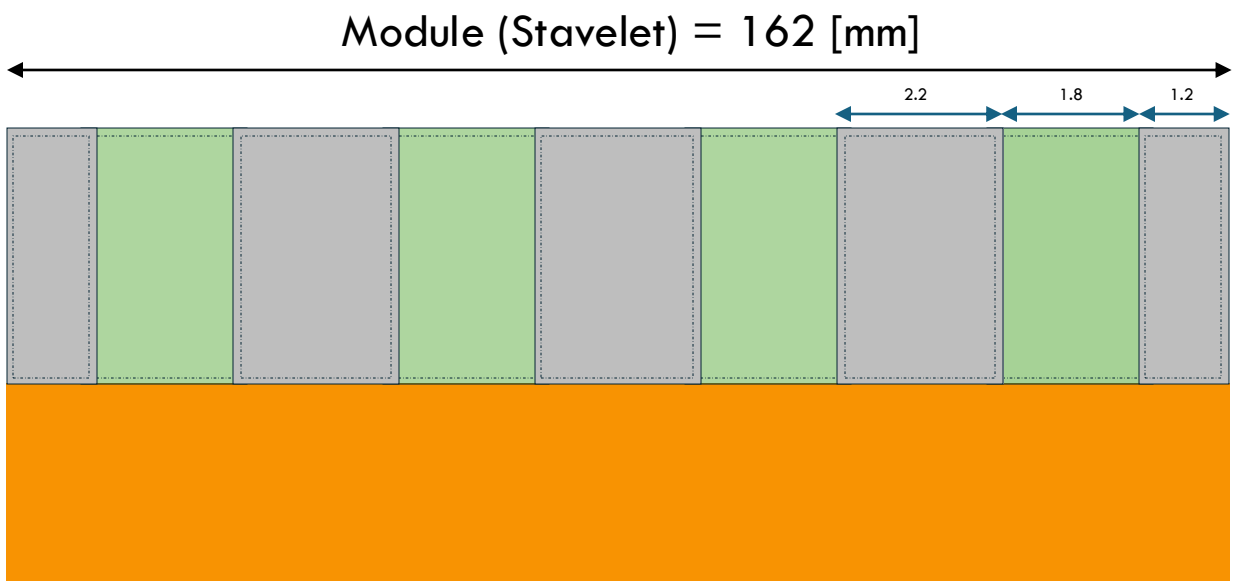
AC-LGAD Time-of-Flight

Satoshi YANO
(Hiroshima University)

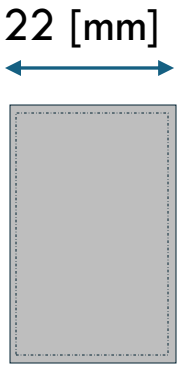
“Modularized” Stave Design



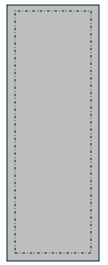
Acceptance = 1260 [mm]



x 8 x 2 x 288
=4608

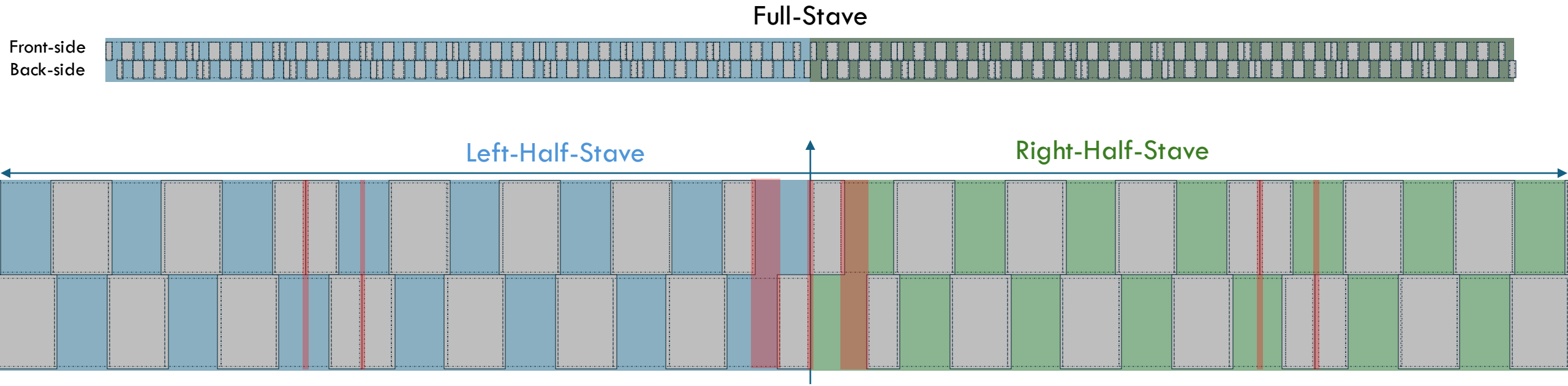


x 8 x 3 x 2 x 288
=13824



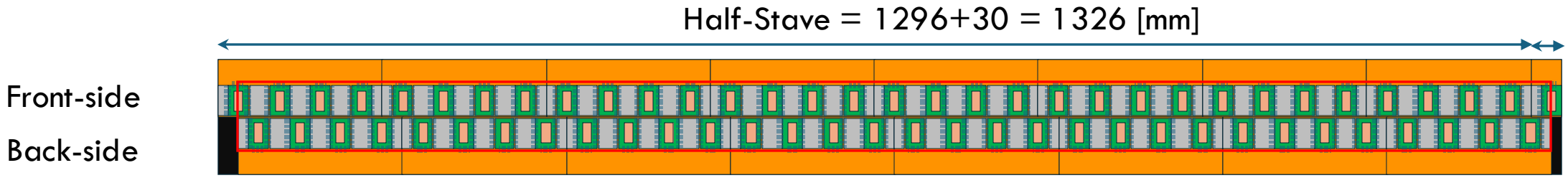
(2 x 8) x 2 x 288
=4608

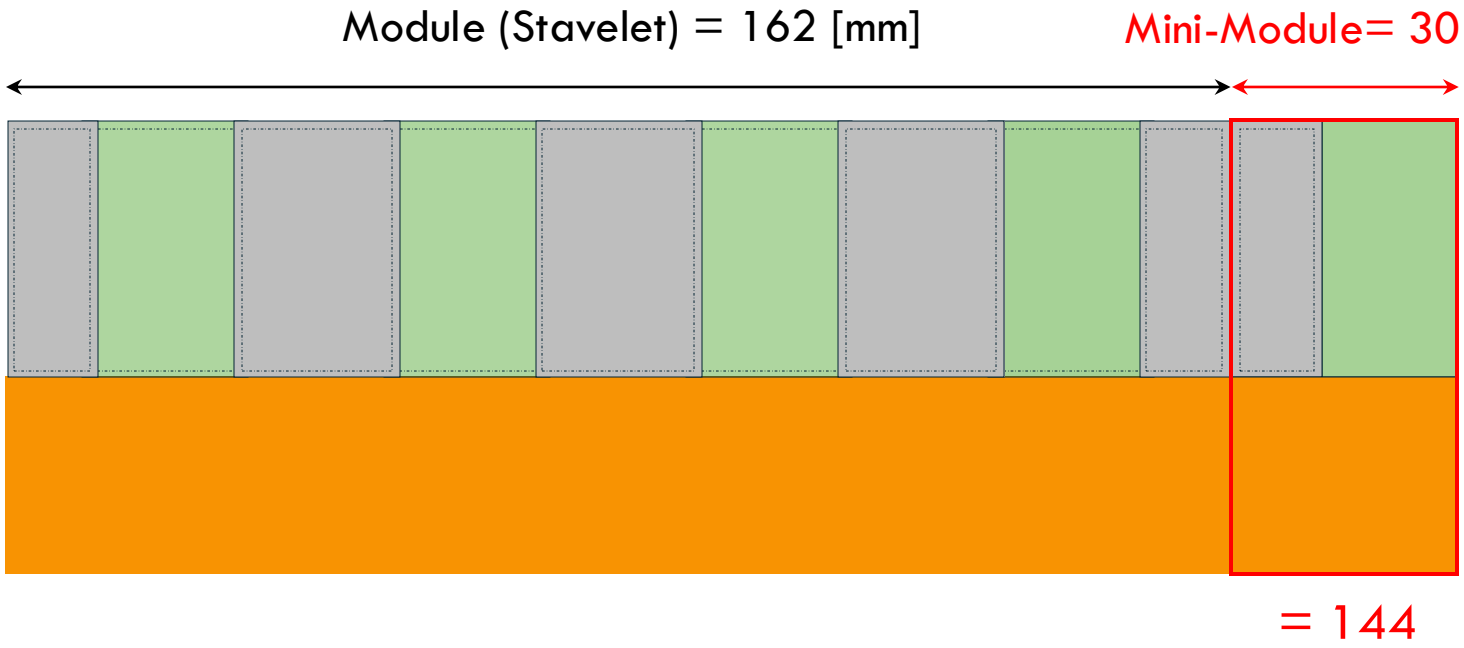
Acceptance Hole

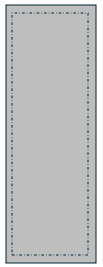


- Between half-staves, there are large acceptance holes
  - 2 mm at right in the middle, 10 mm at little sideways from the middle
- Between modules, there are small 2 mm acceptance holes
  - Due to 1 mm inactive area in a sensor

Mini-Stave Idea

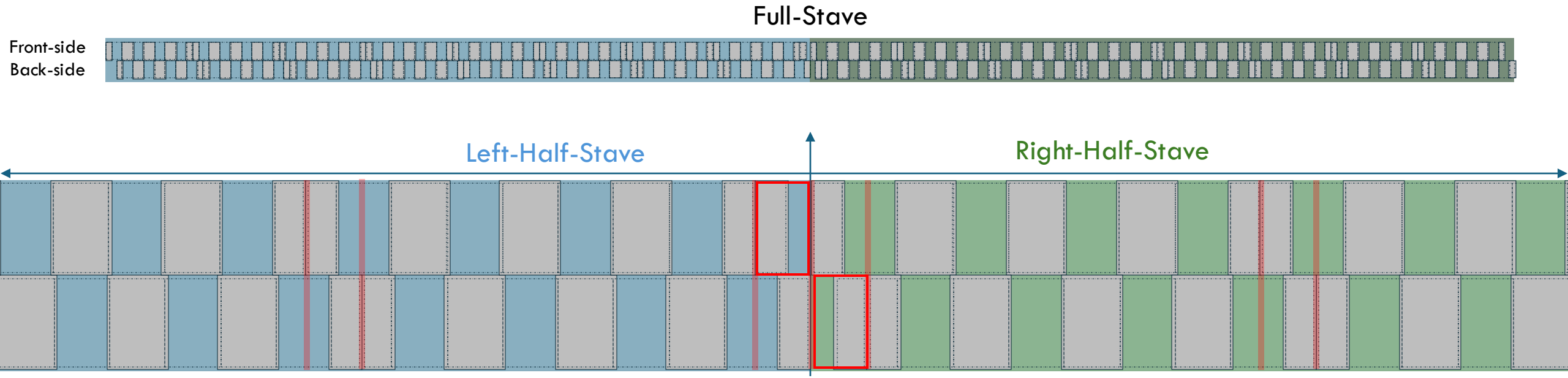






(2 x 8) x 2 x 288+144
=4752

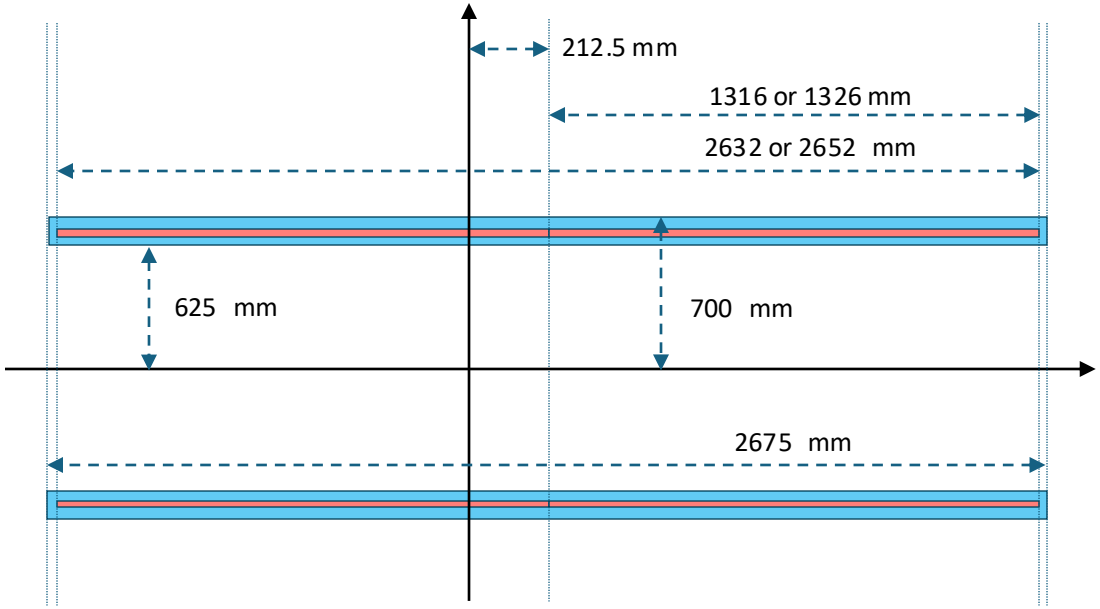
Acceptance Hole w/ Mini-Module

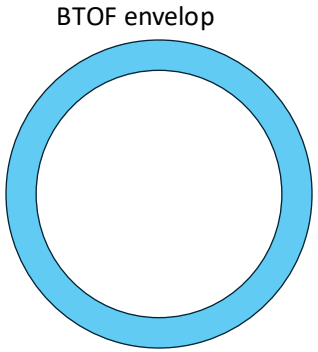


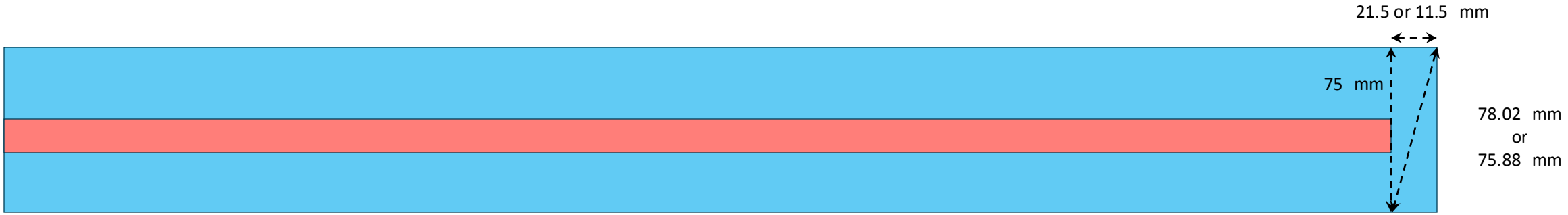
- Between half-staves, there are large acceptance holes
  - 2 mm at right in the middle, 10 mm at little sideways from the middle

- ~~Between modules, there are small 2 mm acceptance holes~~
  - ~~Due to 1 mm inactive area in a sensor~~

Service-Hybrid Location







ASICs candidates for prototyping

- **FCFD**
  - Designed for strip AC-LGAD by FNAL (65nm)
  - Analog block
    - C_{in} = ~10 pF
    - Q_{range} = 1 ~ 30 fC
  - TDC TOA and TOT
  - Power budget: 2 mW/ch
- **EICROC**
  - Designed for pixel AC-LGAD by OMEGA (130nm)
  - Analog block
    - C_{in} = 4 pF
    - Q_{min} = 1 ~ 30 fC
  - Analog from (similar to) ALTIROC
  - ADC from HGCROC
  - TDC (TOA) from HGCROC
  - Power budget: 1 mW/ch
- **ETROC**
  - Designed for DC-LGAD by FNAL (65nm)
  - Analog block
    - C_{in} = 2-5 pF
    - Q_{min} = 10 ~ 20 fC
  - TDC (TOA and TOT)
  - Power budget: 3 mW/ch
- **HGCROC**
  - Designed for Si sensor by OMEGA (130nm)
  - Analog block
    - C_{in} = 5~50 pF
    - Q_{range} = 0.2fC ~ 10pC
  - ADC with 10 bit → 0.4 fC
  - TDC TOT with 12 bit → 2.5 fC
  - TDC TOA with 10 bit
  - Power budget: 15 mW/ch
- **H2GCROC (HGCROC for SiPM)**
  - Designed for SiPM by OMEGA (130nm)
  - HGCROC + input current conveyor (analog block)
  - Analog block
    - C_{in} = 0.5~10 nF
    - Q_{range} = 50fC ~ 300pC
  - Power budget: 10 mW/ch
- **CALOROC1C**
  - Designed for Si sensor by OMEGA (130nm)
  - Analog block
    - C_{in} < 100 pF
    - Q_{range} = 0.2fC ~ 10pC
  - ADC/TOT and TOA are based on HGCROC
  - Power budget: 15 mW/ch
  - (CALOROC1A & 1B based on H2GCROC)