AncASIC - March MPWs: test plan, progress on setups development, discussion

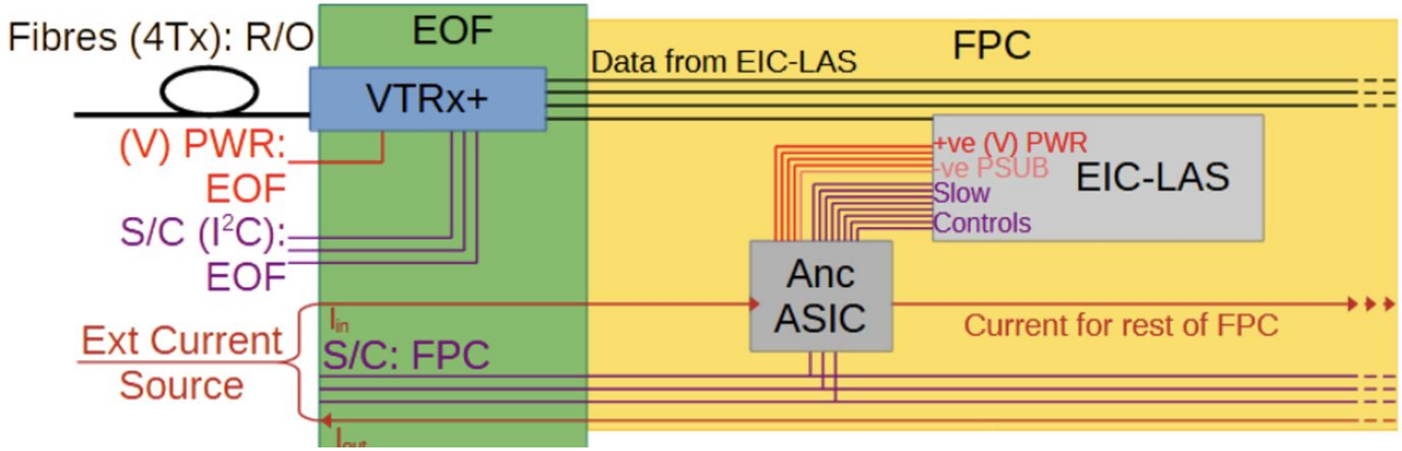
Lukas Tomasek on behalf of WP2

July 9, 2025, SVT working meeting Stony Brook

AncASIC general describtion

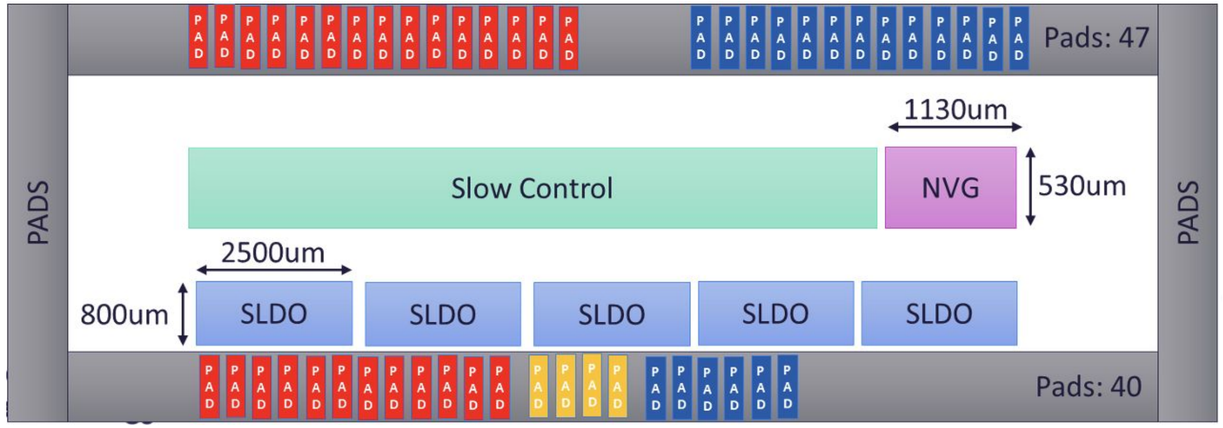
Main blocks:

- Negative Voltage Generator NVG
- SLDO
- AncBRAIN with slow Control



Development stages (preliminary):

- MPW1, 2, 3, x - prototype (chiplets)
- ER AncASIC production on 8“ wafers



MPW1/MPW2

MPW1 - AncASICXT011_P1:

- Negative Voltage Generator (NVG)
- SLDO Pre-Regulator
- CML Transceiver
- Transistor Test Structures (for radiation hardness validation of XT011 process)

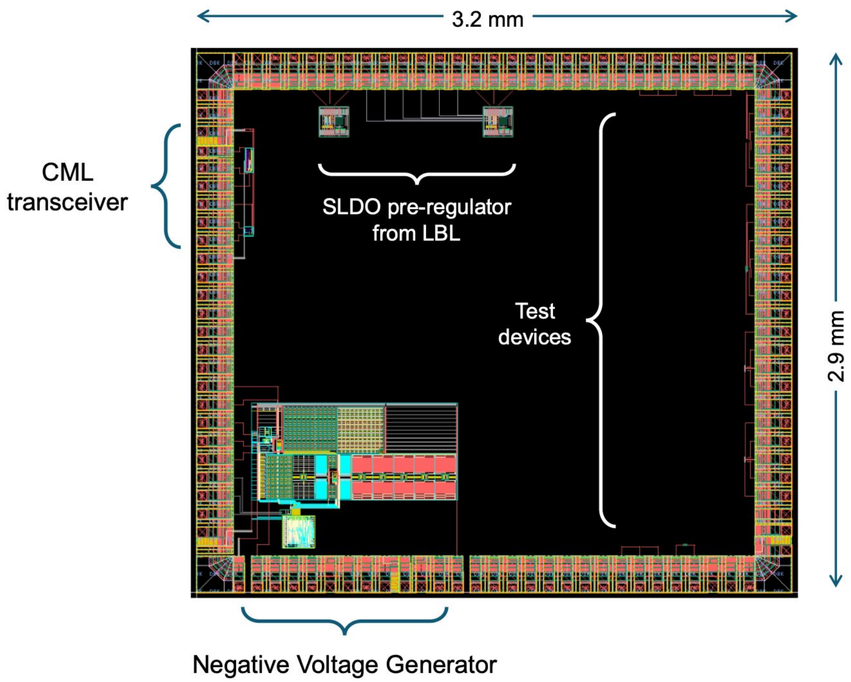
MPW2 - SLDO:

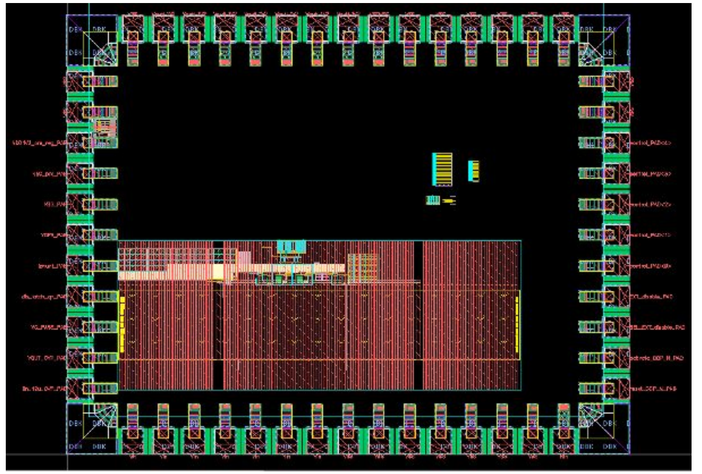
- SLDO by RAL

Details:

- **45 individual chiplets for each MPW1&2**
- already submitted
- **Delivery from the fab September 26, 2025**

1st Prototype: AncASIC sub-blocks and test devices





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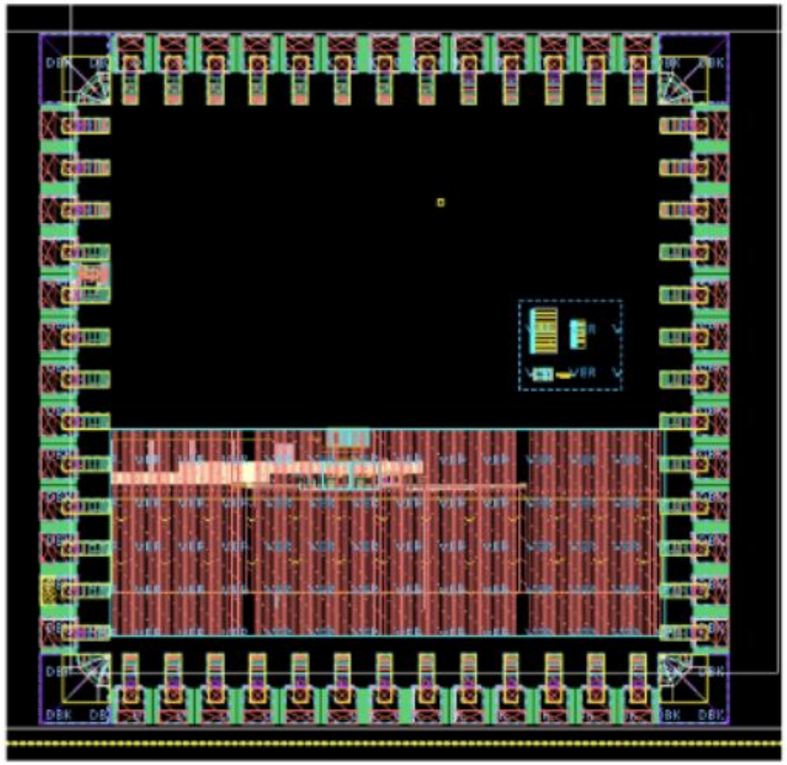
MPW3

MPW3:

- SLDO
- NVBG
- AncBrain (slow control)
- …



- individual chiplets (TBU: 45 or maybe 100)
- **Planned submission September, 2025**
- **Planned delivery March, 2026**

MPW1 AncASICXT011_P1 Task list

	MPW1 AncASICXT011_P1							
	Task	**Start date**	**End date**	**Quantity**	**Testing details, conditions**	**Comments**	**Equipment**	**Responsible group/person (interested person/group)**
	MPW1 tapeout/submission (WP1 task)		09/25					**WP1**
	MPW1 testing		03/26 ?					
1	**Test specs definition**		09/25					**WP1, WP2**
2	**Carrier board PCB design + manufacturing, pre-testing**	06/25	09/25	~45				**LBL** - Zhengwei Xue **(BNL** schematics by end of June**)** - production might need funding support from others!
3	**Chip+PCB assembly, wirebonding**	10/25	11/25	~45				**LBL** - Zhengwei Xue - production might need funding support from others!
4	**Test system HW (control)**		10/25	?				**?** - TBD if/what is needed (LANL I2C control for NVG)
5	**SLDO Pre-Regulator characterization**	10/25	03/26 ?				Standard lab equipment (power supply, IV meters, oscilloscope etc.)	**LBL -** Zhenyu Ye (UK? - maybe later)
	Output Ripple/Noise				Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)				ESR - **3.5k**			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
6	**NVG characterization**	10/25	03/26 ?				Standard lab equipment (power supply, IV meters, oscilloscope etc.) I2C control via FPGA	**LBL -** Zhenyu Ye **(CTU)** **(LANL I2C)** - Joellen Renck
	Output Ripple/Noise				Load Capacitance - RANGE?			
	Transient Response (overshoot and settling time)				Frequency - RANGE?			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Standard Supply Variation	Plus and Minus 20%		
					Ramp Rate - RANGE?			
	Test in combination with APTS/DPTS/ER1					Use NVG to generate back bias for already existing APTS and DPTS chips		
7	**CML transciever**	10/25	03/26 ?		In preparation			**LBL -** Zhenyu Ye
8	**Transistor Test Structures characterization**	10/25	01/26 ?	15?	In preparation		Standard lab equipment (power supply, IV, LCR meters, oscilloscope etc.)	**BNL** - Ivan Kotov / Niccolo' Gallice **(LBL)** **(CTU)**
	Ids vs Vgs						TTS characterization IV setup	
	Vt extraction							
					Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
					Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Standard Supply Variation	Plus and Minus 20%		
9	**Irradiation**	10/25	01/26 ?	15?				**BNL** (Cobalt60, X-ray ?) - Ivan Kotov / Niccolo' Gallice **(LBL)** (X-ray, proton) - Zhenyu Ye **(CTU)** (X-ray, Cobalt60) - Lukas Tomasek
					X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring (**cooling to 27C, ..??**)		
					Standard Radiation Range	0 - 1MRad in 100kRad steps **10krad, 100krad, 1Mrad, 10Mrad ??**		
10	**SEE/SEU Tests in a proton beam**	10/25	03/26 ?	?	TBD	TBD	Proton beam with XY table	**BNL -** Ivan Kotov / Niccolo' Gallice **LBL -** Zhenyu Ye **CTU -** (Lukas Tomasek)

MPW2 SLDO Task list

AncASIC testing task list

MPW2 SLDO

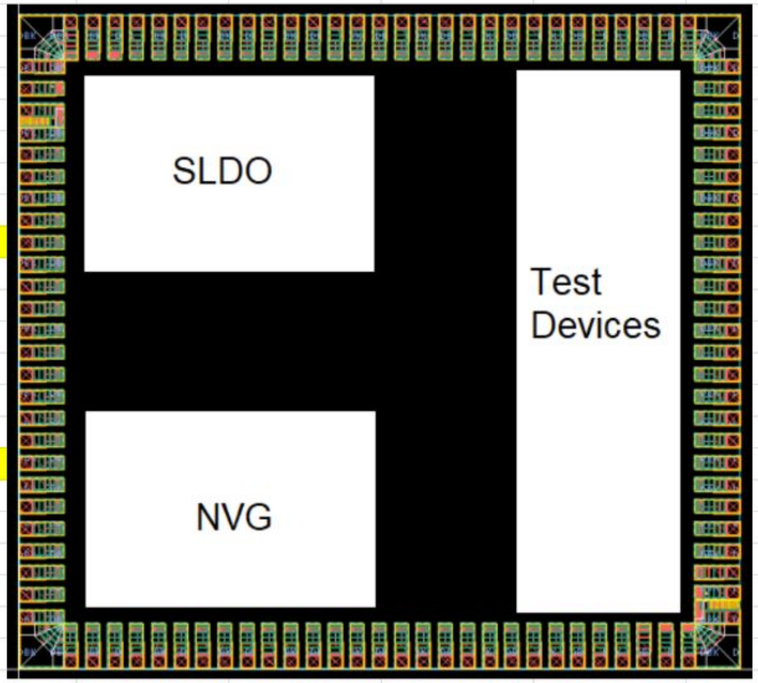
	Task	Start date	End date	Quantity	Testing details, conditions	Comments	Equipment	Responsible group/person (interested person/group)
	MPW2 tapeout/submission (WP1 task)		09/25					**WP1**
	MPW2 testing		03/26 ?					
1	**Test specs definition**		09/25					**WP1, WP2**
2	**Carrier board PCB design + manufacturing, pre-testing**	06/25	09/25	~50		PCB and test system design inc. micro-controller programming at STFC Daresbury Lab (M.Borri,A.Hill)		**Daresbury** - Andrew Hill
3	**Chip+PCB assembly, wirebonding**	10/25	10/25	~50		Wirebonding of DUTs onto carrierboards performed at Univeristy Of Birmingham (J.Glover, C.S.Tse)		**University of Birmingham (UK) -** James Glover, C.S. Tse
4	**Test system HW (control)**	06/25	10/25	5?				**Daresbury** - Andrew Hill
5	**SLDO characterization**	10/25	03/26 ?			Three institutes involved in sLDO testing: University Of Birmingham Brunel University Darasbury Laboratory	Standard lab equipment (power supply, IV meters, oscilloscope etc.)	**University Of Birmingham -** J.Glover; L.Li; **Brunel Univeristy** - L.Teodorescu; **Daresbury Lab** - M.Borri; **(LBL)**
	Output Ripple/Noise				Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)				ESR - **3.5k**			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		X-rays at Daresbury; Protons at Birmingham cyclotron (TBC);
					Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
6	**Irradiation**	10/25	03/26 ?	?				**Daresbury Lab - X-rays - M.Borri** **Univerisity of Birmingham (UK) - (TBC) Protons (Cyclotron) - J.Glover; L.Li;** **(BNL)** (Cobalt60, X-ray ?) - **(CTU)** (X-ray, Cobalt60) - **(LBL)** (X-ray, protons)
					X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring (cooling to 27C, ..??)		X-rays at STFC Daresbury Lab; Protons at Birmingham cyclotron (TBC);
					Standard Radiation Range	0 - 1MRad in 100kRad steps		
						10krad, 100krad, 1Mrad, 10Mrad ??		

- **For all tasks already defined groups and people responsible them**
- It therefore seems that we have **sufficient human and technical resources available for all tasks**, **but some clarification will be needed regarding financing** (carrier boards + assembly, irradiation)
- **Also some parameters of the tests and chip distribution still need to be discussed and clarified** (especially those related to **irradiation**)

ASICs and testing documentation status

Brief general MPW1 test plan defined by WP1:

Measurements	Conditions	Comments
NVG		
Output Ripple/Noise	Load Capacitance - RANGE?	
Transient Response (overshoot and settling time)	Frequency - RANGE?	
PSRR and line regulation	Standard Temperature Range	
Start-up	Standard Radiation Range	
	Standard Supply Variation	
	Ramp Rate - RANGE?	
Test in combination with APTS/DPTS/ER1		Use NVG to generate back bias for already existing APTS and DPTS chips
SLDO Pre-regulator		
Output Ripple/Noise	Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space
Transient Response (overshoot and settling time)	ESR - **3.5k**	Number in red is the expected value. Others are for exploring the parameter space
PSRR and line regulation	Standard Temperature Range	
Start-up	Standard Radiation Range	
	Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s	Number in red is the expected value. Others are for exploring the parameter space
Transistor Test Structures		
	Ids vs Vgs	
	Vt extraction	
	Standard Temperature Range	
	Standard Radiation Range	
	Standard Supply Variation	
	Standard Temperature Range	-20, 27, 60, 105
	Standard Radiation Range	0 - 1MRad in 100kRad steps
	Standard Supply Variation	Plus and Minus 20%



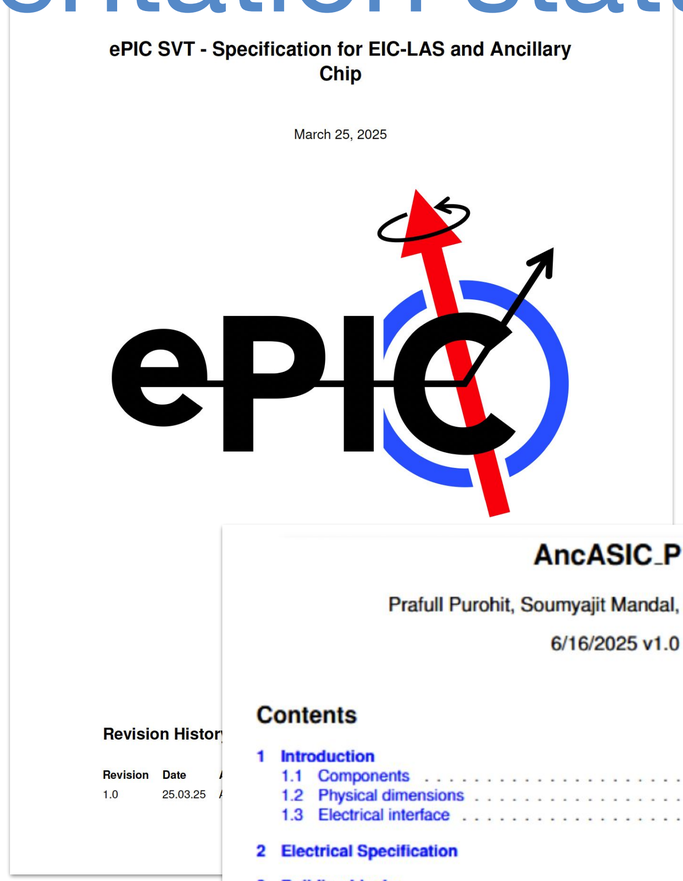
Pin List

ASICs and testing documentation status

Detailed MPW1&2 chip specifications and testing plan by WP1 in the document(s):

- Prafull Purohit et al., **AncASIC_P1**
  - NVBG
  - test structures
  - transmission line
  - CML
  - finalized by Prafull

- Iain Sedgwick et al.,**ePIC SVT - Specification for EIC-LAS and Ancillary Chip**
  - SLDO
  - NVG
  - will be updated soon

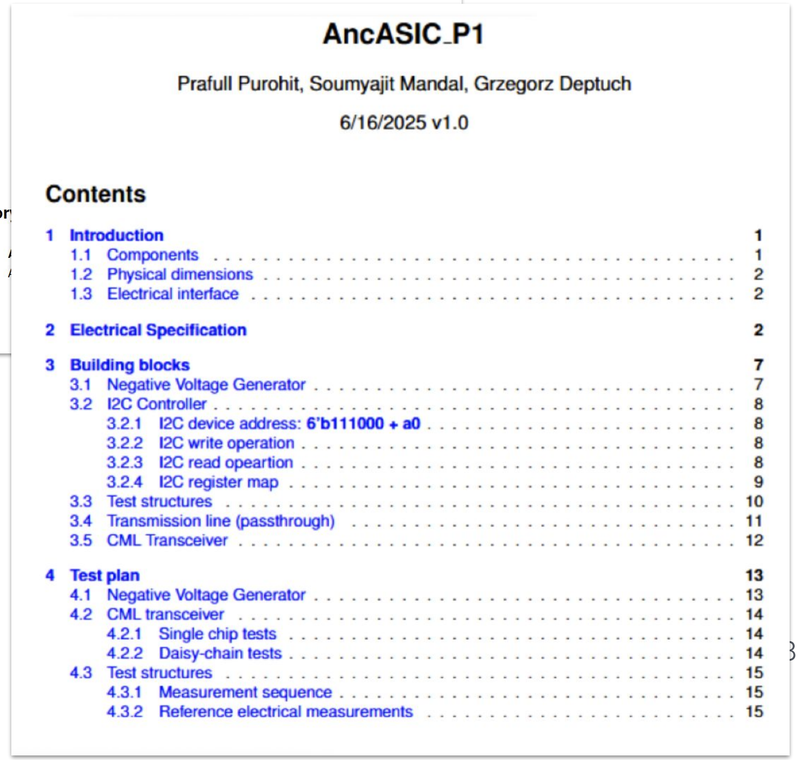


ePIC SVT - Specification for EIC-LAS and Ancillary Chip

March 25, 2025

Revision Histor

Revision	Date
1.0	25.03.25



AncASIC_P1

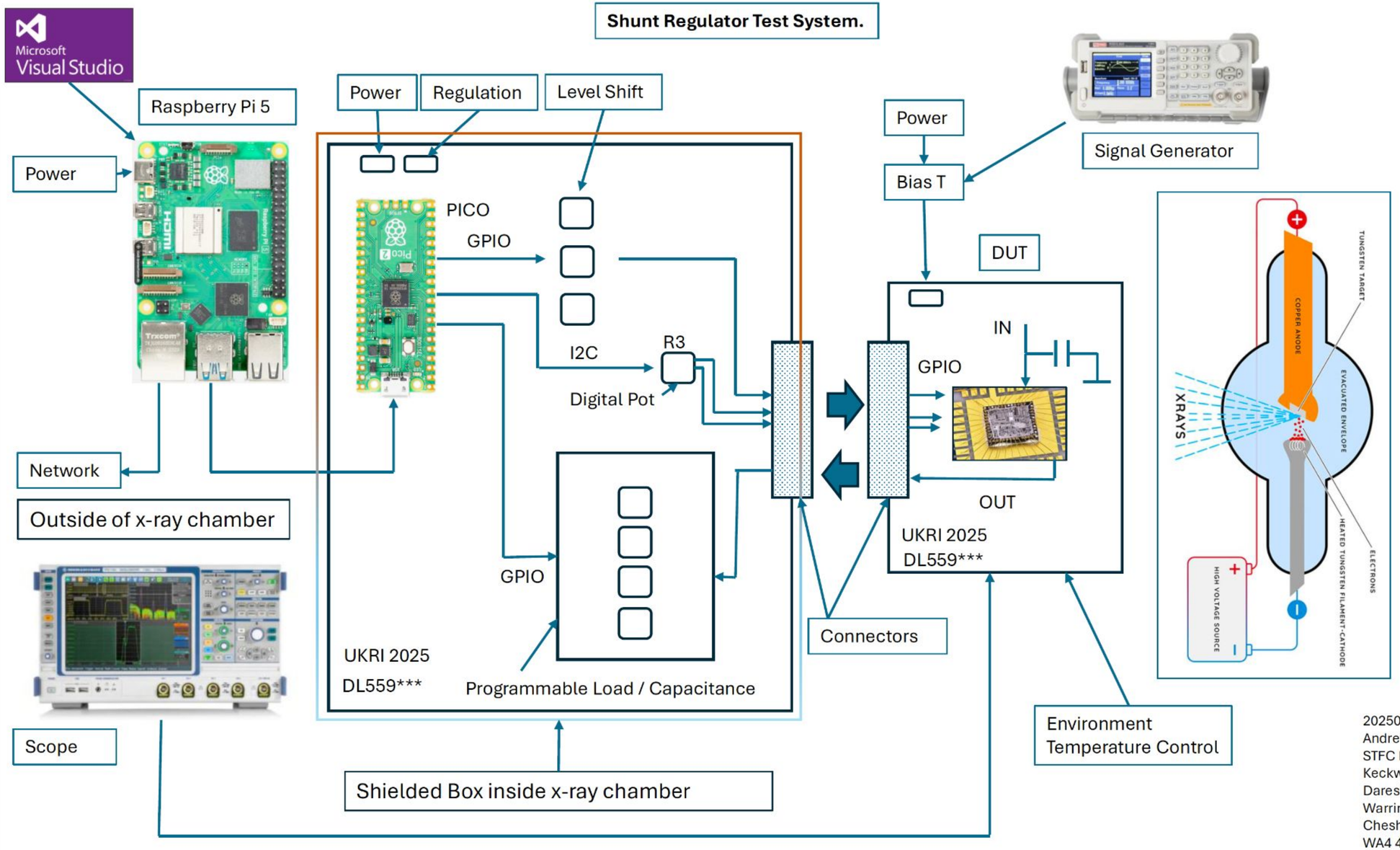
Prafull Purohit, Soumyajit Mandal, Grzegorz Deptuch

6/16/2025 v1.0

Contents

Testing HW status MPW2

Shunt Regulator Test System by Andrew Hill, STFC Daresbury Laboratory



20250609
Andrew Hill (T2)
STFC Daresbury Laboratory
Keckwick Lane
Daresbury
Warrington
Cheshire
WA4 4AD

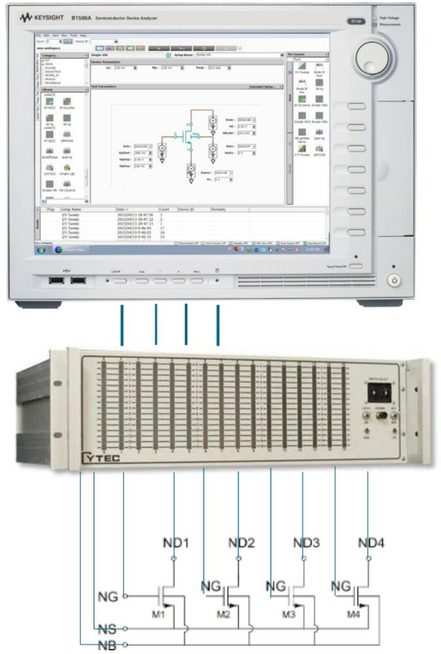
Testing HW status MPW1

- **MPW1 Carrier Board** will be designed by Zhegwei Xue from LBL with help from BNL (Grzegorz, Niccolo) to start the design for functionality testing

- **Evaluation setup for test structure characterization and irradiation testing** with ^{60}Co source available at BNL

Evaluation setup

- Currently we have two B1500A semiconductor analyzers, with 4/5 SMU units each and one C-V unit
- Re-commissioning a switching matrix to test multiple devices
- The irradiation facility allows to have some instruments close to the source (w/ appropriate shielding) and to wire additional connections/communication out to the “control room”



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Irradiation facility

- Instrumentation dpt. owned and managed facility
- ^{60}Co source with 450 Ci activity in 2020
- Characterization of handheld-size samples at high dose rates (~10-20 krad/hour)
- Dosimetry with radiation protection division
- Used for strip detectors and asic for ATLAS, sPHENIX SiPM radiation damage

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Testing SW status

Each group responsible for testing any AncASIC block in the MPW1 & MPW2 phases is also responsible for developing their own test software (with some help from WP2 SW group).

However, the **WP2 SW group** has prepared a **skeleton of a general test software framework**, which will be used in the production phase for both the sensors and the AncASIC.

Therefore, where possible and meaningful, the use of this framework is supported and encouraged.

For **MPW1 & MPW2**, we definitely want to use at least a **shared database** for all measurements.

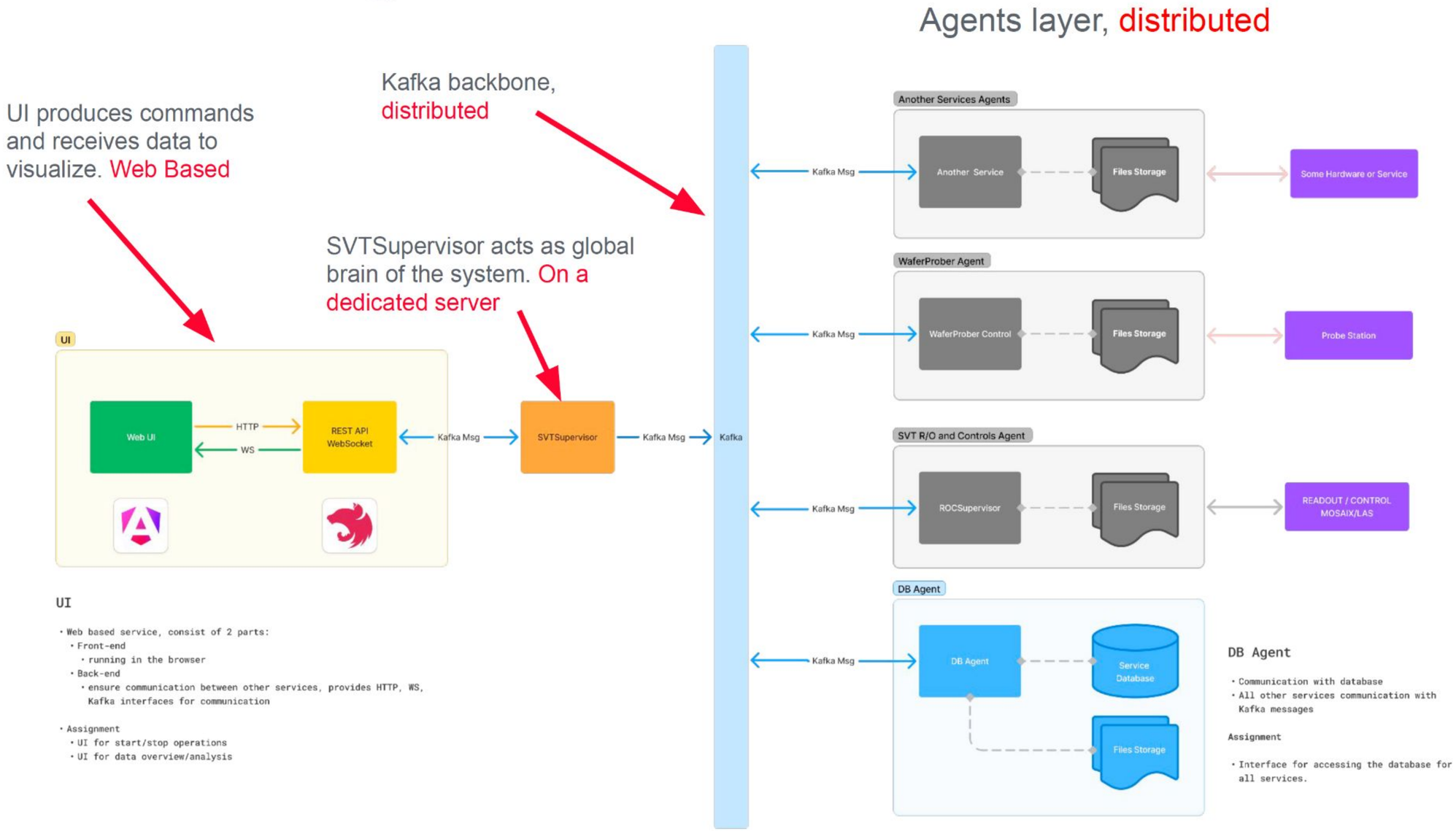
Starting from **MPW3**, it will be important to start to integrate testing into a unified test system, which will gradually evolve into the **final production software** used for wafer probing.

WP2 SW group mandate

- Create the general testing framework used to include each sub-component's testing software. The framework should be designed to be easily extended to the production software.
- Develop the needed control/test software for each subcomponent.
- Develop analysis tools for each step of the characterization.
- Assist the Readout and General Strategy task force.
- Interact with the WP responsible for the final software integration.

Testing SW status - general testing framework

SW Block Diagram



UI

- Web based service, consist of 2 parts:
  - Front-end
    - running in the browser
  - Back-end
    - ensure communication between other services, provides HTTP, WS, Kafka interfaces for communication
- Assignment
  - UI for start/stop operations
  - UI for data overview/analysis

DB Agent

- Communication with database
- All other services communication with Kafka messages

Assignment

- Interface for accessing the database for all services.

Summary

As mentioned, most of the tasks related to testing in the MPW1 and MPW2 phases are, as far as possible, already sufficiently covered in terms of people and equipment.

However, it is still necessary to gradually **clarify some testing parameters and the distribution of chips** for individual tests.

Also, the **funding for some tasks** (such as **carrier board production and assembly, irradiation**) is not yet 100% settled, but this will become clearer over time.

In any case, there does not seem to be anything that is urgently critical or that would cause significant delays at this stage.

Questions?

Topics for discussion:

➔ **irradiation parameters**
- dose up to 1 MRad or 10 MRad?,
- how many steps?
- temperature monitoring or cooling (to what temperature(s)?

➔ **SEE/SEU tests in a proton beam**
- NVG I^2C?
- beam energy

➔ **chip distribution**

➔ **anything else**

Irradiation testing discussion

12 chips + spares

- For test structures:
  - 10, 10^2, 10^3, 10^4 krad
  - 2 temperature settings @27°C and @0°C (technical solutions under eval: Peltier, Stirling, cryo-cooler)
  - Power ON and OFF states
  - 3x for statistics
- For blocks (NVBG):
  - Parallel testing?
  - Developing a bench-setup compatible with irradiation testing?

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Standard Temperature Range	-20, 27, 60, 105
Standard Radiation Range	0 - 1MRad in 100kRad steps

Chips powered during the irradiation, temperature monitoring (**cooling to 27C, ..??**)
0 - 1MRad in 100kRad steps **10krad, 100krad, 1Mrad, 10Mrad ??**