OAK RIDGE National Laboratory

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MOSAIX Mockup Board

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ORNL

U.S. DEPARTMENT OF ENERGY

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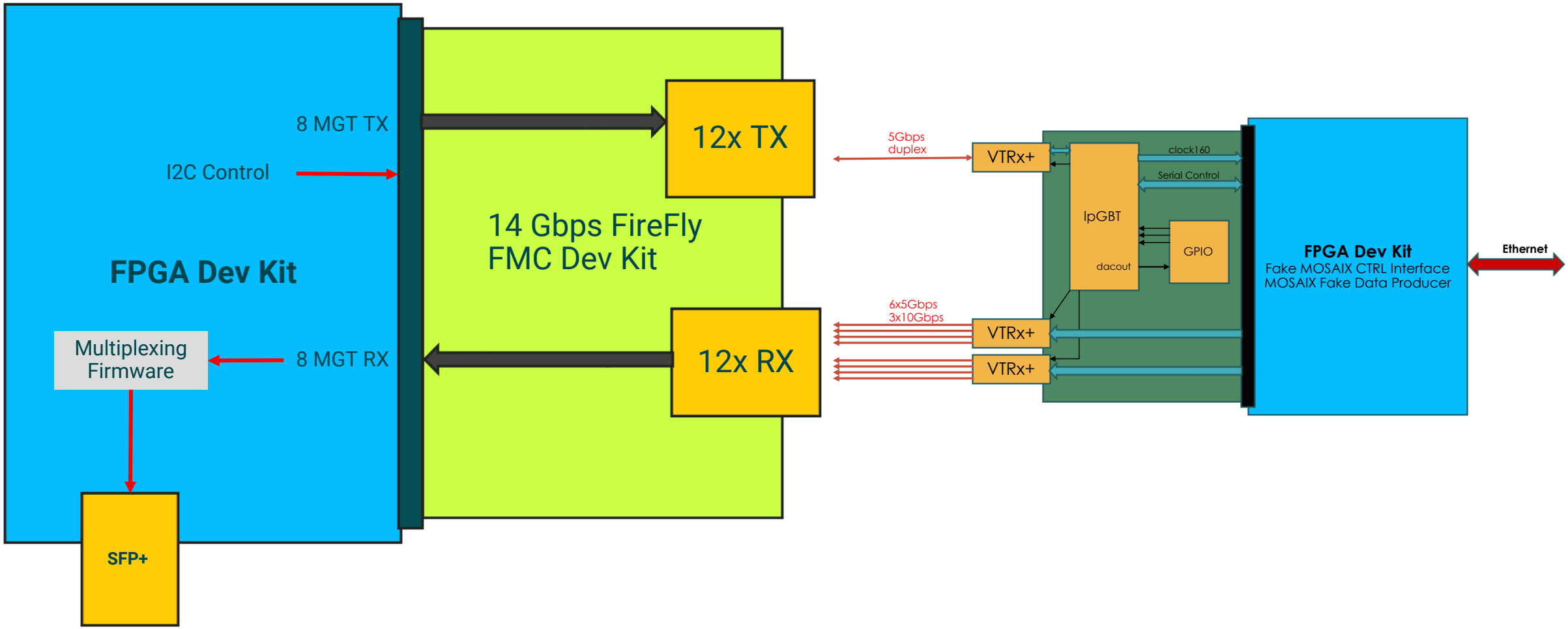
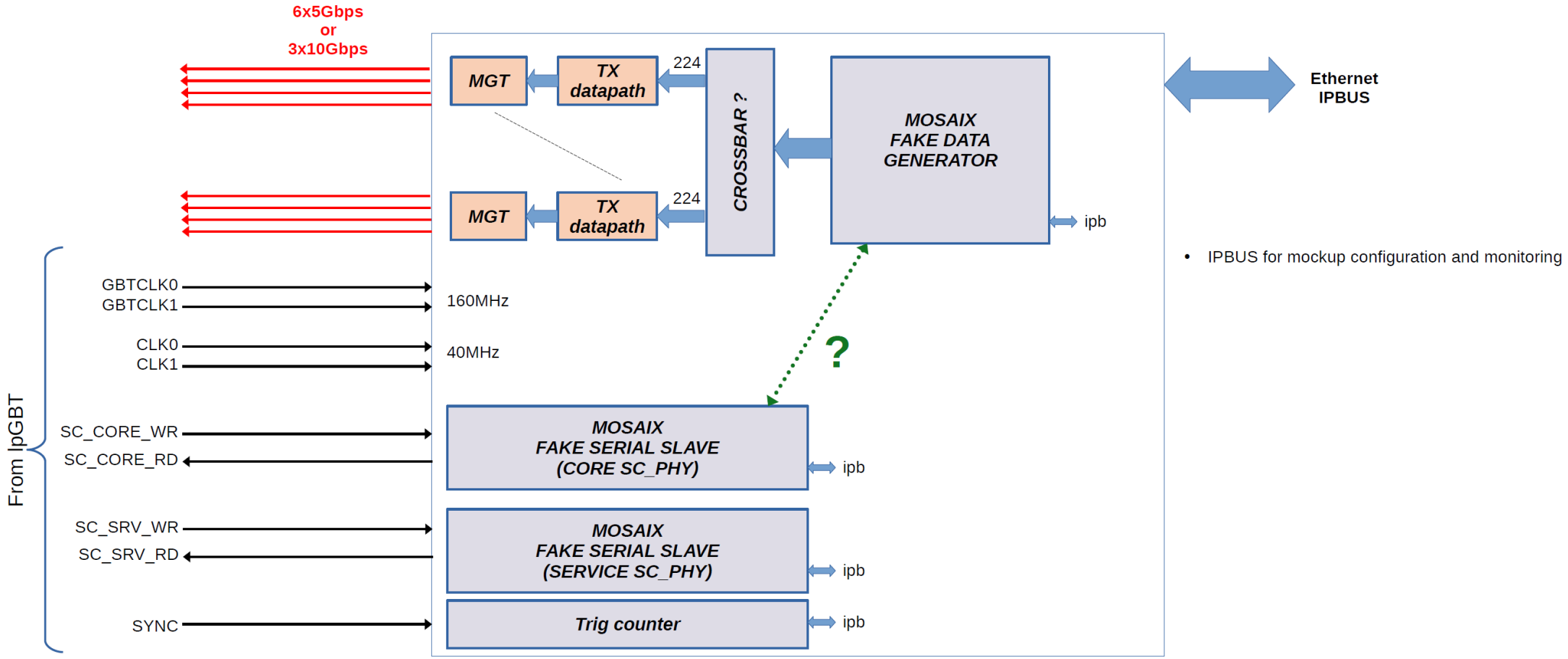
MOSAIX Hardware Mockup & Aggregator Board Prototypes

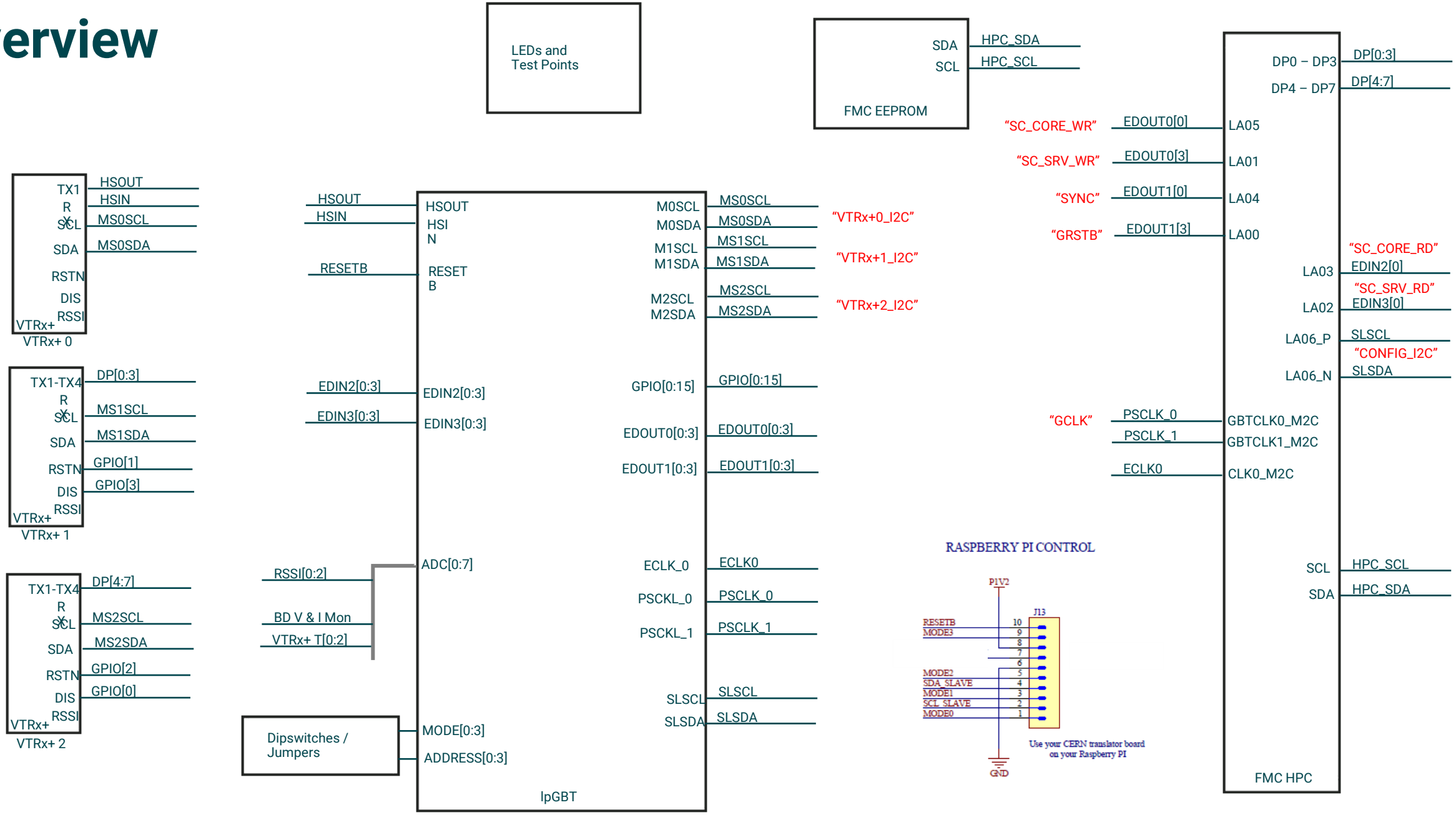


Mockup of MOSAIX with FPGA Firmware



- IPBUS for mockup configuration and monitoring

Overview

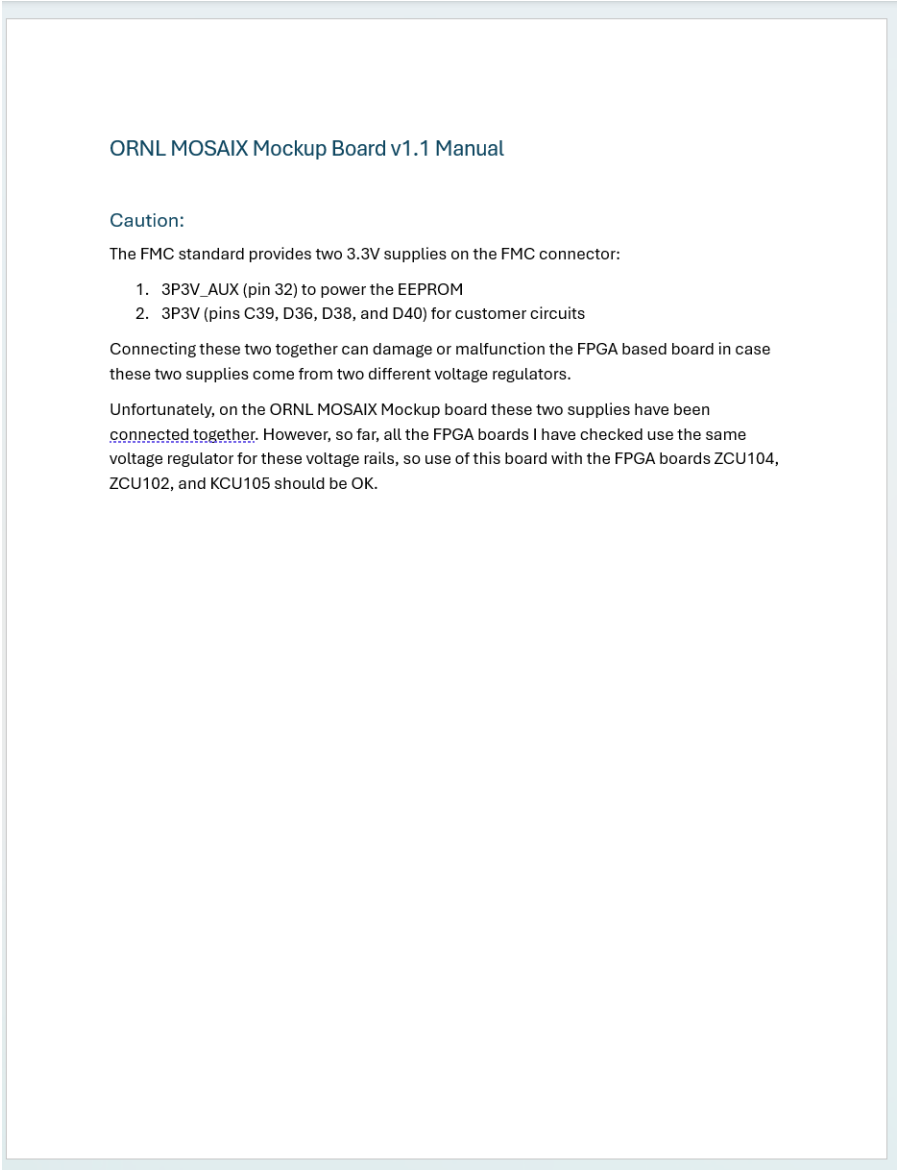

LEDs and Test Points
SDA
SCL
HPC_SDA
HPC_SCL
FMC EEPROM
DP0 – DP3
DP4 – DP7
DP[0:3]
DP[4:7]
"SC_CORE_WR"
EDOUT0[0]
LA05
"SC_SRV_WR"
EDOUT0[3]
LA01
"SYNC"
EDOUT1[0]
LA04
"GRSTB"
EDOUT1[3]
LA00
"SC_CORE_RD"
LA03
EDIN2[0]
"SC_SRV_RD"
LA02
EDIN3[0]
LA06_P
SLSCL
"CONFIG_I2C"
LA06_N
SLSDA
"GCLK"
PSCLK_0
PSCLK_1
GBTCLK0_M2C
GBTCLK1_M2C
ECLK0
CLK0_M2C
SCL
SDA
HPC_SCL
HPC_SDA
FMC HPC
TX1
R
SCL
SDA
RSTN
DIS
RSSI
VTRx+
VTRx+ 0
HSOUT
HSIN
MS0SCL
MS0SDA
TX1-TX4
VTRx+ 1
DP[0:3]
MS1SCL
MS1SDA
GPIO[1]
GPIO[3]
VTRx+ 2
DP[4:7]
MS2SCL
MS2SDA
GPIO[2]
GPIO[0]
HSOUT
HSIN
HSOUT
HSIN
RESETB
RESET B
M0SCL
M0SDA
M1SCL
M1SDA
M2SCL
M2SDA
MS0SCL
MS0SDA
MS1SCL
MS1SDA
MS2SCL
MS2SDA
"VTRx+0_I2C"
"VTRx+1_I2C"
"VTRx+2_I2C"
EDIN2[0:3]
EDIN3[0:3]
EDIN2[0:3]
EDIN3[0:3]
GPIO[0:15]
GPIO[0:15]
EDOUT0[0:3]
EDOUT1[0:3]
EDOUT0[0:3]
EDOUT1[0:3]
RSSI[0:2]
BD V & I Mon
VTRx+ T[0:2]
ADC[0:7]
ECLK_0
PSCKL_0
PSCKL_1
ECLK0
PSCLK_0
PSCLK_1
SLSCL
SLSDA
SLSCL
SLSDA
Dipswitches / Jumpers
MODE[0:3]
ADDRESS[0:3]
lpGBT
RASPBERRY PI CONTROL
P1V2
J13
RESETB
MODE3
MODE2
SDA_SLAVE
MODE1
SCL_SLAVE
MODE0
GND
Use your CERN translator board on your Raspberry PI

Mockup Board Content

- lpGBT v1
- HPC FMC Interface
- 3 VTRx+
    - 1 slow controls interface (1 TX, 1RX)
    - 2 data interface (4 TX each, 8 TX total)
- lpGBT GPIO interfaces:
    - RST & DISABLE to 2 Data VTRx+
    - Monitoring MUX
    - Debug LEDs
- lpGBT I2C (master) interfaces to 3 VTRx+
- LEDs for debugging
- FMC EEPROM (programmed to provide for 1.2V)
- lpGBT Mode & Address switches
- Power from FMC or separate connector
- Possibility for External Reference clock
- lpGBT ADC interfaces (with MUX):
    - V & I monitoring
    - VTRx+ RSSI
    - VTRx+ Thermistors
- 3 lpGBT clocks:
    - 2 PSCLK
    - 1 ECLK
- 4 ePort OUT: SC_CORE_WR, SC_SRV_WR, SYNC, RSTB
- 2 ePort IN: SC_CORE_RD, SC_SRV_RD
- piGBT compatible lpGBT Configuration Connector
- lpBGT Configuration from FMC connector

Production Status

- 2 Versions produced:
  - V1.0 produced 5 PCB, but only one was assembled
  - V1.0 had several issues that required a re-spin
  - V1.1 produced 5 boards
  - One further issue discovered (2 voltages connected together on FMC connector that shouldn't be), but should pose no problems with common eval boards
  - Other than that all 5 boards tested OK (so far)
- 2 boards distributed to Zhenyu and James G.
- First version of a Manual written



ORNL MOSAIX Mockup Board v1.1 Manual

Caution:

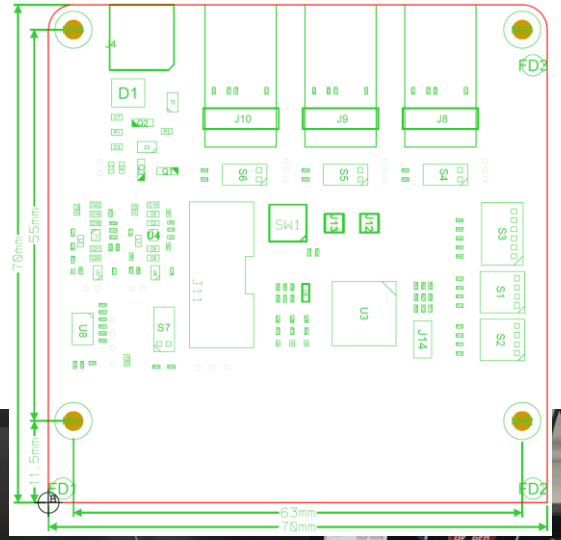
The FMC standard provides two 3.3V supplies on the FMC connector:

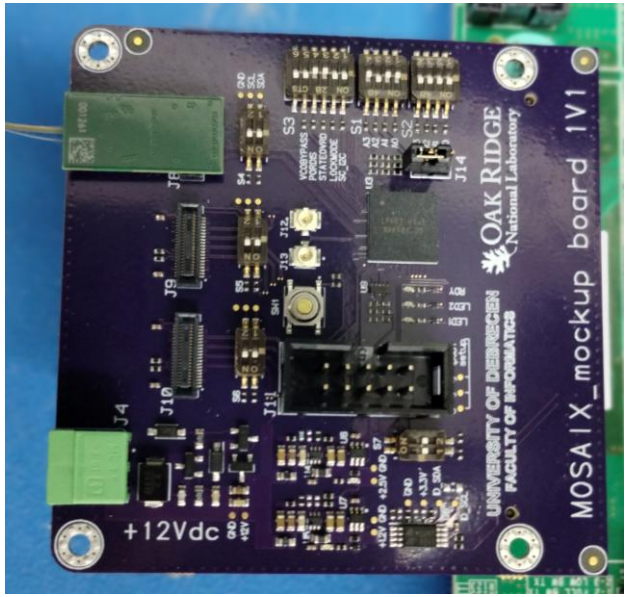
1. 3P3V_AUX (pin 32) to power the EEPROM
2. 3P3V (pins C39, D36, D38, and D40) for customer circuits

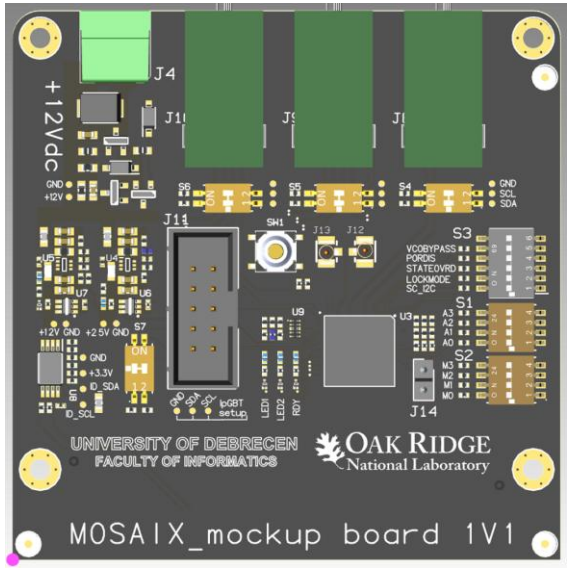
Connecting these two together can damage or malfunction the FPGA based board in case these two supplies come from two different voltage regulators.

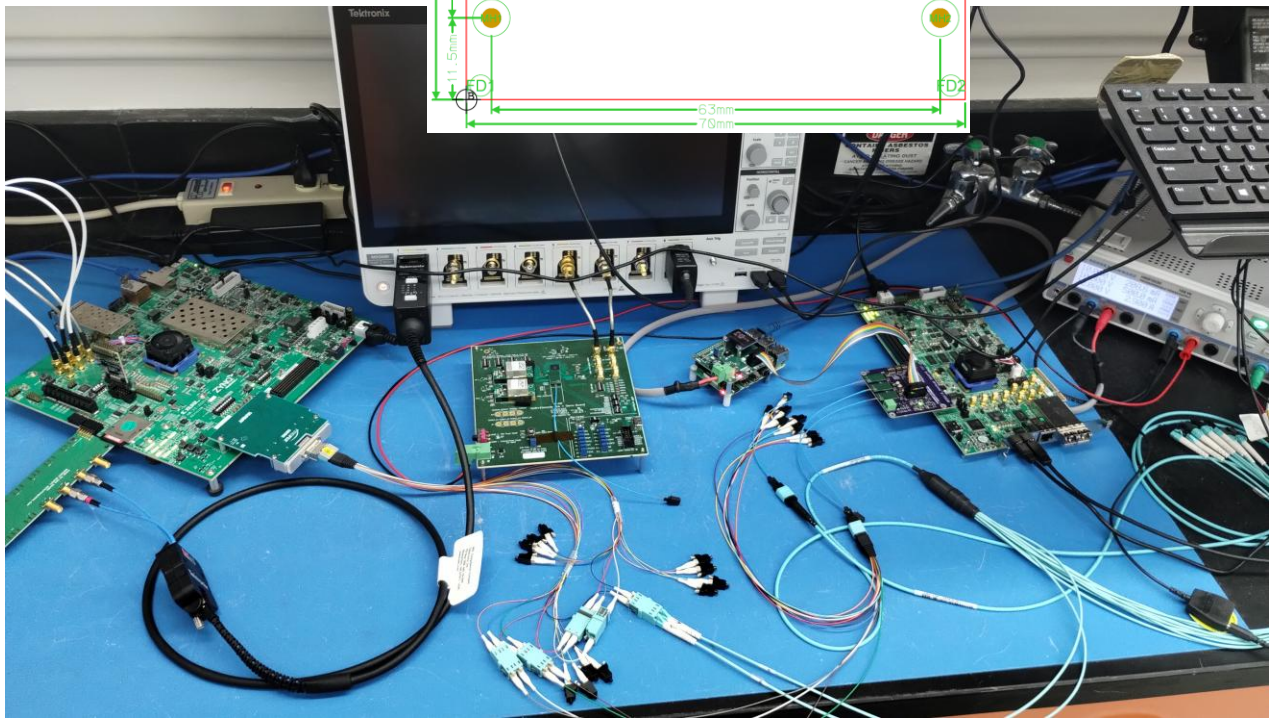
Unfortunately, on the ORNL MOSAIX Mockup board these two supplies have been connected together. However, so far, all the FPGA boards I have checked use the same voltage regulator for these voltage rails, so use of this board with the FPGA boards ZCU104, ZCU102, and KCU105 should be OK.

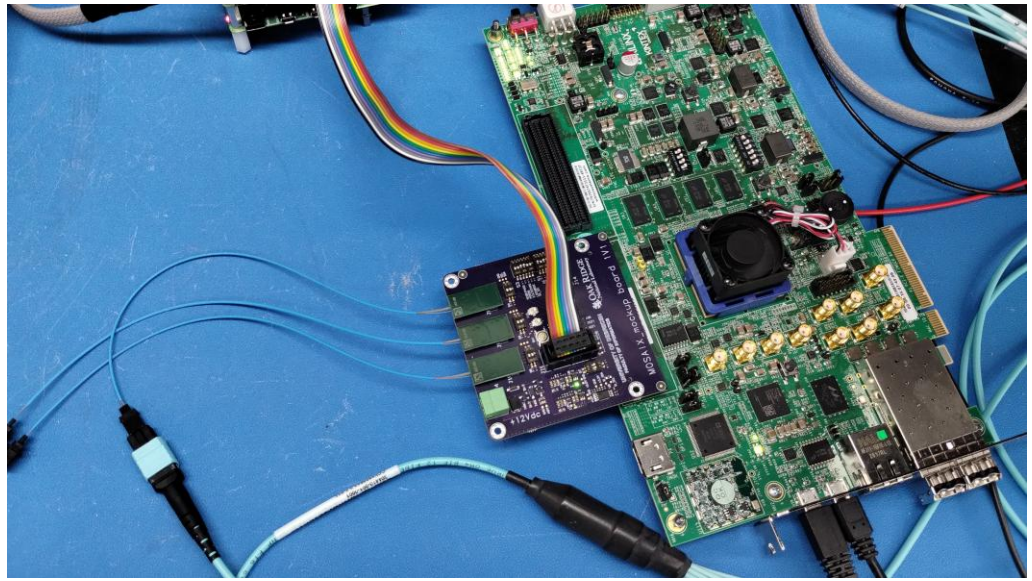
MOSAIX Mockup v1.1



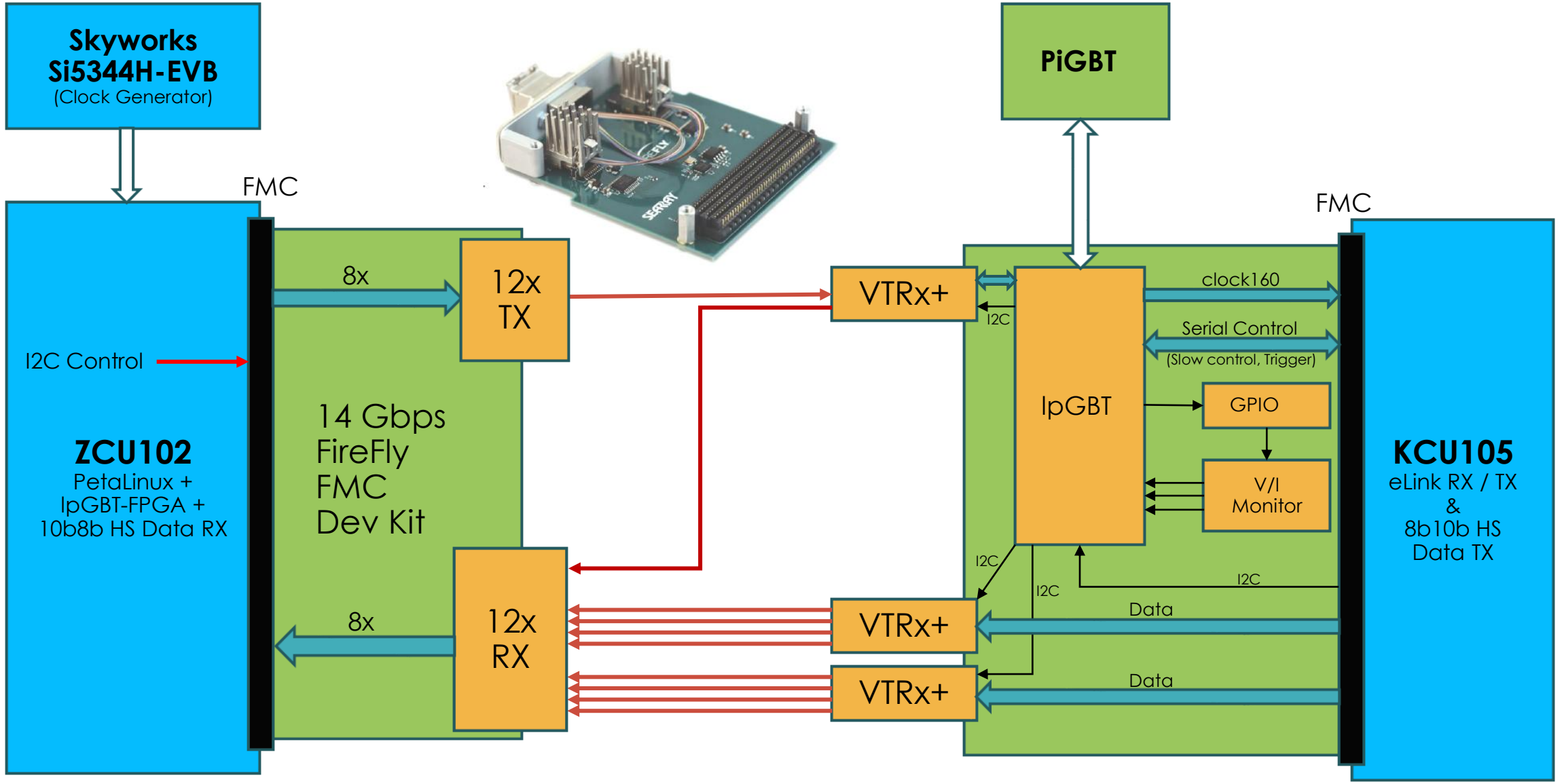








Test Setup at ORNL



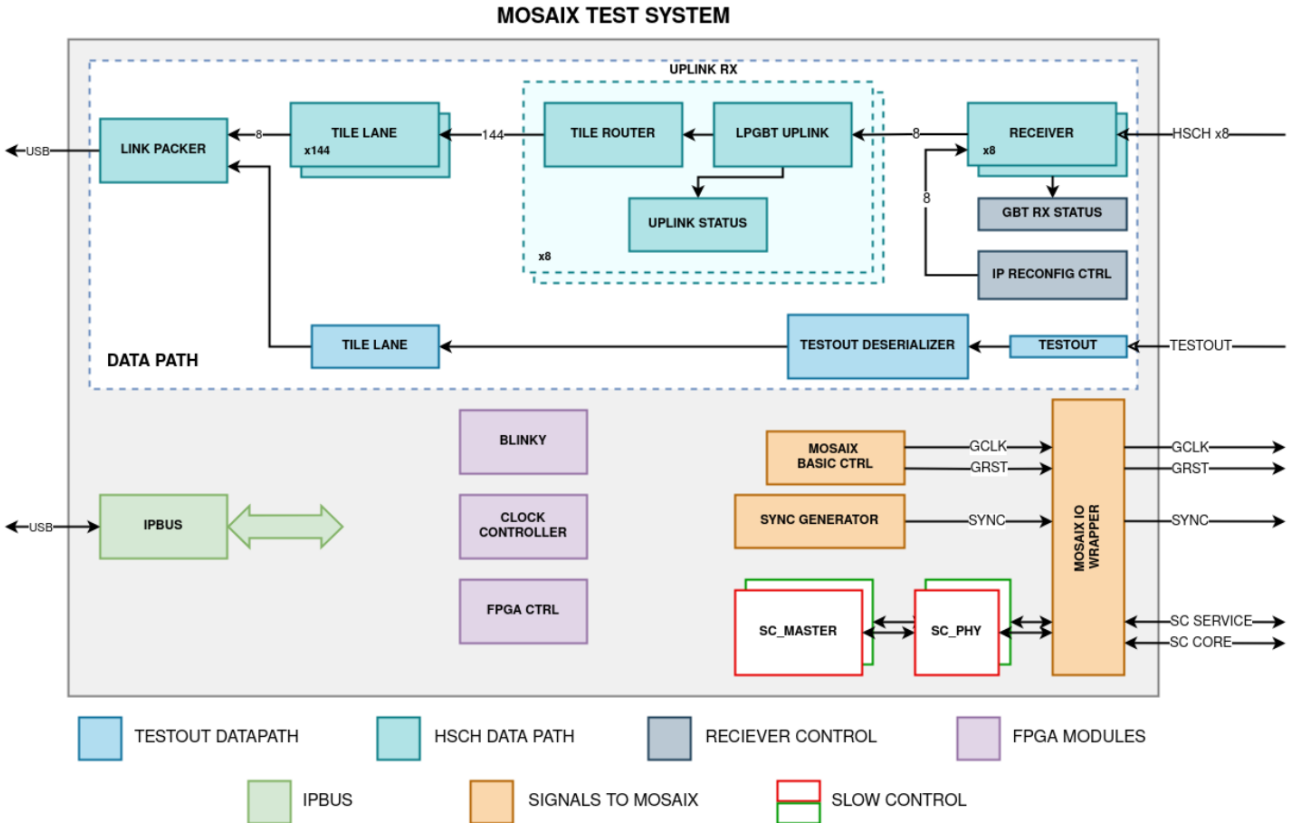
Test Procedures - so far

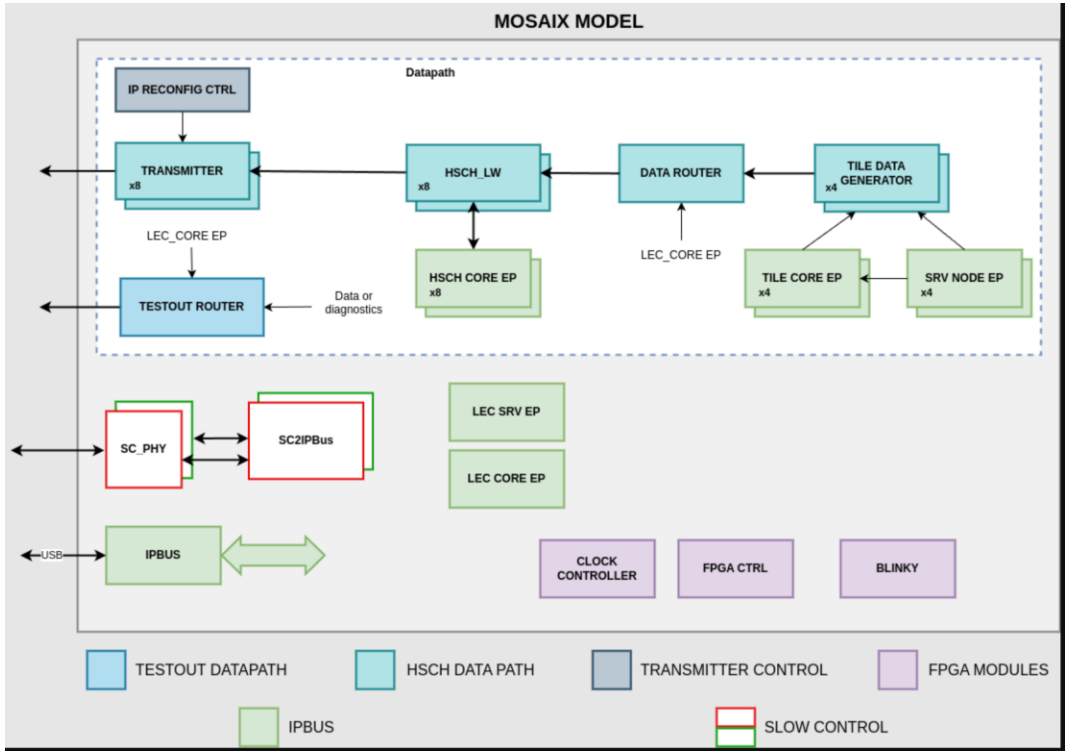
- Test Hardware Setup:
  - ZCU102 as FELIX or Fiber aggregation stand in
  - Samtec Optical FireFly FMC eval board
  - Si5344H to provide 320MHz reference clock (“GTU”)
  - PiGBT interface on Raspberry Pi
  - KCU105 as MOSAIX firmware mockup
  - High-speed Scope
  - Custom Fiber fanouts
- ZCU Firmware:
  - PetaLinux in PS, including “fpgautil” (for quickly changing PL firmware), I2C interface to FireFly, GPIO to FireFly, XVC server for Vivado debug interface (VIO & ILA) over net
  - PL running (ported) CERN lpgbt-FPGA firmware from CERN to interface to the slow control fibers, using FEC12, 10.24Gbps
  - PL firmware with 4 GTH 10b8b receivers, both VIO and ILA
  - PL firmware using CERN slow controls interface for control of the lpGBT registers vi the IC bits of the lpGBT frame
- KCU105 Firmware:
  - Simple ILA receiver for ePort OUT interfaces on FMC
  - HSSIO @320MHz for ePort out, configurable with either fixed pattern (programmable via VIO), or PRBS
  - 8 GTH 10b8b TX for VTRx+ HS Data with reference clock from lpGBT via FMC; configurable as either “comma”, fixed pattern, or PRBS (via VIO)
- Tests performed so far:
  - lpGBT connection (FEC12, 10.24Gbps)
  - Change of FireFly modulation
  - GPIO tests (MUX, LEDs)
  - I2C tests to VTRx+
  - ADC reads (voltages, currents, RSSI, thermistors)
  - ePort Tests (IN and OUT)
  - HS Data Tests @ 10.24 Gbps, 10b8b comma and fixed
  - VTRx+ configurations; enable all 4 TX

Mockup Board Future

- Need to implement ITS3 MOSAIX Test System Firmware from ITS3 WP3 (made available to us by ITS3 in gitlab, but without further support other than Wiki documentation)
- Consists of two distinct top-level designs:
    - **MOSAIX Test System (MTS):** the backend system for the MOSAIX, handling all of the MOSAIX interfaces like slow control, sync and high-speed data links
    - **MOSAIX Model (MM):** A functional emulation of the MOSAIX, used primarily for development and verification (encrypted)
- Currently targeted to an Enclustra eval board containing an Altera Aria10 FPGA; needs to be ported to our setup with the Mockup board connected to Xilinx evaluation boards
- Includes simulation targeted to RivieraPro Simulator
- Communication with MTS and MM provided using IPbus over USB (FX3)

Top Level Block Diagrams





USA: unit service-node addressing
GSA: global service-node addressing

UTA: unit tile addressing
GTA: global tile addressing