EIC-AncBRAIN:

A Slow Control & Communication Management System of AncASIC

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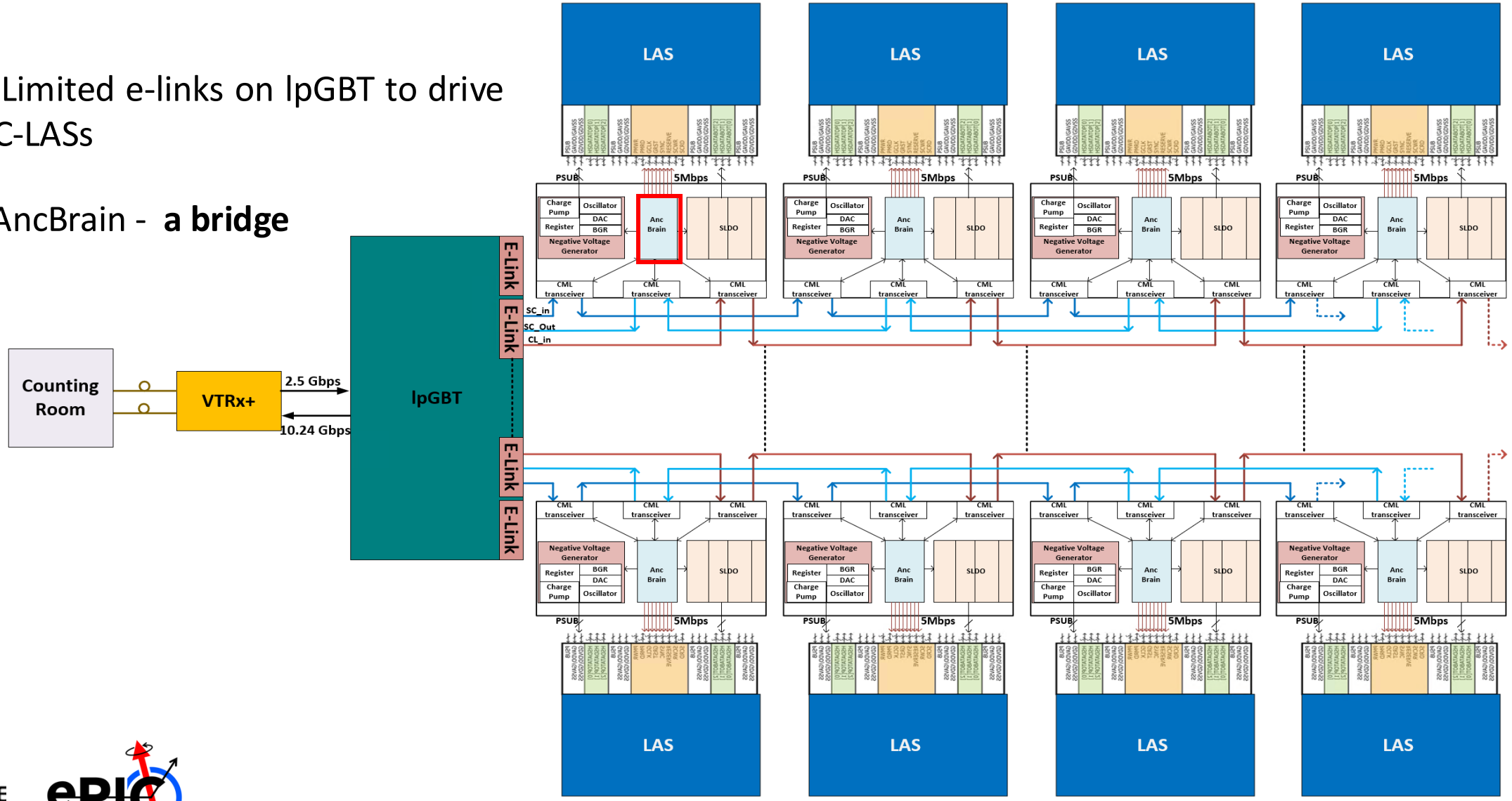
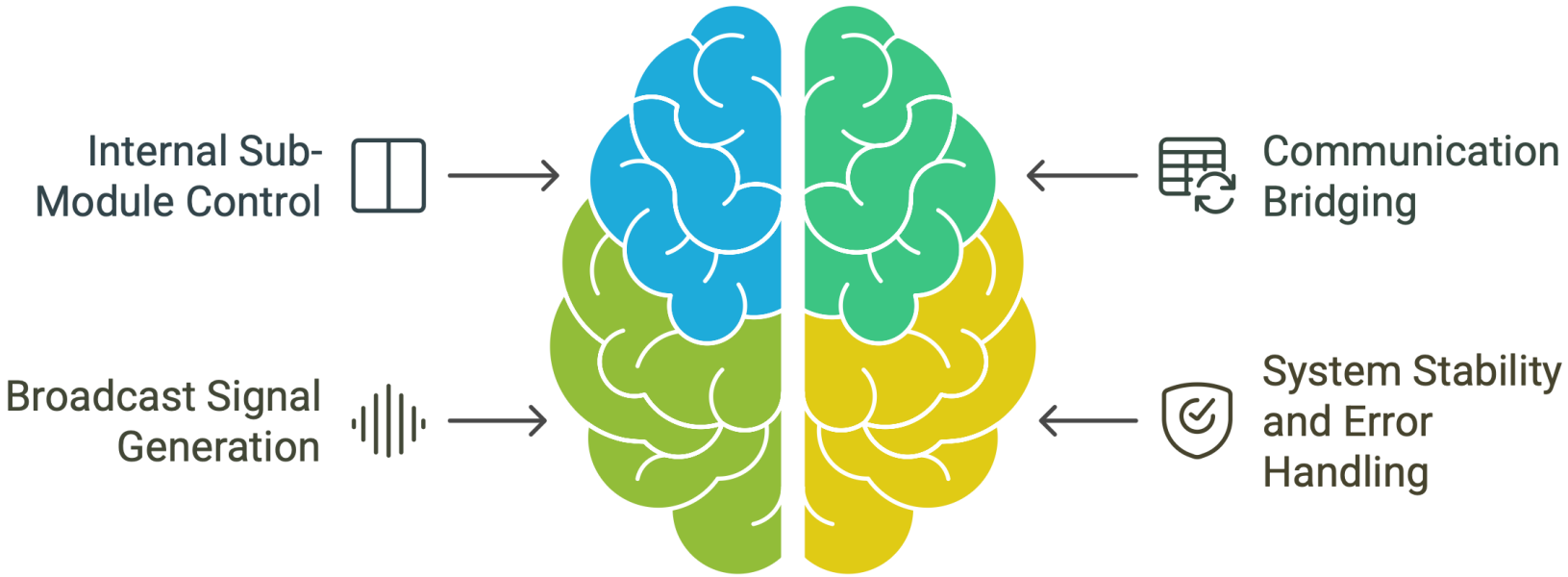
The Bottleneck

- **Challenge:** Limited e-links on lpGBT to drive multiple EIC-LASs
- **Solution:** AncBrain - **a bridge**



AncBrain: Key Functionalities

Core Operations Inside AncBrain



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Communication Interface

Talking to the world:

- **lpGBT Interface:**
  - Serial, Global Clock Synchronized
  - SC_in, SC_out
  - Protocol: Start/End Frame, Address, Data Type, Payload, CRC
- **Las Interface:**
  - Dedicated serial, 5 Mbps
  - Manchester encoding for reliability
  - LAS Protocol
- **GCLK Interface:**
  - Routing Global Clock (SCL) to LAS

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Interface Protocol Format

Communication Bridge

Transaction Breakdown

Table 1: Overall Transaction Structure

Field Name	Width (bits)	Description
Start of Frame	2	Predefined bit pattern to signal the beginning of a transaction("01")
Module Address	3	Identifies the target ANC module within the daisy chain (0-3); 000: Global Reset; 111: Global Sync
Data Type	2	00: Internal, 01: LAS Service Management, 10: LAS Core Management, 11: Reserved
40-bit Data Frame	40	Table ***2*** for details based on Data Type
Frame Checksum (CRC)	16	CRC-16 for error detection
End of Frame	2	Predefined bit pattern to signal the end of a transaction ("01")

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Interface Protocol Format

Communication Bridge

Payload Interpretation

Table 2: 40-bit Data Frame Formats

Field ID	Field Name	Width	Description
Internal	Submodule Identifier	4	Identifies the target sub-module within AncASIC(0-15 possible)
	R/W	2	Transaction type: Write or Read
	Register Address	8	Register address within the target sub-module
	Control/Data	4	Sub-module control data or internal signaling
	Parity	1	Transaction parity bit
	Stop	1	Internal signaling (or reserved)
	Unused	20	Reserved for future use
LAS(Service/Core Mgmt)	HDR	4	Fixed value (4'hA) indicating start of transaction
	R/W	2	0: WRITE_posted, 1: WRITE_non-posted, 2: READ
	EP_ADDR	8	Endpoint address
	REG_ADDR	8	Register address within the LAS module
	REG_DATA	16	Register write or read data

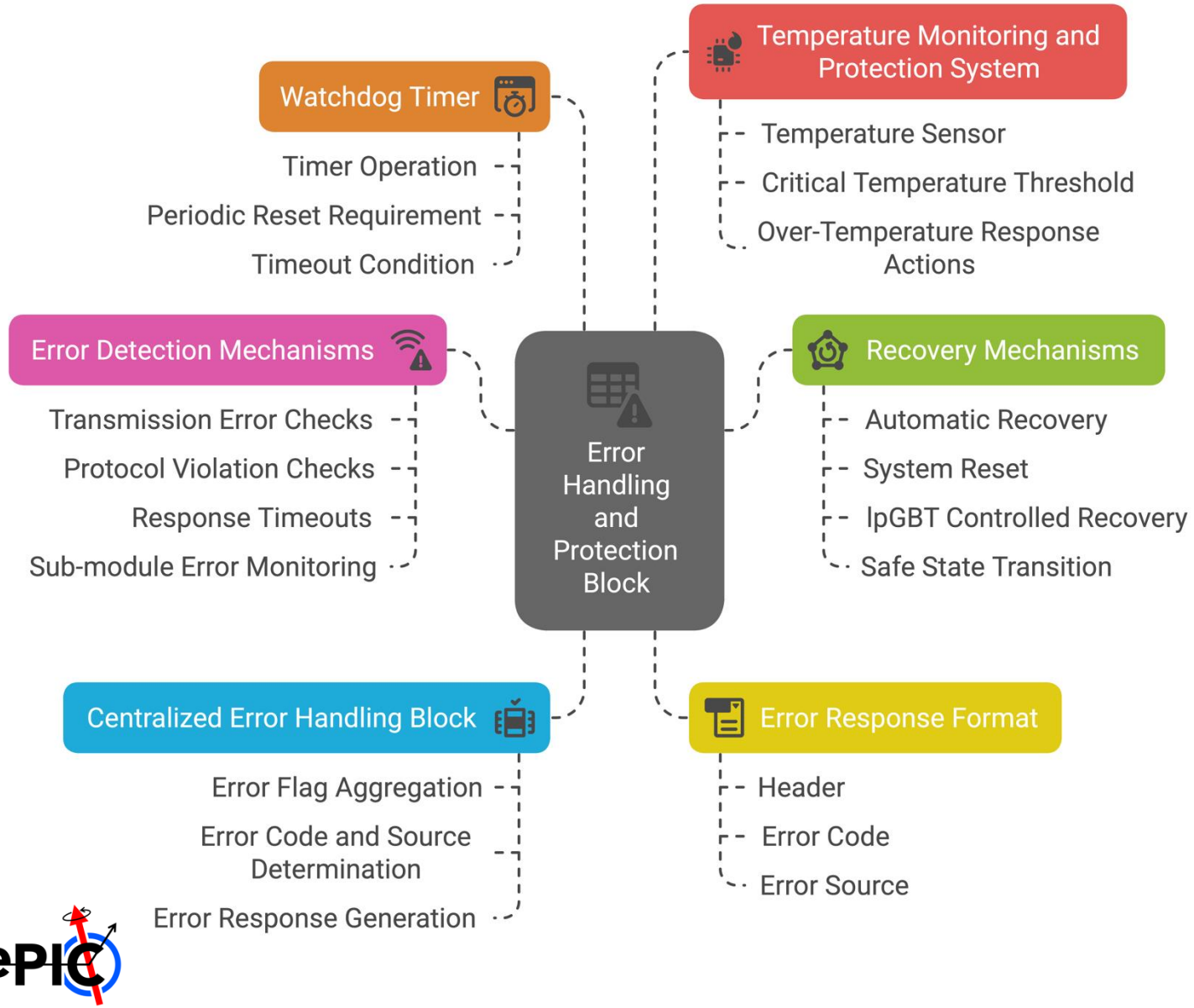
Broadcast Signal Generation

Synchronization and Efficiency

- **Dedicated Bit in "Module Address":** Broadcast signal indicator.
- **Digital Delay Line:** Fine-grained timing adjustment.
- **Broadcast Identification Patterns:**
  - 000: Global Reset
  - 111: Global Sync
  - 001-100: Module Addresses
- **Broadcast Detection:** Address Comparator triggers broadcast_command signal.

Error Handling & Protection

System Stability & Error Handling



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Sub-Module Control

Managing NBVG & SLDO:

- **Negative Bisa Voltage Generator (NBVG):**
  - Bias Voltage Generator
  - Configurable Bias level
  - Dedicated Registers
- **Shunt LDO (SLDO):**
  - Stable and regulated output voltage
  - Configurable Bits
  - Dedicated Registers

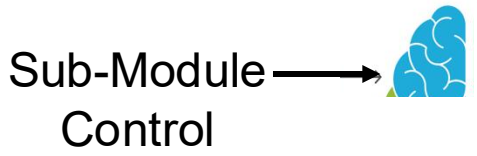


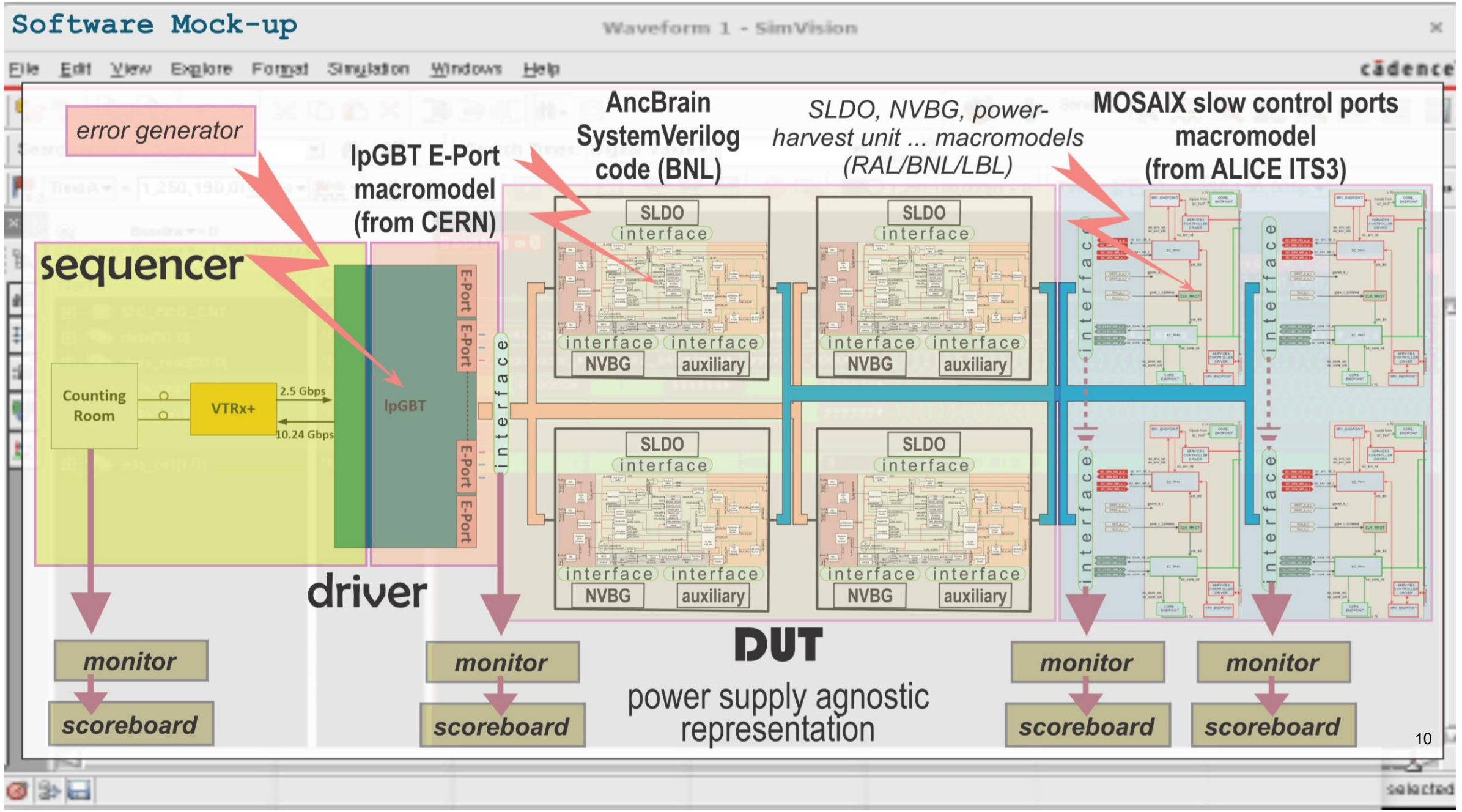
Table 3: Negative Bias Voltage Generator (NBVG)

Register Name	Address	Bit Field	Description
NBVG_CTRL	0x00	7-0	Output Voltage Setting (unsigned 8-bit value)
NBVG_MODE	0x01	1-0	Operating Mode: (00: Continuous, 01: Pulsed, 10: Standby, 11: Reserved)
		7-2	Reserved
NBVG_STATUS	0x02	0	Overcurrent Flag (1: Overcurrent)
		1	Over-Temperature Flag (1: Over-temperature)
		7-2	Reserved

Table 4: Shunt LDOs (assuming 4)

Register Name	Address	Bit Field	Description
SLDOx_CTRL	0x10 + (x-1)*4	5-0	Output Current Setting (unsigned 6-bitvalue)
		6	Enable (1: Enabled, 0: Disabled)
		7	Reserved
SLDOx_STATUS	0x11 + (x-1)*4	0	Overcurrent Flag (1: Overcurrent)
		1	Out-of-Regulation Flag (1: Out-of-regulation)
		7-2	Reserved

Design Verification – digital twin



Sub-Module Control

Sub-Module Control

Internal Module Config (Register Read)

```
--- Running Command Decoding Tests ---

[TEST] Starting Command Decoding Tests

[TEST] Test 1: Read from Register File
[TEST] Sending read command: submodule=REG_FILE, addr=0x05, parity=1
[TB Monitor] Time=1435000: Command valid_in asserted, cmd='{sof:'h1, module_address:'h2, data_type:'h0, payload:'h6814200000, crc:'habcd, eof:'h1}
[SCOREBOARD] REG_READ: [Mod:2][Sub:6][Addr:0x05] => 0x00
[SCOREBOARD] Added expected response for command type 0 at time 1435000
[SCOREBOARD] Added expected response for command: module=0x2, type=0
             1445000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
             1445000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
             1455000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
             1455000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
             1465000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             1465000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             1475000: [TB] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
             1475000: [DEBUG] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
             1475000: Register Read: submodule=SUBID_REG_FILE, addr=0x05, data=0x00
             1485000: [TB] FSM State change: ST_PROCESS_INT -> ST_SEND_RESPONSE
             1485000: [DUT DEBUG] Generating response for command type 0
             1485000: [DUT DEBUG] Generating response for command type 0, payload=0x0000000000
             1485000: [DEBUG] FSM State change: ST_PROCESS_INT -> ST_SEND_RESPONSE
[TB] Time=1485000: Response received from DUT: payload=0x0000000000
             1495000: [TB] FSM State change: ST_SEND_RESPONSE -> ST_IDLE_AncBrain
[TB Monitor] Time=1495000: Response valid_out asserted: payload=0x0000000000
[TB Monitor] Time=1495000: DUT.valid_resp_reg asserted
[SCOREBOARD] Time=1495000: Received response: payload=0x0000000000, status=0x0
[SCOREBOARD] Response Check at time 1495000:
  Command type: 0
  Expected: payload=0x0000000000, status=0x0
  Actual  : payload=0x0000000000, status=0x0
[INFO][SCORE] PASS: Response matches expected value at time 1495000
[MONITOR] Time=1495000: Response payload=0000000000, CRC=5a5a
[INFO][RESP] Time=1495000: Response valid_out asserted: payload=0x0000000000
             1495000: [DEBUG] FSM State change: ST_SEND_RESPONSE -> ST_IDLE_AncBrain
[TEST] Received read response: payload=0x0000000000
```

```
**** SCOREBOARD RESULTS ****
Pass count     : 58
Fail count     : 0
Unexpected     : 0
Total checked  : 58
Pass rate      : 100.00%
```

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Sub-Module Control

Sub-Module Control

Internal Module Config (Register Write)

```
[TEST] Test 2: Write to Register File
[TEST] Sending write command: submodule=REG_FILE, addr=0x20, data=0x5, parity=0
[TB Monitor] Time=1615000: Command valid_in asserted, cmd='{sof:'h1, module_address:'h2, data_type:'h0, payload:'h6481400000, crc:'habcd, eof:'h1}
[INFO][REG] REG_WRITE: [Mod:2][Sub:6][Addr:0x20] = 0x05 (Reg File Addr 0x20)
[SCOREBOARD] REG_WRITE: [Mod:2][Sub:6][Addr:0x20] = 0x05
[SCOREBOARD] Added expected response for command type 0 at time 1615000
[SCOREBOARD] Added expected response for command: module=0x2, type=0
             1625000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
             1625000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
             1635000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
             1635000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
             1645000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             1645000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             1655000: [TB] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
             1655000: [TB] Register Write: submodule=SUBID_REG_FILE, addr=0x20, data=0x05
             1655000: [DEBUG] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
             1655000: Register Write: submodule=SUBID_REG_FILE, addr=0x20, data=0x05
             1665000: [TB] FSM State change: ST_PROCESS_INT -> ST_SEND_RESPONSE
             1665000: [DUT DEBUG] Generating response for command type 0
             1665000: [DUT DEBUG] Generating response for command type 0, payload=0x0000000001
             1665000: [DEBUG] FSM State change: ST_PROCESS_INT -> ST_SEND_RESPONSE
[TB] Time=1665000: Response received from DUT: payload=0x0000000001
             1675000: [TB] FSM State change: ST_SEND_RESPONSE -> ST_IDLE_AncBrain
[TB Monitor] Time=1675000: Response valid_out asserted: payload=0x0000000001
[TB Monitor] Time=1675000: DUT.valid_resp_reg asserted
[SCOREBOARD] Time=1675000: Received response: payload=0x0000000001, status=0x0
[SCOREBOARD] Response Check at time 1675000:
  Command type: 0
  Expected: payload=0x0000000001, status=0x0
  Actual  : payload=0x0000000001, status=0x0
[INFO][SCORE] PASS: Response matches expected value at time 1675000
[MONITOR] Time=1675000: Response payload=0000000001, CRC=5a5a
[INFO][RESP] Time=1675000: Response valid_out asserted: payload=0x0000000001
             1675000: [DEBUG] FSM State change: ST_SEND_RESPONSE -> ST_IDLE_AncBrain
[TEST] Received write response: payload=0x0000000001
```

```
========================================
WRITE TEST SUMMARY:
  Patterns sent:     25
  Patterns verified: 25
  Test result:       PASSED
========================================

 Simple Improved Register Test Complete


=== Dumping Register Database After Write Tests ===

=== REGISTER DATABASE DUMP ===
Time: 6185000
  [Module:2][NBVG][0x00000000] = 0x0f (writes:4, last_access:1315000)
  [Module:2][SLD00][0x00000000] = 0x0f (writes:4, last_access:2335000)
  [Module:2][SLD01][0x00000000] = 0x0e (writes:3, last_access:2845000)
  [Module:2][SLD02][0x00000000] = 0x0d (writes:3, last_access:3355000)
  [Module:2][SLD03][0x00000000] = 0x0f (writes:3, last_access:3865000)
  [Module:2][DELAY][0x00000000] = 0x0f (writes:3, last_access:4375000)
  [Module:2][TEMP_SENSOR][0x00000000] = 0x0f (writes:3, last_access:4885000)
Total initialized registers: 32
=== END DATABASE DUMP ===
```

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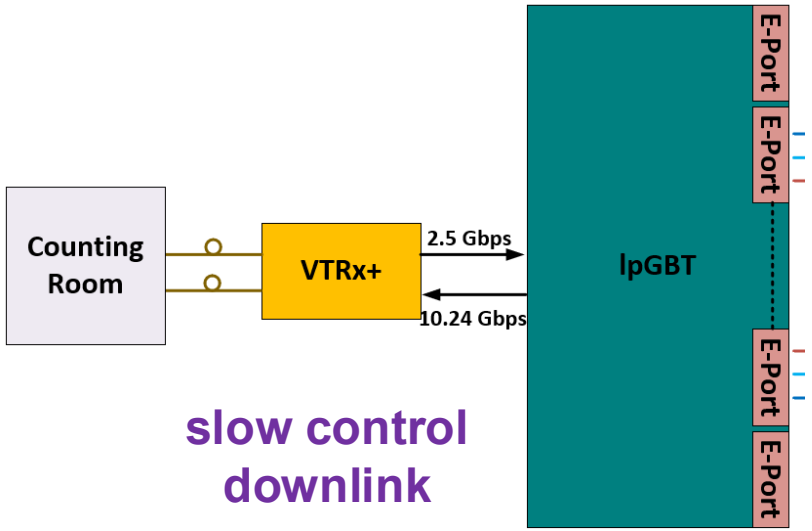
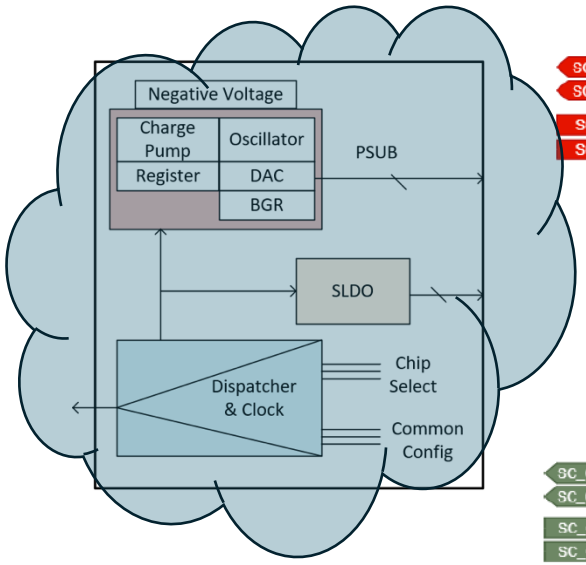
LAS Interface

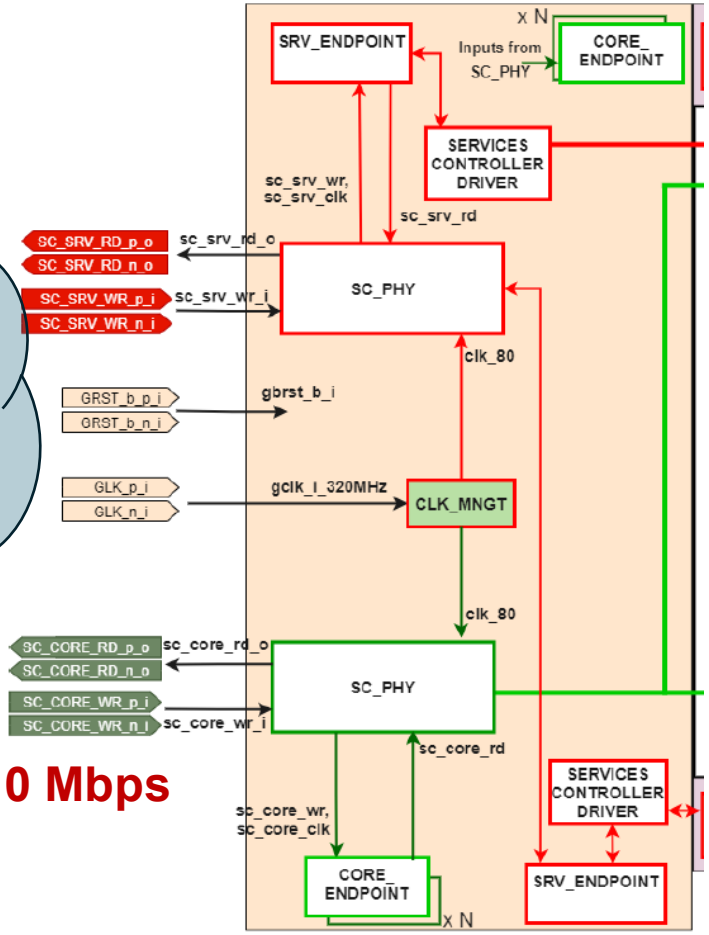
Communication Bridge



slow control downlink

AncASIC





5-10 Mbps

MOSAIX / EIC-LAS interface

MOSAIX (all diff. CLPS):
Clock - input
Reset - input
Sync - input
2× slow control – input/output
Services management
Core management
1× reserved

– +HS Data (all differential):
8× high-speed channels (4 top, 4 bottom)

MOSAIX interface needs to be formalized

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LAS Emulator

Communication Bridge

LAS: Non-Posted Service Management (Write)

```
================================================================
[Time 145000] [TEST] Starting Manchester test: Test Case 1: Non-posted Write (Service, Manchester Mode)
[MANCH CMD] HDR:a, RW:00, EP_ADDR:10, REG_ADDR:20, REG_DATA:1234, PARITY:1, STOP:1
[MANCH ENCODED] 01100110 10100101 10101001 10101010 10100110 10101010 10101001 10100110 10100101 10011010
[Time 215000] [SLOW_CLK] Rising edge detected (Edge 1).
[Time 245000] [TEST] Asserting manch_valid to trigger command capture
[Time 245000] [DEBUG] Manchester command valid detected
[Time 245000] [LAS] Manchester command received and decoded
[Time 255000] [STATE] Transition: IDLE -> PROCESS
[Time 255000] [STATE] PROCESS: Processing command.
[Time 255000] [MONITOR] Service Write: Reg 0x20 updated to xxxx
[Time 255000] [RECV] Command: HDR=a, RW=00, EP=10, REG=20, DATA=1234
[Time 255000] [PROC] Non-posted write to reg 0x20: 0x1234
[Time 265000] [STATE] Transition: PROCESS -> DELAY
[Time 265000] [STATE] DELAY: Delaying before response.
[EXPECT] Non-posted Write: Expect response (ACK) and register update.
[Time 365000] [WAIT] Waiting for response completion... (Timeout = 3650 cycles)
[Time 365000] [RESP] Response ready, transmitting on Service channel
[Time 375000] [STATE] Transition: DELAY -> RESPOND
[Time 375000] [STATE] RESPOND: Transmitting 80-bit response.
[Time 375000] [RESP] Starting response with preamble on SERVICE channel
[Time 375000] [RESP] Starting response transmission, setting valid_rx=1
[Time 385000] [RESP] Response transmission started on Service channel
[Time 385000] [RESP] Starting response with preamble on SERVICE channel
[Time 385000] [RESP] Starting response transmission, setting valid_rx=1
[Time 395000] [RESP] Starting response with preamble on SERVICE channel
```

```
Time 32225000] [RESP] Transmitted bit 80: 0
Time 32505000] [WAIT] Still waiting... (3213/3650 cycles)
Time 32625000] [RESP] Transmitting bit 81 of 80 on Service channel
Time 32625000] [RESP] Response transmission complete, setting response_complete=1
Time 32635000] [STATE] Transition: RESPOND -> IDLE
Time 32635000] [STATE] IDLE: Ready for Manchester command.
Time 32635000] [RESP] Response complete detected.
Time 33025000] [RESP] Transmitting bit 81 of 80 on Service channel
Time 33285000] [TEST] Completed Manchester test: Test Case 1: Non-posted Write (Service, Manchester Mode)
================================================================
```

LAS: Posted Core Management (Write)

```
================================================================
[Time 201085000] [TEST] Starting Manchester test: Test Case 8: Manchester Posted Write (Core)
[MANCH CMD] HDR:7, RW:01, EP_ADDR:80, REG_ADDR:35, REG_DATA:def0, PARITY:1, STOP:1
[MANCH ENCODED] 10010101 10010101 01101010 10101010 10100101 10011001 01011001 01010110 01010101 10101010
[Time 201185000] [TEST] Asserting manch_valid to trigger command capture
[Time 201185000] [DEBUG] Manchester command valid detected
[Time 201185000] [LAS] Manchester command received and decoded
[Time 201195000] [RESP] Response transmission completed
        Duration: 33070000, Channel: Service
[Time 201195000] [STATE] Transition: IDLE -> PROCESS
[Time 201195000] [STATE] PROCESS: Processing command.
[Time 201195000] [MONITOR] Core Write: Reg 0x35 updated to xxxx
[Time 201195000] [RECV] Command: HDR=7, RW=01, EP=80, REG=35, DATA=def0
[Time 201195000] [PROC] Posted write to reg 0x35: 0xdef0
[Time 201205000] [STATE] Transition: PROCESS -> IDLE
[Time 201205000] [STATE] IDLE: Ready for Manchester command.
[EXPECT] Posted Write: No response expected; only register update.
[Time 201305000] [INFO] Posted write issued; no response expected.
[Time 202405000] [TEST] Completed Manchester test: Test Case 8: Manchester Posted Write (Core)
================================================================
```

Test Summary

```
=================== TESTING COMPLETE ===================
[Time 202605000] [SUMMARY] Simulation finished.

============================================================
                      TEST SUMMARY
============================================================
Total Tests Run:  8
Passed:           8
Failed:           0

Success Rate: [==================================================] 100.0% (8/8)

============== DETAILED TEST RESULTS ================
Test 1: Non-posted Write (Service)        : PASS
Test 2: Read Operation (Service)          : PASS
Test 3: Posted Write (Core)               : PASS
Test 4: Read Operation (Core)             : PASS
Test 5: Invalid Parity Error Injection    : PASS
Test 6: Slow Clock Timing Verification    : PASS
=====================================================

TEST RESULT: PASS - All tests completed successfully!
============================================================


============= REGISTER FILE CONTENTS ==============
Service EP 0x10, Reg 0x20: 0x1234
Service EP 0x10, Reg 0x25: 0xabcd
Core EP 0x80, Reg 0x30: 0x5678
Core EP 0x80, Reg 0x35: 0xdef0
=====================================================

Simulation complete via $finish(1) at time 202805 NS + 0
./rtl/verification/tb_las_physical_emulator.sv:439      $finish;
xcelium>
```

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LAS Communication

```
[DRIVER] ============ LAS Service Non-Posted WRITE Test ============
[DRIVER] Test registration requested: LAS Service non-posted WRITE operation
[DRIVER] Starting LAS Service Non-Posted WRITE Test at time 855000
[DRIVER] Creating non-posted WRITE transaction to EP=0x12, Reg=0x34, Data=0x5678
[DRIVER DEBUG] LAS frame fields before packing:
  hdr=0xa (4 bits)
  rw=0x00 (2 bits)
  ep_addr=0x12 (8 bits)
  reg_addr=0x34 (8 bits)
  reg_data=0x5678 (16 bits)
  parity=1 (1 bit)
  stop=1 (1 bit)
[DRIVER DEBUG] Packed payload using las_pkg: 0xa048d159e3
[DRIVER] Non-posted WRITE transaction prepared: payload=0xa048d159e3
[DRIVER] Sending non-posted WRITE command to DUT
[TB] Registered test with scoreboard: LAS Service non-posted WRITE operation
Time=865000: [FSM_DEBUG] ST_IDLE -> ST_RECEIVE_HEADER (new command, will be buffered)
875000: [INFO|LAS ] [SCOREBOARD] LAS Command: WRITE (non-posted) on SERVICE channel
[SCOREBOARD] LAS COMMAND DETAILS: hdr=0xa, rw=0x00, ep_addr=0x12, reg_addr=0x34, data=0x5678
[SCOREBOARD] LAS WRITE: [Type: SRV][EP:0x12][Reg:0x34] = 0x5678 (RW=00 non-posted)
[SCOREBOARD] Expected response payload: 0xa048d00005
[SCOREBOARD] DEBUG: Final predict_response result: resp_type=1, response_data=0xa048d00005
Time=875000: [FSM_DEBUG] Command buffered: data_type=0x1, is_broadcast=0
[DRIVER] Monitoring LAS interface for command forwarding...
[DRIVER] Verifying Manchester encoding and 5MHz timing...
[DRIVER] Waiting for LAS response generation...
[DRIVER] Waiting for AncBrain to forward response back to control room...
             885000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
             885000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
Time=885000: [FSM_DEBUG] ST_ADDRESS_CHECK -> ST_DECODE_DATA (buffer_valid=1, data_type=0x1)
             895000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
             895000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
Time=895000: [FSM_DEBUG] ST_DECODE_DATA -> ST_PROCESS_LAS (data_type=0x1)
             905000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             905000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
             915000: [TB] FSM State change: ST_DECODE_DATA -> ST_PROCESS_LAS
             915000: [DUT DEBUG] Clearing LAS response latch
             915000: [DEBUG] FSM State change: ST_DECODE_DATA -> ST_PROCESS_LAS
             925000: [TB] FSM State change: ST_PROCESS_LAS -> ST_WAIT_LAS_RESP
             925000: [DEBUG] FSM State change: ST_PROCESS_LAS -> ST_WAIT_LAS_RESP
935000: [INFO|LAS |LAS_CTRL] Starting Manchester encoding (SERVICE channel)
             945000: [LAS MANCH ENC] Starting to encode latched data: 0xa048d159e3
             945000: [LAS MANCH ENC] Manchester encoding in progress
945000: [INFO|LAS |LAS_CTRL] Starting Manchester encoding (SERVICE channel)
             955000: [LAS MANCH ENC] Encoding complete: 0x66aa9a6a59a9996956a5
[Time 975000] [LAS EMUL] Manchester command valid detected (rising edge)
985000: [INFO|LAS |LAS_CTRL] Transmitting frame: 0xa048d159e3, Encoded: 0xcd5534d4b35332d2ad4a
[Time 995000] [RECV: LAS EMUL] Command: HDR=a, RW=00, EP=12, REG=34, DATA=5678
[Time 995000] [LAS EMUL WRITE] Non-posted write success, returning code 0x0001
[Time 995000] [LAS EMUL] NON-POSTED WRITE detected, preparing response, storing data=0x5678
2575000: [INFO|LAS |LAS_CTRL] Transmission complete, waiting for response for non-posted write or READ operation
[Time 2585000] [LAS EMUL DEBUG] Response frame details:
  - Header:    a
  - RW:        00
  - EP Addr:   12
  - Reg Addr:  34
  - Reg Data:  0001
  - Parity:    0
  - Stop:      1
  - 40-bit packed: a048d00005
  - 80-bit Manchester (calculated for TX): 66aa9a6a59aaaaaaaa99
```

Communication Bridge

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LAS Communication

Communication Bridge

```
[Time 2585000] [RESP: LAS EMUL] Response ready (using 8-half-bit preamble 10011001), delaying 10 cycles before transmit on Service channel
2595000: [INFO|LAS |LAS_CTRL] Waiting for response, service_channel=1
[Time 2695000] [RESP: LAS EMUL] Delay complete, starting response on Service channel
[Time 2705000] [RESP: LAS EMUL] Starting response transmission (88 half-bits inc. preamble), valid_rx=1
2745000: [LAS EMUL RESP] Preamble half-bit 1 -> 1 (on  rising edge)
2755000: [INFO|LAS |LAS_CTRL] Service RX transition detected: 0 -> 1
2815000: [INFO|LAS |LAS_CTRL] Debounce complete. Captured first preamble half-bit: 1. Entering SYNC for 7 more half-bits.
2835000: [INFO|LAS |LAS_CTRL] SYNC state: processing 7 more preamble half-bits.
2845000: [LAS EMUL RESP] Preamble half-bit 2 -> 0 (on falling edge)
2895000: [INFO|LAS |LAS_CTRL] Sampled half-bit 0, Next Preamble buffer state: 01000000, run_in_counter (before dec):  7
2945000: [LAS EMUL RESP] Preamble half-bit 3 -> 0 (on  rising edge)
2995000: [INFO|LAS |LAS_CTRL] Sampled half-bit 0, Next Preamble buffer state: 00100000, run_in_counter (before dec):  6
3045000: [LAS EMUL RESP] Preamble half-bit 4 -> 1 (on falling edge)
3095000: [INFO|LAS |LAS_CTRL] Sampled half-bit 1, Next Preamble buffer state: 10010000, run_in_counter (before dec):  5
3145000: [LAS EMUL RESP] Preamble half-bit 5 -> 1 (on  rising edge)
3195000: [INFO|LAS |LAS_CTRL] Sampled half-bit 1, Next Preamble buffer state: 11001000, run_in_counter (before dec):  4
3245000: [LAS EMUL RESP] Preamble half-bit 6 -> 0 (on falling edge)
3295000: [INFO|LAS |LAS_CTRL] Sampled half-bit 0, Next Preamble buffer state: 01100100, run_in_counter (before dec):  3
3345000: [LAS EMUL RESP] Preamble half-bit 7 -> 0 (on  rising edge)
3395000: [INFO|LAS |LAS_CTRL] Sampled half-bit 0, Next Preamble buffer state: 00110010, run_in_counter (before dec):  2
3445000: [LAS EMUL RESP] Preamble half-bit 8 -> 1 (on falling edge)
3495000: [INFO|LAS |LAS_CTRL] Sampled half-bit 1, Next Preamble buffer state: 10011001, run_in_counter (before dec):  1
3495000: [INFO|LAS |LAS_CTRL] Preamble processing complete (MATCH: 10011001). Moving to RECEIVE state. Next edge will sample first half.
3515000: [INFO|LAS |LAS_CTRL] Beginning Manchester reception (m_bit_counter=40, manch_bit_phase=0)
3545000: [LAS EMUL RESP] Data half-bit 1 (overall 9) -> 0 (on  rising edge)
3645000: [LAS EMUL RESP] Data half-bit 2 (overall 10) -> 1 (on falling edge)
3745000: [LAS EMUL RESP] Data half-bit 3 (overall 11) -> 1 (on  rising edge)
3845000: [LAS EMUL RESP] Data half-bit 4 (overall 12) -> 0 (on falling edge)
3945000: [LAS EMUL RESP] Data half-bit 5 (overall 13) -> 0 (on  rising edge)
4545000: [LAS EMUL RESP] Data half-bit 11 (overall 19) -> 1 (on  rising edge)
5545000: [LAS EMUL RESP] Data half-bit 21 (overall 29) -> 1 (on  rising edge)
6545000: [LAS EMUL RESP] Data half-bit 31 (overall 39) -> 1 (on  rising edge)
7545000: [LAS EMUL RESP] Data half-bit 41 (overall 49) -> 1 (on  rising edge)
8545000: [LAS EMUL RESP] Data half-bit 51 (overall 59) -> 1 (on  rising edge)
9545000: [LAS EMUL RESP] Data half-bit 61 (overall 69) -> 1 (on  rising edge)
10545000: [LAS EMUL RESP] Data half-bit 71 (overall 79) -> 1 (on  rising edge)
11045000: [LAS EMUL RESP] Data half-bit 76 (overall 84) -> 1 (on falling edge)
11145000: [LAS EMUL RESP] Data half-bit 77 (overall 85) -> 1 (on  rising edge)
11245000: [LAS EMUL RESP] Data half-bit 78 (overall 86) -> 0 (on falling edge)
11345000: [LAS EMUL RESP] Data half-bit 79 (overall 87) -> 0 (on  rising edge)
11445000: [LAS EMUL RESP] Data half-bit 80 (overall 88) -> 1 (on falling edge)
11495000: [INFO|LAS |LAS_CTRL] Reception of 40 bits complete (m_bit_counter was 1), moving to validation state.
            11505000: [LAS MANCH DEC] Starting to decode 80-bit Manchester data: 0x66aa9a6a59aaaaaaaa99
11515000: [INFO|LAS |LAS_CTRL] Unpacked response frame (current cycle):
11515000: [INFO|LAS |LAS_CTRL]   - Header:    a
11515000: [INFO|LAS |LAS_CTRL]   - RW:        00
11515000: [INFO|LAS |LAS_CTRL]   - EP Addr:   12
11515000: [INFO|LAS |LAS_CTRL]   - Reg Addr:  34
11515000: [INFO|LAS |LAS_CTRL]   - Reg Data:  0001
11515000: [INFO|LAS |LAS_CTRL]   - Parity:    0 (expected 0 in frame)
11515000: [INFO|LAS |LAS_CTRL]   - Stop:      1
11515000: [INFO|LAS |LAS_CTRL] Parity check result (current cycle): 1
11515000: [INFO|LAS |LAS_CTRL] Response validated (decode OK, parity OK). Moving to HOLD_VALID.
11515000: [INFO|LAS |LAS_CTRL] Validating received response data (end of state_changed block for MANCH_VALIDATE)
Time=11515000: [anc_fsm] LAS response received in ST_WAIT_LAS_RESP state, transitioning to ST_PACK_LAS_RESP
[TB LAS Monitor] LAS signals: valid_tx=x, valid_rx=1
            11525000: [LAS MANCH DEC] Decoding successful. Decoded data: 0xa048d00005
            11525000: [DUT DEBUG] Latching LAS response data: 0xa048d00005
Time=11525000: [anc_fsm] Packing LAS response, transitioning to ST_SEND_RESPONSE
            11535000: [TB] FSM State change: ST_WAIT_LAS_RESP ->
[TB LAS Monitor] LAS signals: valid_tx=x, valid_rx=1
11535000: [INFO|LAS |LAS_CTRL] Holding valid_rx for 9 cycles
            11535000: [RESP_GEN] ===== 65-BIT RESPONSE GENERATION =====
            11535000: [RESP_GEN] LAS NON-POSTED WRITE response: payload=0xa048d00005
            11535000: [RESP_GEN] Building 65-bit lpGBT response frame:
            11535000: [RESP_GEN]   SOF=0x0
            11535000: [RESP_GEN]   Source Module=0x0
            11535000: [RESP_GEN]   Data Type=0x0 ( LAS_SRV)
            11535000: [RESP_GEN]   Response Type=0x0 (RESP_DATA)
            11535000: [RESP_GEN]   Source Info=0x0
            11535000: [RESP_GEN]   Status Code=0x00 (SUCCESS)
            11535000: [RESP_GEN]   Response Data=0x0000000000
            11535000: [RESP_GEN]   Parity=0
            11535000: [RESP_GEN]   EOF=0x0
            11535000: [RESP_GEN]   response_valid asserted
            11535000: [RESP_GEN] ====================================
            11535000: [DEBUG] FSM State change: ST_WAIT_LAS_RESP -> ST_PACK_LAS_RESP
            11545000: [TB] FSM State change:  -> ST_SEND_RESPONSE
[TB LAS Monitor] LAS signals: valid_tx=x, valid_rx=1
```

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LAS Communication

Communication Bridge

```
[SCOREBOARD] Time=11555000: Received response: payload=0xa048d00005, status=0x00
[SCOREBOARD] Non-internal command, using FIFO
11555000: [INFO|SCOR] ====== 65-BIT lpGBT RESPONSE FRAME VERIFICATION ======
11555000: [INFO|SCOR] Test:   LAS_SRV NON_POSTED_WRITE
11555000: [INFO|SCOR|SCOREBOARD] Frame structure verification: PASS
11555000: [INFO|SCOR] Frame details:
11555000: [INFO|SCOR]   SOF=0x1, Source=0x2, DataType=0x1, RespType=0x1
11555000: [INFO|SCOR]   SourceInfo=0x0, Status=0x00, Parity=0, EOF=0x1
11555000: [INFO|SCOR]   ResponseData=0xa048d00005
11555000: [INFO|SCOR] ================================================
[SCOREBOARD] PASS: 65-bit lpGBT frame structure verification successful
[SCOREBOARD] ===== STANDARD PAYLOAD VERIFICATION =====
  Command type: 1
  Expected: payload=0xa048d00005, status=0x00
  Actual  : payload=0xa048d00005, status=0x00
[SCOREBOARD] 65-bit Frame Comparison:
  Expected Frame:
    SOF=1, Source=2, DataType=1, RespType=1
    SourceInfo=0, Status=00, Data=a048d00005, Parity=0, EOF=1
  Actual Frame:
    SOF=1, Source=2, DataType=1, RespType=1
    SourceInfo=0, Status=00, Data=a048d00005, Parity=0, EOF=1
11555000: [INFO|SCOR|SCOREBOARD] PASS: Response payload matches expected value
11555000: [INFO|SCOR|SCOREBOARD] RESPONSE DETECTED: valid_out=1, resp_type=1, status_code=0x00, source=0x0
[MONITOR] Time=11555000: Response response_data=a048d00005, status_code=00
11555000: [SUMM|RESP] Response [LAS_RESPONSE]: Payload=0xa048d00005 Status=0x00 PASS (0 cycles)
          11555000: [DUT DEBUG] Clearing LAS response latch
          11555000: [DUT] lpGBT.valid_out ASSERTED (rising edge)
          11555000: [DEBUG] FSM State change: ST_SEND_RESPONSE -> ST_IDLE_AncBrain
11555000: [INFO|RESP|DRIVER] *** RESPONSE DETECTED *** at cycle 1067
11555000: [SUMM|RESP] Response [LAS_WRITE]: Payload=0xa048d00005 Status=0x00 PASS (1067 cycles)
11555000: [INFO|RESP|DRIVER] Full response details:
11555000: [INFO|RESP|DRIVER]   SOF=0x1, Source=0x2, DataType=0x1, RespType=0x1
11555000: [INFO|RESP|DRIVER]   SourceInfo=0x0, Status=0x00, Data=0xa048d00005, Parity=0, EOF=0x1
11555000: [INFO|LAS |DRIVER] Extracted response fields: rw=00, ep_addr=0x12, reg_addr=0x34, data=0x0001
11555000: [INFO|TEST|DRIVER] PASS: Non-posted WRITE response verification successful
[DRIVER] SUCCESS: Non-posted WRITE response received and verified at time 11555000
[DRIVER] ========= LAS Service Non-Posted WRITE Test Complete =========
```

```
**** SCOREBOARD RESULTS ****
Pass count    : 4
Fail count    : 0
Unexpected    : 0
Total checked : 4
Pass rate     : 100.00%

--- LAS Operation Type Breakdown ---
LAS SERVICE Operations:
  Read operations      : 1
  Write operations     : 2
LAS CORE Operations:
  Read operations      : 1
  Write operations     : 2

Operation Category Totals:
  Total READ operations    : 2 (SRV: 1, CORE: 1)
  Total WRITE operations   : 4 (SRV: 2, CORE: 2)
  Posted writes (total)    : 2 (auto-passed)
  Non-posted operations    : 4 (response verified)

Verification Summary:
  Total LAS operations     : 6
  Operations with responses: 4
  Operations without resp. : 2
```

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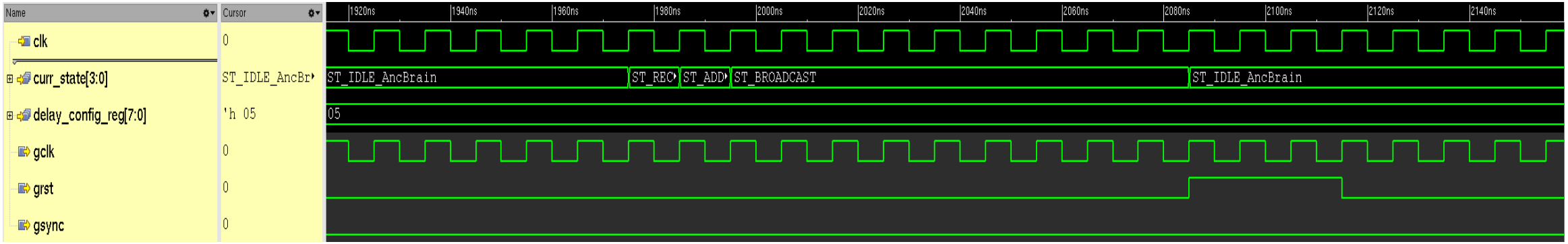
Broadcast Signal Generation

Broadcast Signal Generation




```
[BROADCAST_TEST] Configuring delay register to 5
Time=1745000: [FSM_DEBUG] ST_IDLE -> ST_RECEIVE_HEADER (new command, will be buffered)
1755000: [INFO|SCOR|SCOREBOARD] INTERNAL WRITE COMMAND DETECTED. DELAY[0x00] <= 0x05 (will verify when DUT executes)
Time=1755000: [FSM_DEBUG] Command buffered: data_type=0x0, is_broadcast=0
              1765000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
              1765000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
Time=1765000: [FSM_DEBUG] ST_ADDRESS_CHECK -> ST_DECODE_DATA (buffer_valid=1, data_type=0x0)
              1775000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
              1775000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
Time=1775000: [FSM_DEBUG] ST_DECODE_DATA -> ST_PROCESS_INT (data_type=INTERNAL)
              1785000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
              1785000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
              1795000: [TB] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
              1795000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
              1795000: [DEBUG] FSM State change: ST_DECODE_DATA -> ST_PROCESS_INT
              1795000: Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
              1805000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
              1815000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
              1825000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
              1835000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
Time=1835000: [FSM_DEBUG] Skipping ST_SEND_RESPONSE for internal write operation
              1845000: [TB] Register Write: submodule=SUBID_DELAY, addr=0x00, data=0x05
Time=1845000: [FSM_DEBUG] Buffer cleared after processing in state ST_PROCESS_INT
              1855000: [TB] FSM State change: ST_PROCESS_INT -> ST_IDLE_AncBrain
              1855000: [DEBUG] FSM State change: ST_PROCESS_INT -> ST_IDLE_AncBrain

[BROADCAST_TEST] Test 2: Broadcast Reset Signal Generation
Time=1965000: [FSM_DEBUG] ST_IDLE -> ST_RECEIVE_HEADER (new command, will be buffered)
[BROADCAST_GEN] Time=1975000: Latched reset request
Time=1975000: [FSM_DEBUG] Command buffered: data_type=0x3, is_broadcast=1
[BROADCAST_TEST] Verifying FSM transitions to broadcast state
              1985000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
              1985000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
Time=1985000: [FSM_DEBUG] ST_ADDRESS_CHECK -> ST_BROADCAST (buffer_valid=1, is_broadcast=1)
              1995000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
              1995000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
Time=1995000: [FSM_DEBUG] Waiting for broadcast generator to start (cycle 0)
[BROADCAST_GEN] Time=1995000: Starting broadcast sequence (reset=1, sync=0)
              2005000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_BROADCAST
Time=2005000: [FSM_DEBUG] Buffer cleared after processing in state ST_BROADCAST
              2005000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_BROADCAST
[BROADCAST_TEST] Verifying reset pulse generation with delay=5
Time=2005000: [FSM_DEBUG] Waiting for broadcast generator to start (cycle 1)
Time=2015000: [FSM_DEBUG] Broadcast complete, returning to IDLE (no response needed)
[BROADCAST_GEN] Time=2065000: State transition BCAST_DELAY -> BCAST_PULSE
Time=2075000: [FSM_DEBUG] Broadcast complete, returning to IDLE (no response needed)
[BROADCAST_GEN] Time=2085000: Generating RESET pulse (grst=1)
              2095000: [TB] FSM State change: ST_BROADCAST -> ST_IDLE_AncBrain
              2095000: [DEBUG] FSM State change: ST_BROADCAST -> ST_IDLE_AncBrain
[BROADCAST_GEN] Time=2095000: Generating RESET pulse (grst=1)
[BROADCAST_GEN] Time=2105000: State transition BCAST_PULSE -> BCAST_HOLD
[BROADCAST_GEN] Time=2105000: Generating RESET pulse (grst=1)
[BROADCAST_GEN] Time=2115000: State transition BCAST_HOLD -> BCAST_CLEANUP
[BROADCAST_GEN] Time=2115000: Generating RESET pulse (grst=1)
[BROADCAST_GEN] Time=2125000: State transition BCAST_CLEANUP -> BCAST_IDLE
[BROADCAST_TEST] PASS: GRST pulse width = 4 cycles
```

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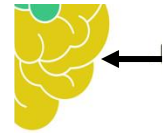
Error Response Format

```
[READ_ERROR_TEST 6] Read SLD01 Control - Parity Error
  Testing: Read SLD01 Control - Parity Error
  Injecting parity error: correct_parity=0, sent_parity=1
Time=32885000: [FSM_DEBUG] ST_IDLE -> ST_RECEIVE_HEADER (new command, will be buffered)
32895000: [INFO|SCOR|SCOREBOARD] INTERNAL READ: SLD01[0x00] (response expected)
[SCOREBOARD] DEBUG: Final predict_response result: resp_type=2, response_data=0x0000000000
[SCOREBOARD] PARITY ERROR: Expected 0, got 1
32895000: [INFO|SCOR|SCOREBOARD] ERROR DETECTED IN INPUT: Parity Error Detected (code=0x20) - waiting for DUT response
Time=32895000: [FSM_DEBUG] Command buffered: data_type=0x0, is_broadcast=0
  Waiting for error response...
            32905000: [TB] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
            32905000: [DEBUG] FSM State change: ST_IDLE_AncBrain -> ST_RECEIVE_HEADER
Time=32905000: [FSM_DEBUG] ST_ADDRESS_CHECK -> ST_DECODE_DATA (buffer_valid=1, data_type=0x0)
            32915000: [TB] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
            32915000: [DEBUG] FSM State change: ST_RECEIVE_HEADER -> ST_ADDRESS_CHECK
Time=32915000: [FSM_DEBUG] ST_DECODE_DATA -> ST_PROCESS_INT (data_type=INTERNAL)
Time=32915000: [FSM_DEBUG] ST_DECODE_DATA -> ST_ERROR_DETECTED (internal command validation error)
            32925000: [TB] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
            32925000: [ERROR_HANDLER] Latching PARITY_ERROR (0x20)
            32925000: [DEBUG] FSM State change: ST_ADDRESS_CHECK -> ST_DECODE_DATA
            32925000: [INTERNAL_CMD_VALIDATOR] *** VALIDATION ERROR ***
            32925000: [INTERNAL_CMD_VALIDATOR]   Submodule: ID=2 -   VALID
            32925000: [INTERNAL_CMD_VALIDATOR]   Address: 0x00 -   VALID
            32925000: [INTERNAL_CMD_VALIDATOR]   R/W: 0x2 -   VALID
            32925000: [INTERNAL_CMD_VALIDATOR]   Parity: 1 (expected 0) - INVALID
            32925000: [INTERNAL_CMD_VALIDATOR]   Error Type: 0x20
            32935000: [TB] FSM State change: ST_DECODE_DATA ->
            32935000: [DEBUG] FSM State change: ST_DECODE_DATA -> ST_ERROR_DETECTED
            32935000: [ERROR_HANDLER] *** PARITY ERROR STABLE ***
            32945000: [ERROR_HANDLER] State transition: ERR_IDLE -> ERR_DETECT
            32945000: [ERROR_HANDLER] Error detected! Type: ERR_PARITY_ERROR (0x20)
            32945000: [ERROR_HANDLER] Error will be stable in 4 cycles
            32975000: [TB] FSM State change:  ->
            32975000: [DEBUG] FSM State change: ST_ERROR_DETECTED -> ST_ERROR_RESPONSE
            32985000: [ERROR_HANDLER] State transition: ERR_DETECT -> ERR_PROCESS
            32995000: [DEBUG] Error detected! Type: 32
            32995000: [ERROR_HANDLER] State transition: ERR_PROCESS -> ERR_RESPONSE_GEN
            32995000: [ERROR_HANDLER] Generating error response for: ERR_PARITY_ERROR (0x20)
            32995000: [ERROR_HANDLER] *** ERROR_VALID ASSERTED for type: ERR_PARITY_ERROR (0x20) ***
Time=32995000: [FSM_DEBUG] Error response ready - acknowledged and proceeding to cleanup
            33005000: [RESP_GEN] TASK: Building error response with err_code=0x20
            33005000: [RESP_GEN] TASK: resp_type=RESP_ERROR(2), source_info=ERR_HANDLER(0xa), status_code=0x20
            33005000: [RESP_GEN] ===== ENHANCED ERROR RESPONSE GENERATION =====
            33005000: [RESP_GEN] Enhanced error response: ERR_PARITY_ERROR (code=0x20)
            33005000: [RESP_GEN] Building 65-bit error response frame:
            33005000: [RESP_GEN]   SOF=0x1
            33005000: [RESP_GEN]   Source Module=0x2
            33005000: [RESP_GEN]   Data Type=0x0
            33005000: [RESP_GEN]   Response Type=0x2 (RESP_ERROR)
            33005000: [RESP_GEN]   Source Info=0xa (ERR_HANDLER)
            33005000: [RESP_GEN]   Status Code=0x20
            33005000: [RESP_GEN]   Response Data=0x0000000000
            33005000: [RESP_GEN]   Parity=1
            33005000: [RESP_GEN]   EOF=0x1
            33005000: [RESP_GEN]   response_valid asserted
            33005000: [RESP_GEN] ================================================
            33005000: [ERROR_HANDLER] State transition: ERR_RESPONSE_GEN -> ERR_WAIT_ACK
            33005000: [ERROR_HANDLER] *** ERROR_RESPONSE_READY ASSERTED for type: ERR_PARITY_ERROR (0x20) ***
[TB] Time=33005000: Response received from DUT: response_data=0x0000000000
            33015000: [TB] FSM State change:  ->
Time=33015000: [FSM_DEBUG] Buffer cleared after processing in state ST_ERROR_CLEANUP
            33015000: [ERROR_HANDLER] Clearing all enhanced error signals (state=ST_ERROR_CLEANUP)
            33015000: [DEBUG] FSM State change: ST_ERROR_RESPONSE -> ST_ERROR_CLEANUP
            33015000: [ERROR_HANDLER] State transition: ERR_WAIT_ACK -> ERR_COMPLETE
            33015000: [ERROR_HANDLER] Error handling complete
            33015000: [ERROR_HANDLER] *** ERROR_RESPONSE_READY DEASSERTED ***
            33025000: [TB] FSM State change:  -> ST_IDLE_AncBrain
            33025000: [DEBUG] FSM State change: ST_ERROR_CLEANUP -> ST_IDLE_AncBrain
            33025000: [ERROR_HANDLER] State transition: ERR_COMPLETE -> ERR_IDLE
            33025000: [ERROR_HANDLER] *** ERROR_VALID DEASSERTED ***
  ! Found error response in resp_out (valid_out may have been missed)
  Response: status_code=0x20, resp_type=2
  SUCCESS: Error correctly detected and reported
    Expected error type: ERR_PARITY_ERROR (0x20)
    Actual error code: 0x20
    Response type: RESP_ERROR (2)
[READ_ERROR_TEST 6] PASSED: Read SLD01 Control - Parity Error

[TEST] ==== PERFORMING COMPLETE SYSTEM RESET BETWEEN TESTS ====
```



System Stability & Error Handling

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ePIC

What's next?

Transitioning to Synthesizable RTL: From Functional Mock-up to Hardware Implementation with Triplication

Thank You

EIC-AncBrain Block Diagram