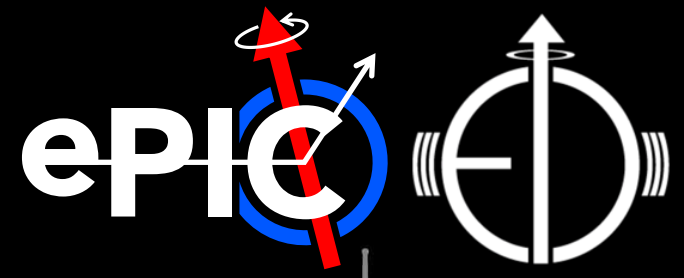




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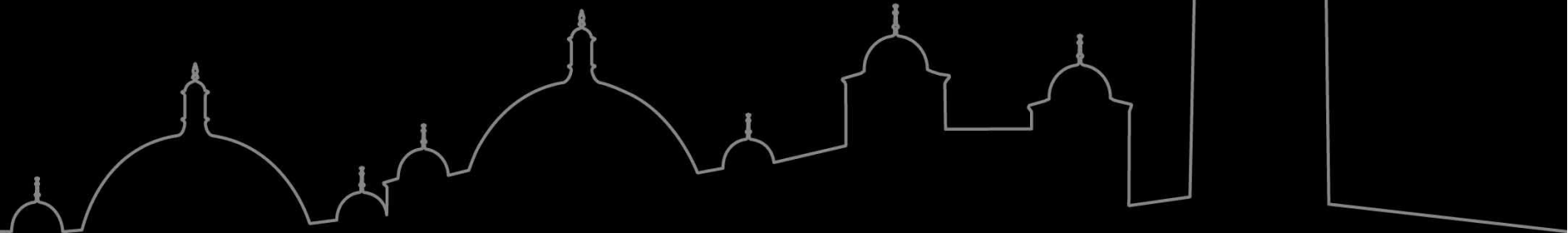


# ePIC SVT RDO boards Locations and power

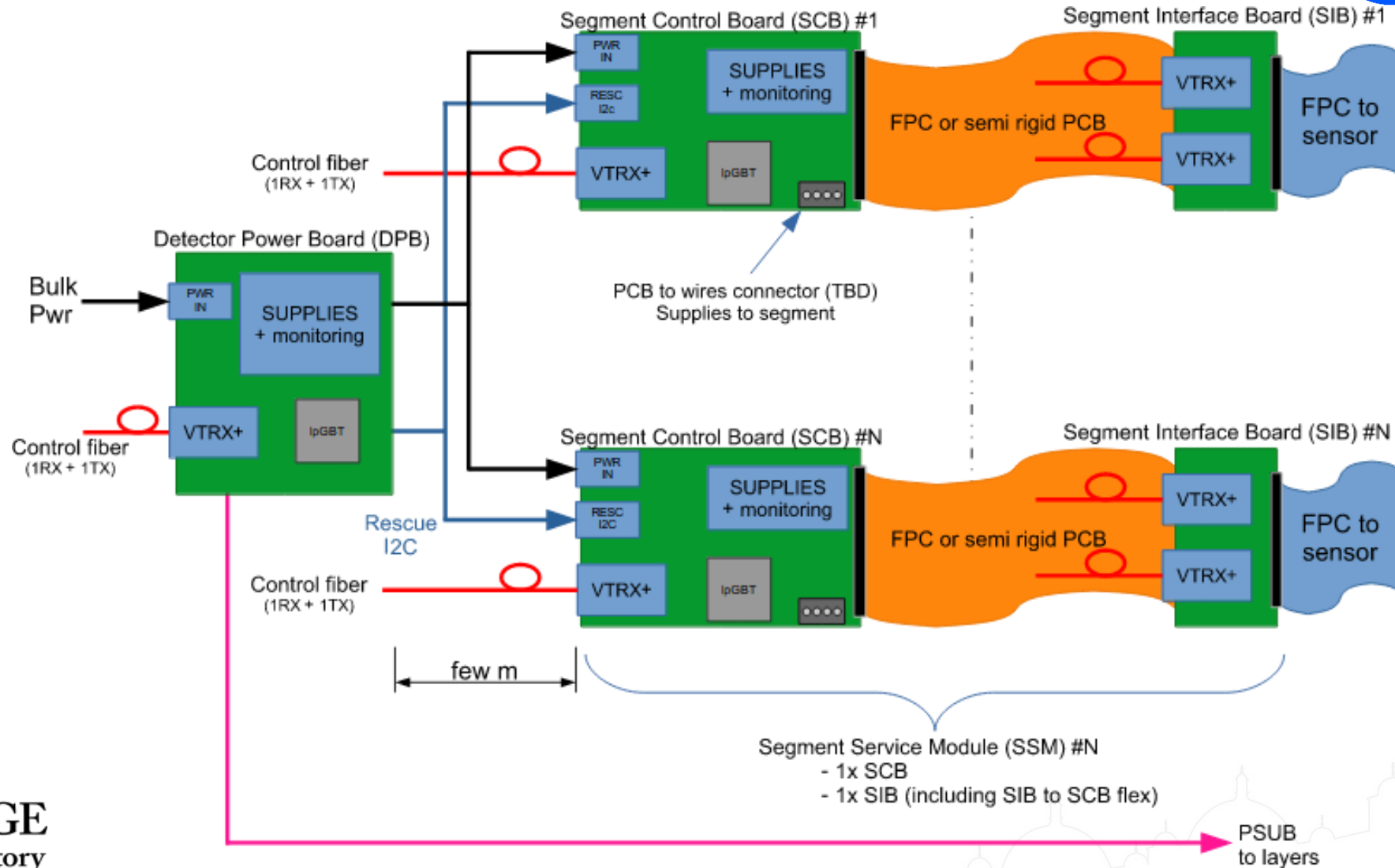
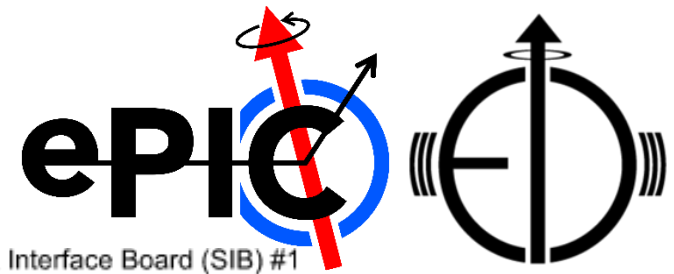
James Glover

ePIC SVT working meeting  
Stony Brook University

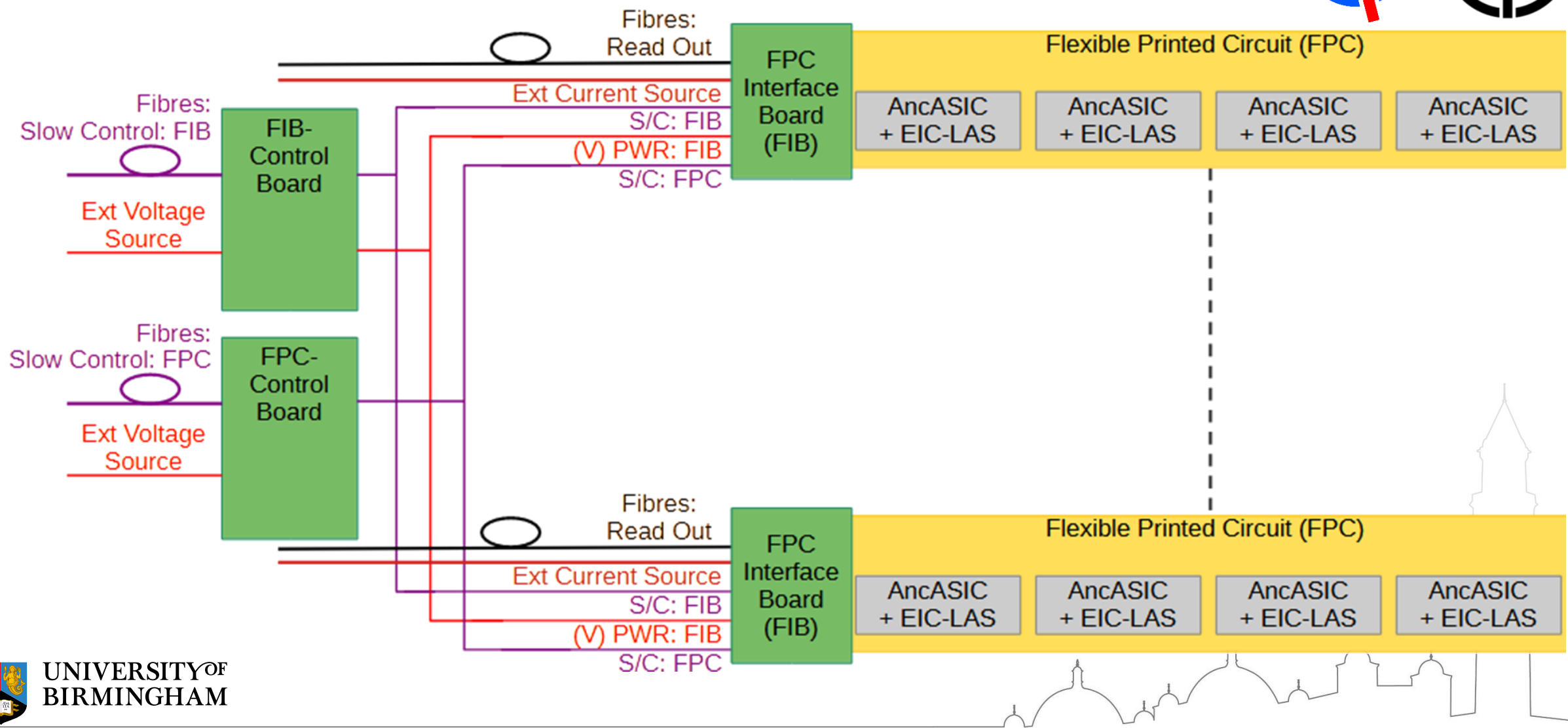
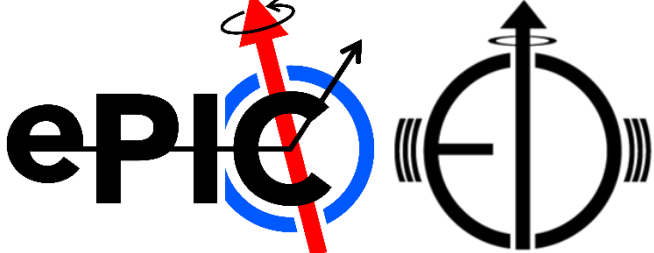
Wed, 9<sup>th</sup> July 2025



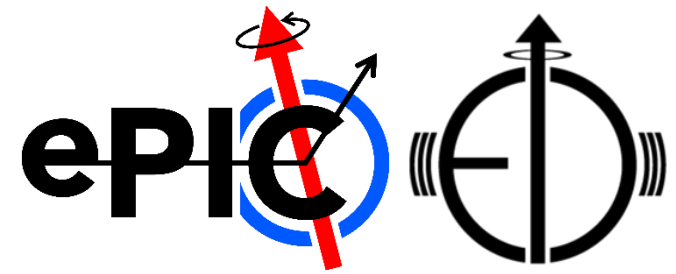
# Reminder: IB Readout Architecture



# OB/Disk: What we had



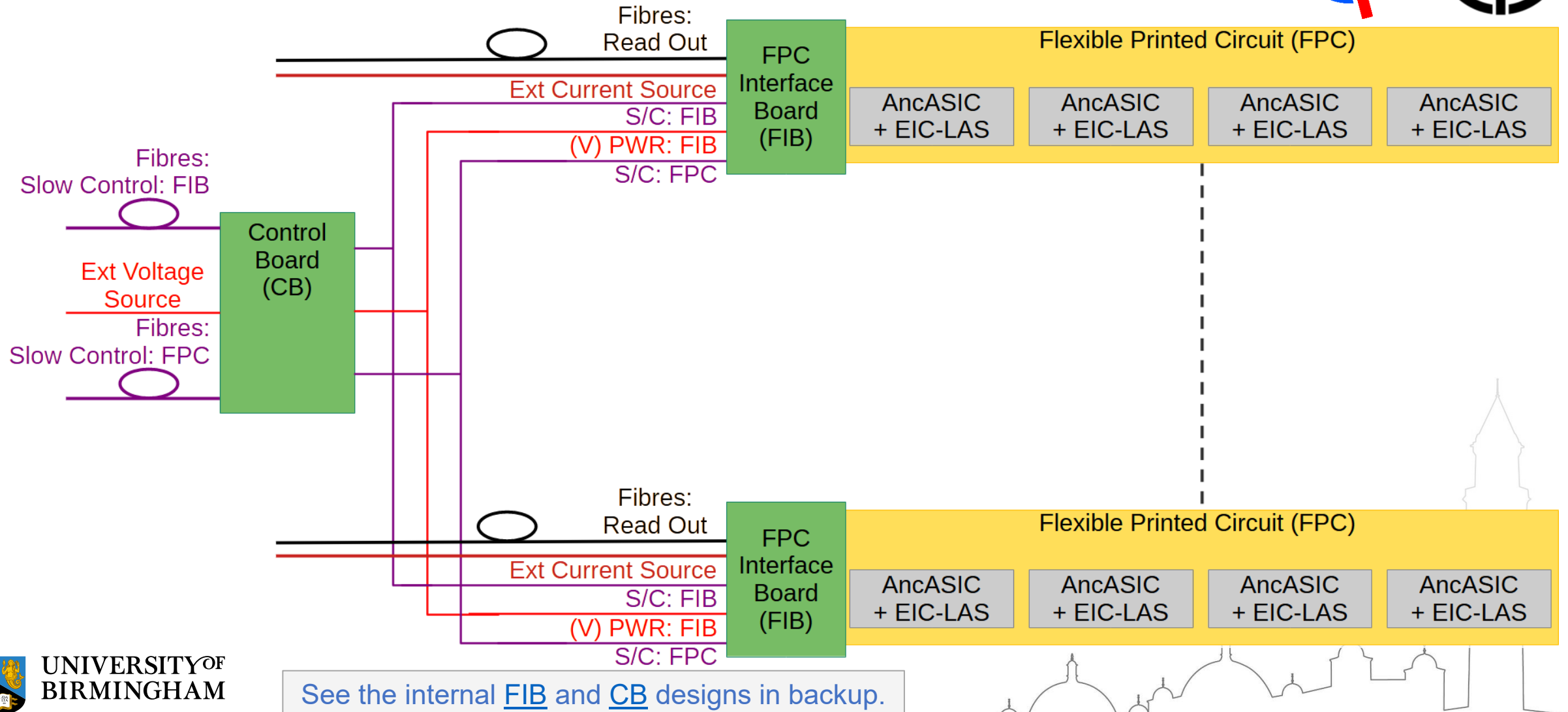
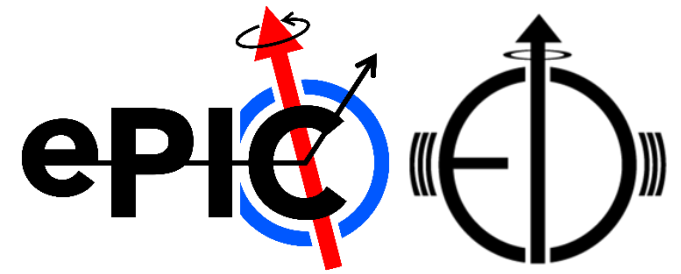
# What has changed?



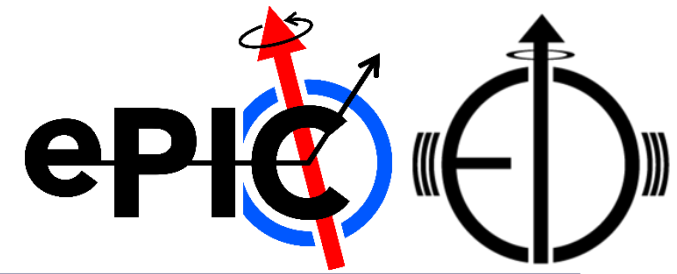
- Previously planning (hoping) to send S/Cs for as many VTRx+ (FIBs) as possible – utilise most of the **16 e-links** of a IpGBT.
- Has become clear that VTRx+ I<sup>2</sup>C is very specific, and **communication will only work** via the (**3**) I<sup>2</sup>C master ports of a IpGBT.
- This greatly reduces the number of VTRx+ (FIBs) controllable by 1 IpGBT – if a 1:4 serial multiplexer is used:
  - Reduces from 1(IpGBT) : 48(VTRx+) (assuming 4 e-links reserved for onboard use).
  - To 1(IpGBT) : 12(VTRx+).
- Now, both FPC-CB and FIB-CB would be 1(parent) : 12(children) boards.



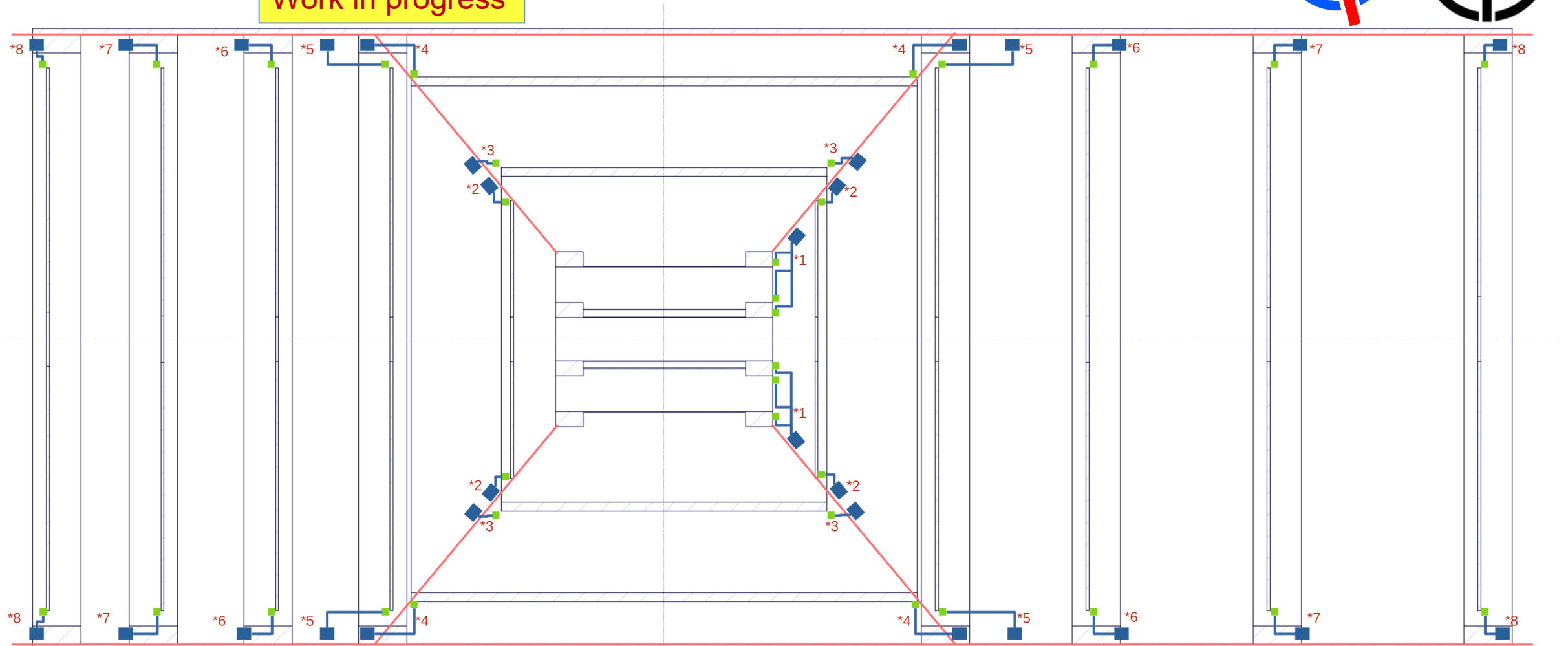
# New OB/Disk Readout Architecture



# Approx SVT RDO board locations



Work in progress



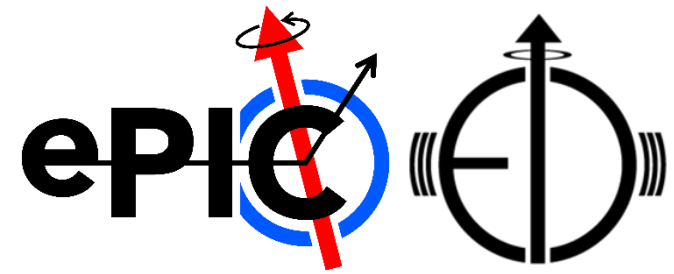
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- Carbon fibre support structure (tube and cone)
- Electronics boards (Interface Boards)
- Electronics boards (Control Boards/Power Boards)

# IB: Segment Interface Board

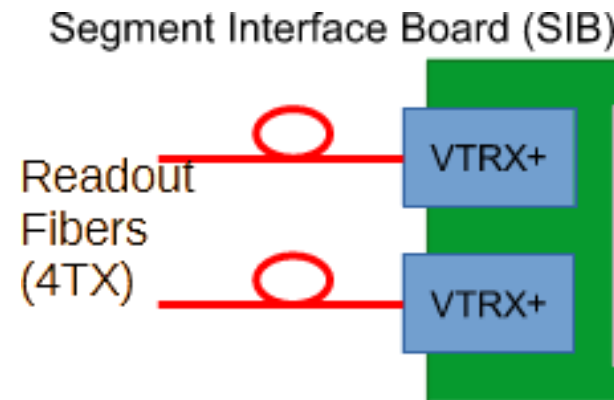


Work in progress

- Contains 2 VTRx+ only.
- No downstream power to be supplied.
- About **0.4 W supplied to and burnt off on the board.**
- 1 SIB for each MOSAIX segment.
- 68 SIB needed for the whole IB.
- Connected to SCB by printed circuit.
  - Rigid/flexible yet to be determined.

## Assumptions

- Based on old ITS3 DPB plan (new plan would need 16 DPBs).
- Assumed regulator losses based on the BPOL family of DC/DCs (as in ITS3).

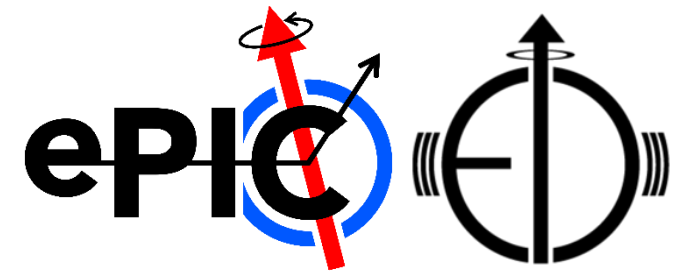


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# IB: Segment Control Board

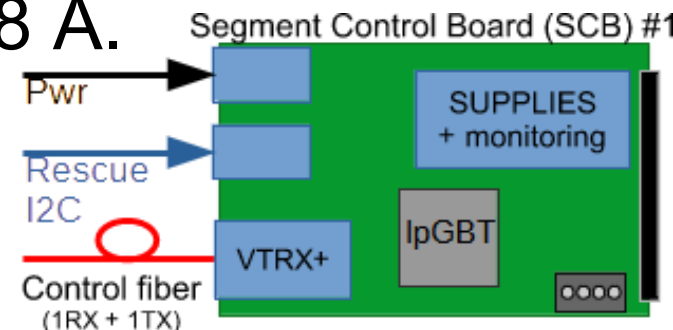


Work in progress

- Contains VTRx+, IpGBT, voltage regulators (10V to 2V5 and 1V2) and monitoring.
- Up to 8 W needing to be supplied to SCB.
- About 4.25 W burnt off on the board (rest for SIB).
- 1 SCB for each SIB.
- Provides 2V5 and 1V2 supply to SIBs.
- 68 SCB needed for the whole IB.
- Could be supplied by 10 V @ 0.8 A.
- 1.42 mm wire diameter needed.

- Assumptions**
- Based on old ITS3 DPB plan (new plan would need 16 DPBs).
  - Assumed regulator losses based on the BPOL family of DC/DCs (as in ITS3).

Assuming aluminium wire and a V-drop of 3% over 10 m @ 75 °C.



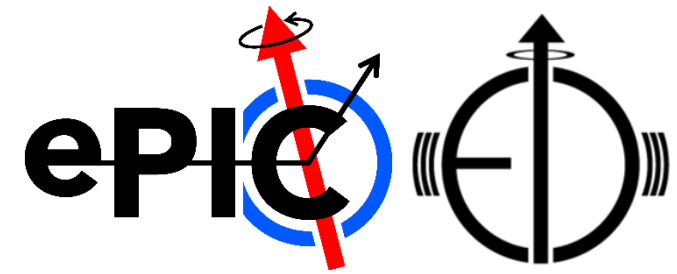
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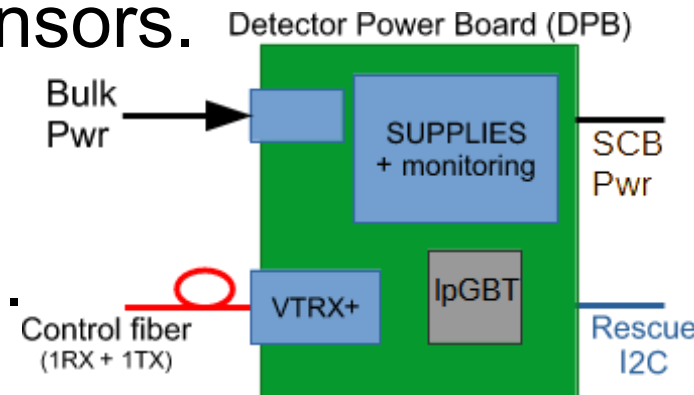
# IB: Detector Power Board



Work in progress

- Contains VTRx+, IpGBT, voltage regulators (50V to 10V, 2V5, 1V2 and -ve PSUB) and monitoring.
- Up to 130 W needing to be supplied to DPB!
- About **14 W burnt off on the board!**
- 1 DPB for up to 14 SSMs (SCB+SIB).
- Provides 10V supply to SCBs.
- Supplies -ve PSUB to ~4 IB sensors.
  - Diced piece of silicon, containing multiple segments.
- 6 DPB needed for the whole IB.

- Assumptions**
- Based on old ITS3 DPB plan (new plan would need 16 DPBs).
  - Assumed regulator losses based on the BPOL family of DC/DCs (as in ITS3).



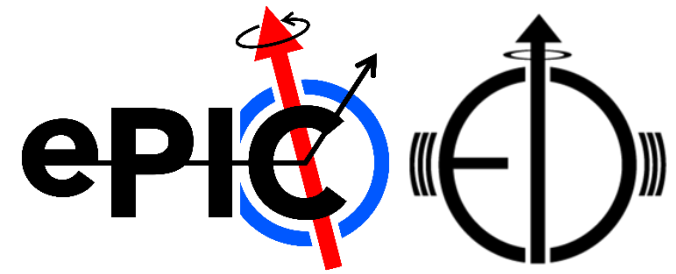
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PSUB to layers

# OB/Disk: FPC Interface Board



- On board powering needs: VTRx+ only.
  - No downstream power to be supplied.
- About 0.2 W supplied to and burnt off on the board.
- Supplied by Control Board with 2V5 and 1V2.
- ~1,112 of these boards needed for whole SVT.
- ~4,448 wires (source and return, 2 voltages) between CBs and FIBs.
  - 0.55 mm wire diameter needed for 2V5\*.
  - 0.80 mm wire diameter needed for 1V2\*.
    - Heavily dependant on temperature and cable length.
    - Worst case assumptions made.

Work in progress

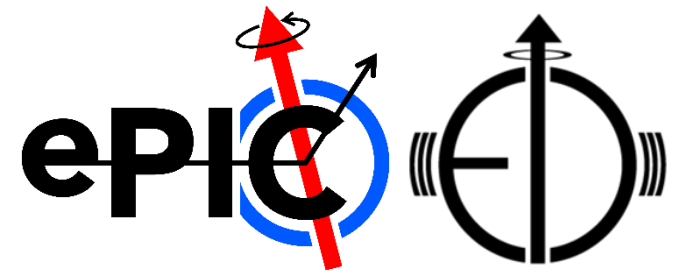
\* Assuming aluminium wire, 60 mA of current, 3% V-drop over 5 m, 60 °C environment.

Compare with [FPC-CB](#) and [FIB-CB](#) powering in backup.



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# OB/Disk: Control Board



- On board powering needs: VTRx+, IpGBT(s) and serial multiplexers
- Downstream powering needs: VTRx+ (on up to 12 FIBs).
- Up to 10 W needing to be supplied!
- About 7 W burnt off on the board.
- ~104 of these control boards needed for whole SVT.
- Could be supplied by 54 V @ 0.21 A.
- 0.57 mm wire diameter needed.
  - Assuming aluminium wire and a V-drop of 10% over 100 m @ 75 °C.
- ~208 wires needed (source and return lines) from PSU to SVT.

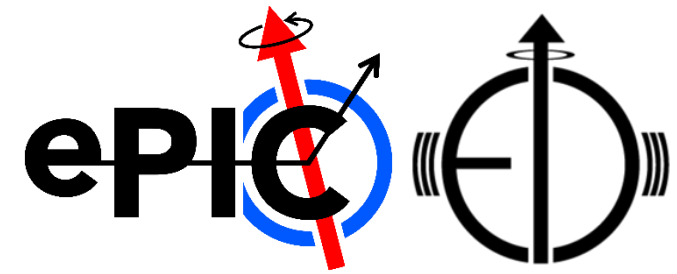
Work in progress



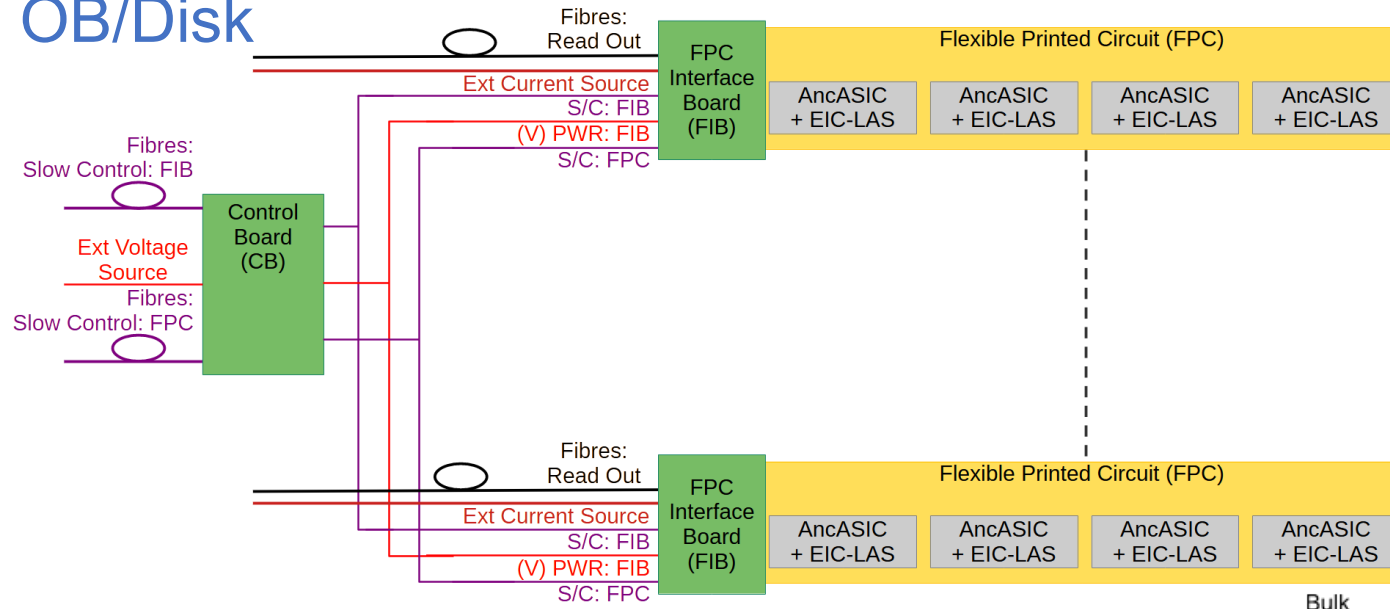
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Compare with [FPC-CB](#) and [FIB-CB](#) powering in backup.

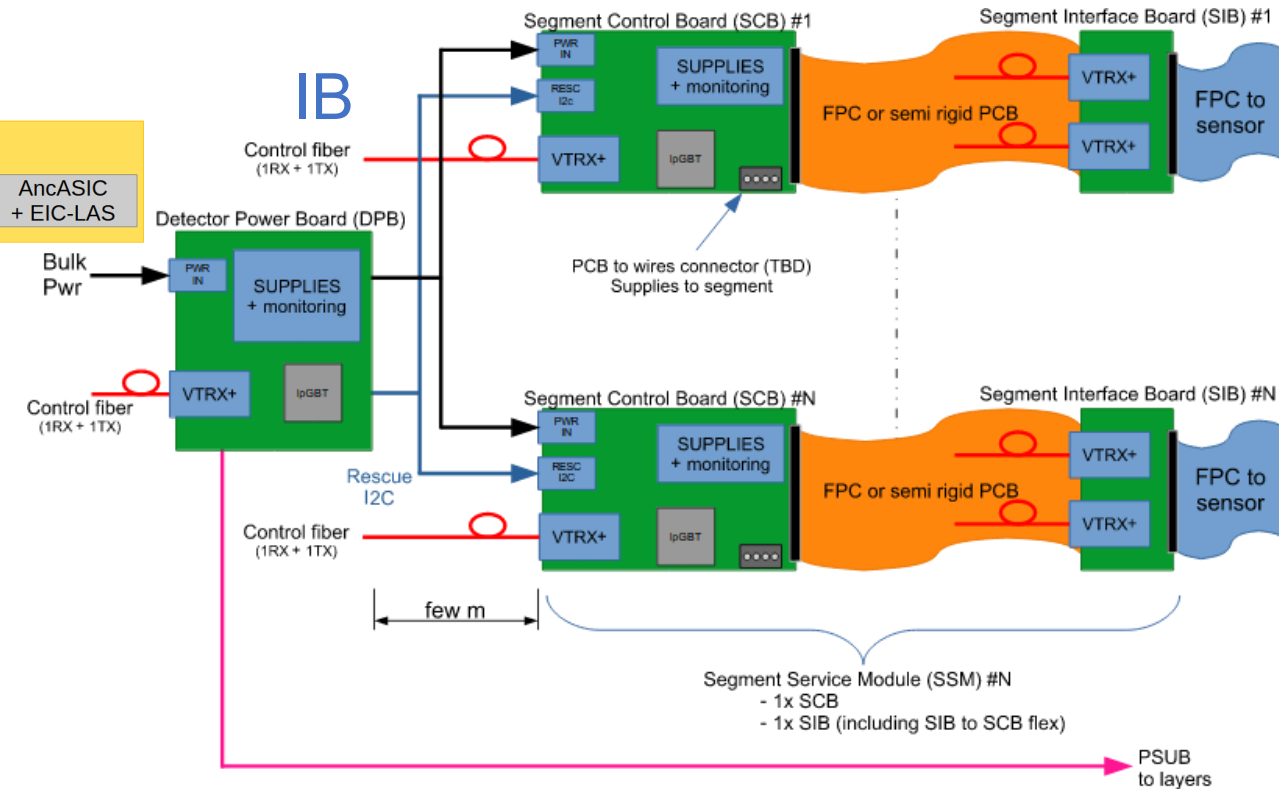
# SVT Readout Architecture



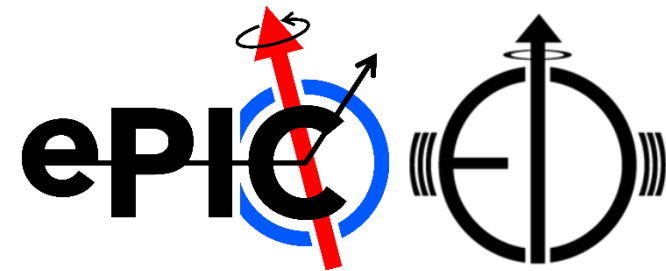
OB/Disk



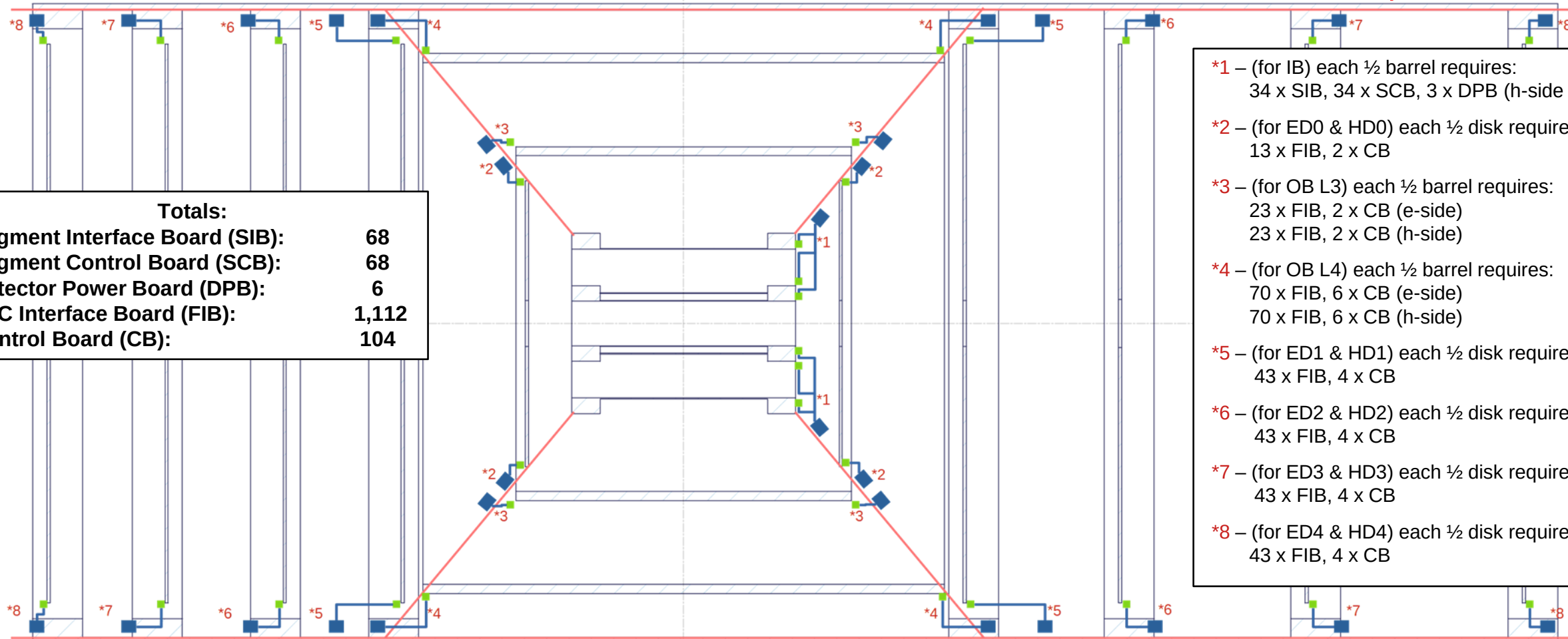
Total power to be **cooled** in the SVT readout boards could be as high as 1.4kW!



# Approx SVT RDO board locations



Work in progress



## Totals:

|                                |       |
|--------------------------------|-------|
| Segment Interface Board (SIB): | 68    |
| Segment Control Board (SCB):   | 68    |
| Detector Power Board (DPB):    | 6     |
| FPC Interface Board (FIB):     | 1,112 |
| Control Board (CB):            | 104   |

- \*1 – (for IB) each ½ barrel requires:  
34 x SIB, 34 x SCB, 3 x DPB (h-side only)
- \*2 – (for ED0 & HD0) each ½ disk requires:  
13 x FIB, 2 x CB
- \*3 – (for OB L3) each ½ barrel requires:  
23 x FIB, 2 x CB (e-side)  
23 x FIB, 2 x CB (h-side)
- \*4 – (for OB L4) each ½ barrel requires:  
70 x FIB, 6 x CB (e-side)  
70 x FIB, 6 x CB (h-side)
- \*5 – (for ED1 & HD1) each ½ disk requires:  
43 x FIB, 4 x CB
- \*6 – (for ED2 & HD2) each ½ disk requires:  
43 x FIB, 4 x CB
- \*7 – (for ED3 & HD3) each ½ disk requires:  
43 x FIB, 4 x CB
- \*8 – (for ED4 & HD4) each ½ disk requires:  
43 x FIB, 4 x CB



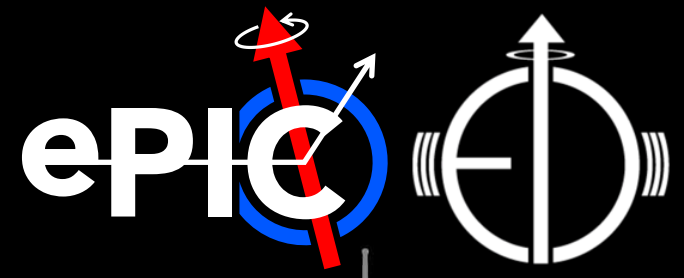
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[Old version in backup.](#)

- Carbon fibre support structure (tube and cone)
- Electronics boards (Interface Boards)
- Electronics boards (Control Boards/Power Boards)

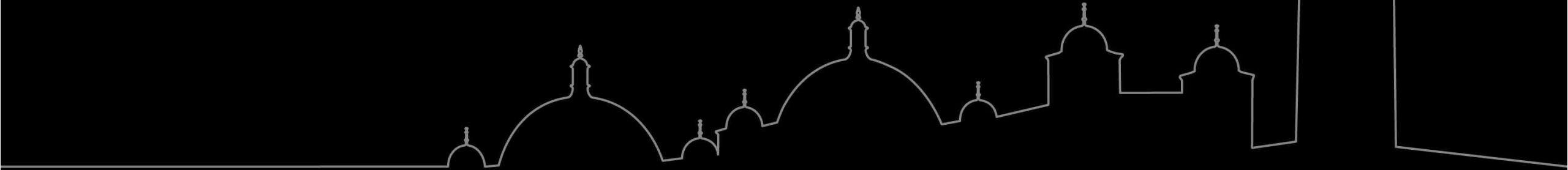


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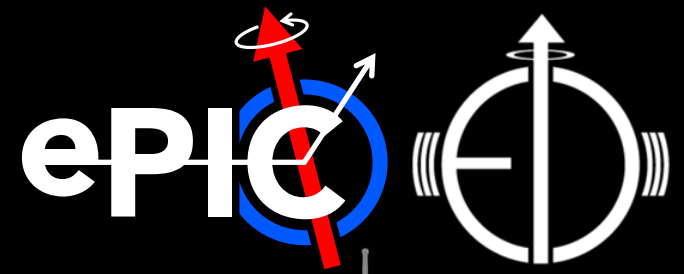
# Thank you very much!

Any questions?

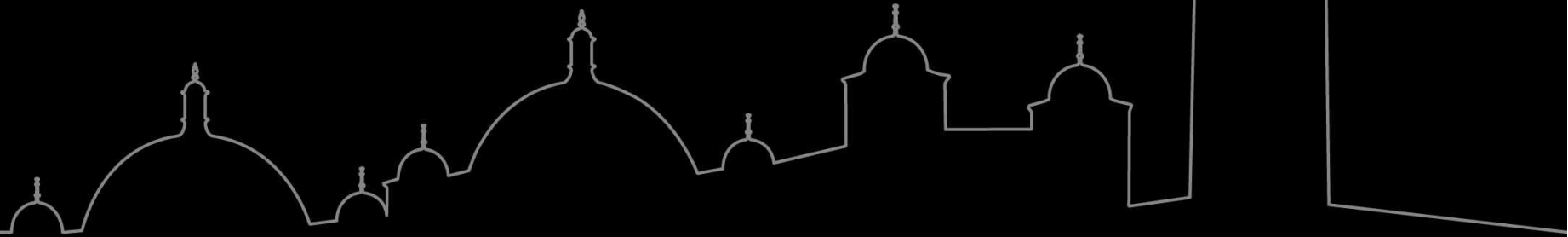




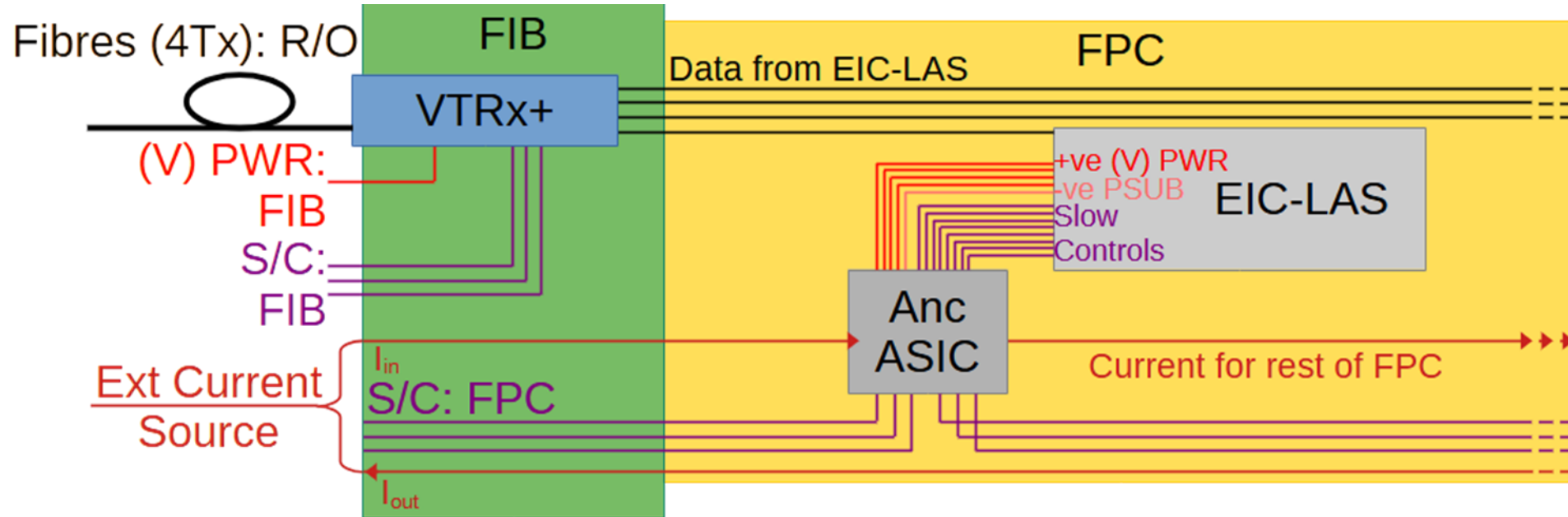
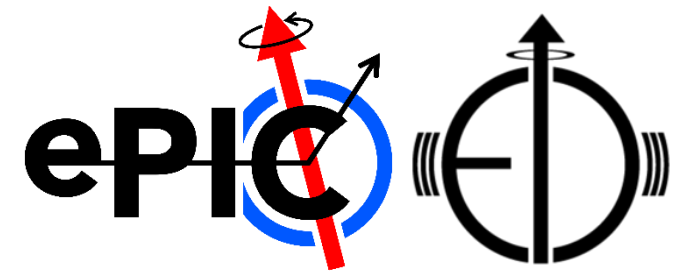
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# Additional (support) slides



# OB/Disc: FPC Interface Board (FIB)



[Back to New OB/Disc Readout Architecture.](#)

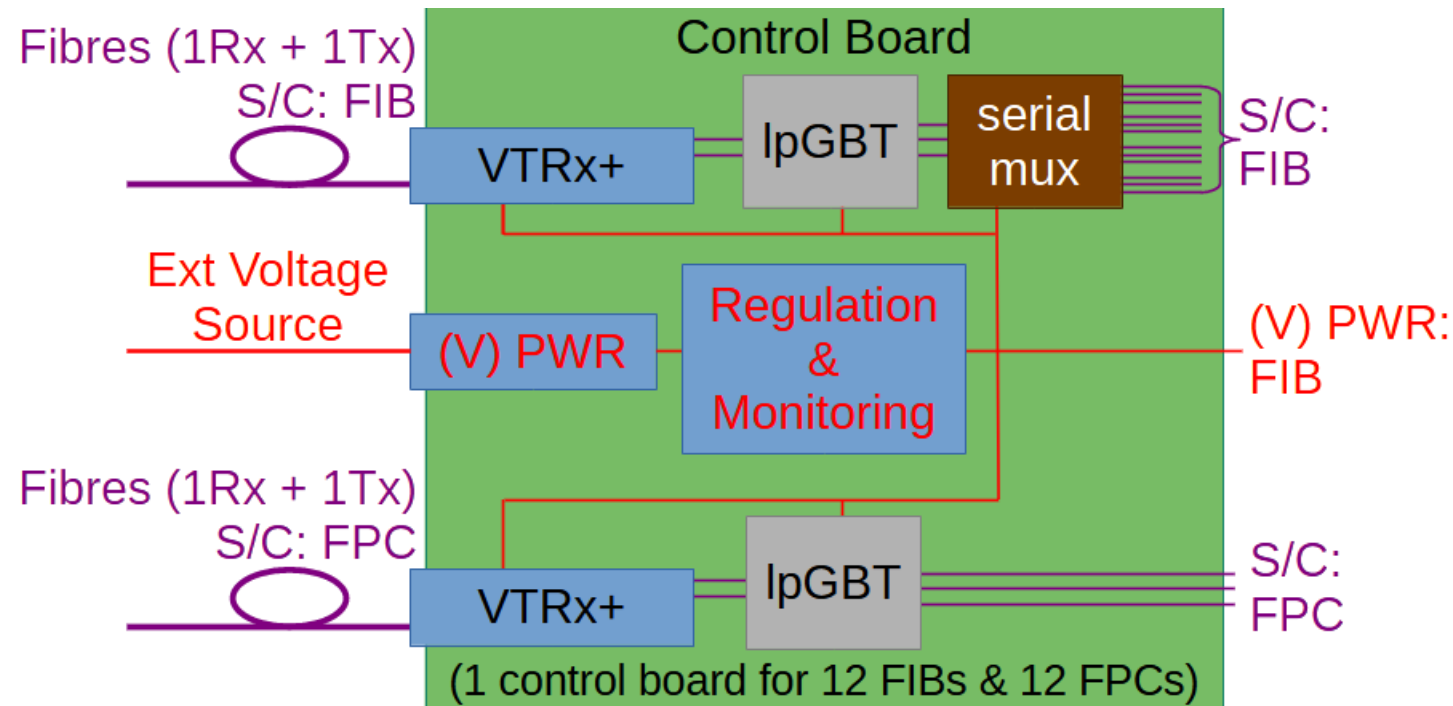
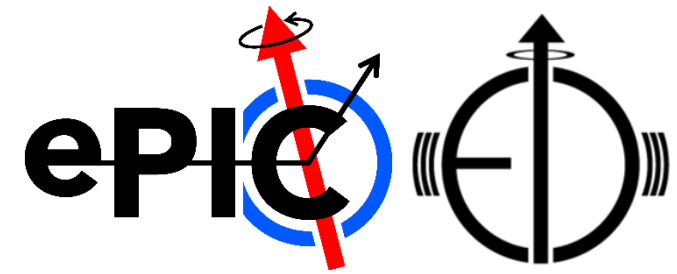
- FIB PWR and S/C for the VTRx+ (EIC-LAS data).
- FPC current supply and S/C for AncASIC to translate to 5 power domains (incl. -ve substrate bias) and slow control protocol for EIC-LAS.



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# OB/Disc: Control Board



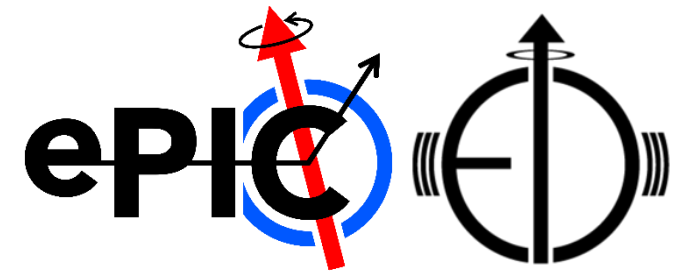
- Use the IpGBT e-links for the FPC S/C commands.
- Use the IpGBT I<sup>2</sup>C master connections for the FIB S/C commands.

[Back to New OB/Disc Readout Architecture.](#)

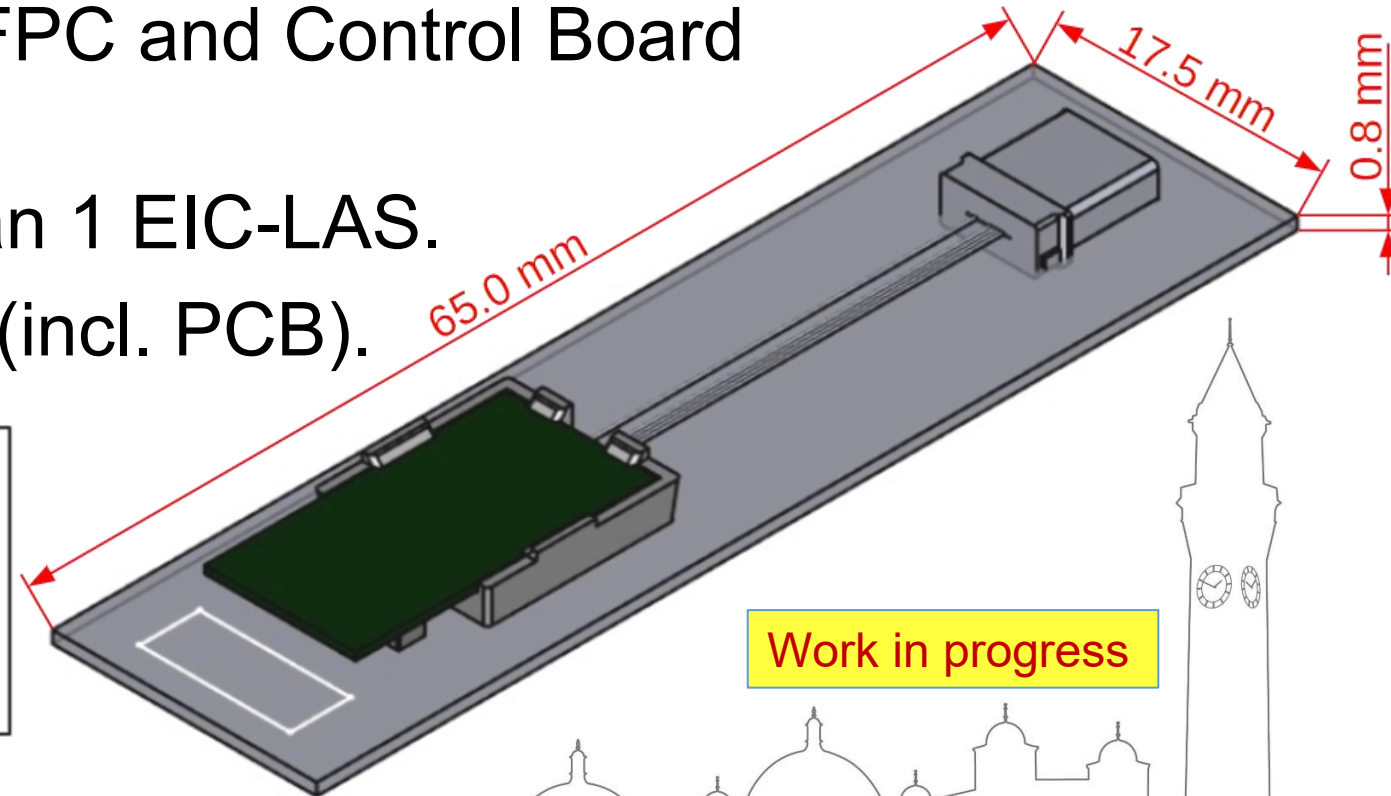
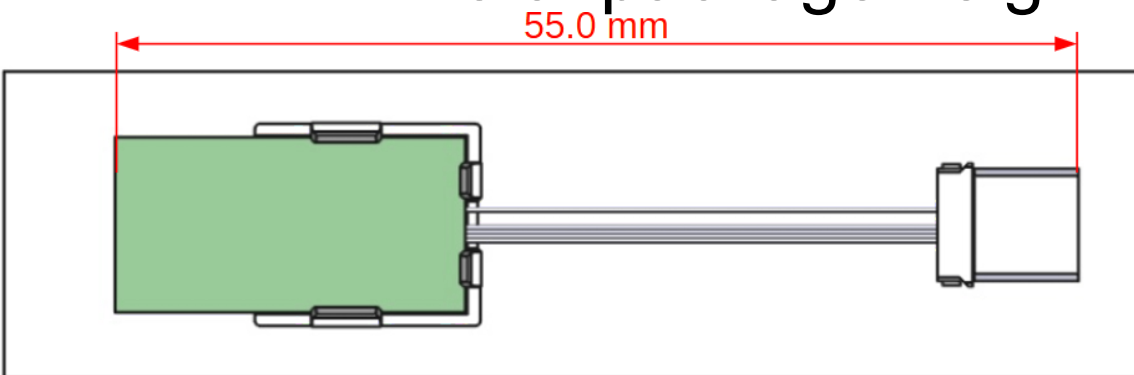


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# OB/Disk: FIB dimensions



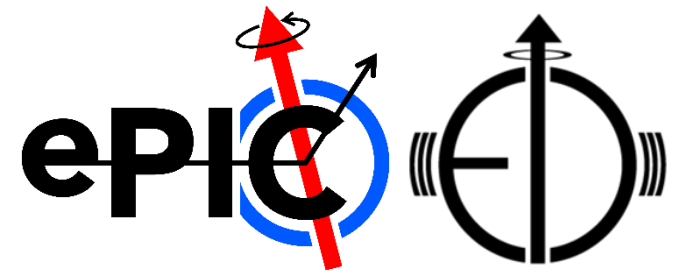
- Shortest possible total length (5.5 cm) that CERN will produce.
- Prevent damage to VTRx+ pigtail, by mounting total length on the FIB.
- Allow space to bond/solder FPC and Control Board connections to FIB.
- Keep the board narrower than 1 EIC-LAS.
- ~4 mm total package height (incl. PCB).



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No change here!

# OB/Disk: Control Board dimensions

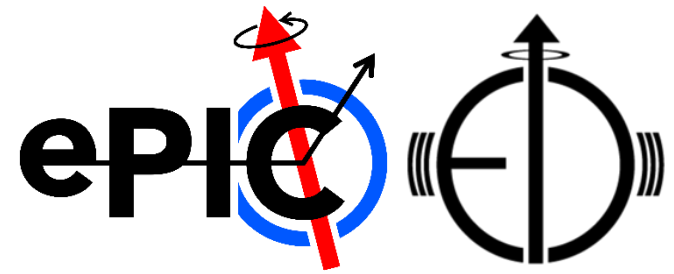


- Less constrained than the FIB.
- Roughly same 65 mm length.
  - Total length of VTRx+ and pigtail still to be mounted on the PCB.
  - Space to bond/solder connections still needed.
- Additional space needed for:
  - Power regulation.
  - Monitoring.
  - IpGBT(s) –  $\sim 1 \text{ cm}^2$ .
  - Serial multiplexers (FIB – Control Board only) – typ.  $< 1 \text{ cm}^2$  per mux.
    - Such as [Texas Instruments TCA9544A](#).
  - (Extra VTRx+ - if 2 IpGBTs are needed).

Work in progress



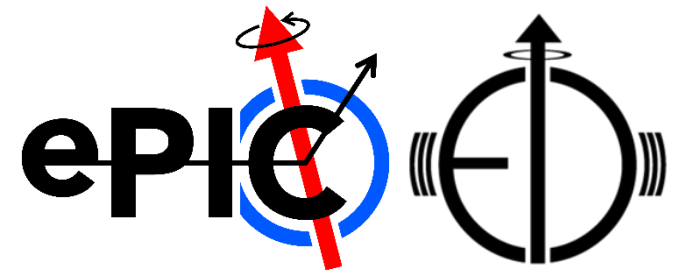
# OB/Disk: Control Board dimensions



- Assumed  $65 \times 17.5$  mm additional area needed for 2<sup>nd</sup> VTRx+.
  - Assumed  $65 \times 35$  mm additional area to enable the addition of 2 IpGBTs, power regulation & monitoring, and 3 serial multiplexers.
  - Total extra area:  $65 \times 52.5$  mm (on top of the FIB dimensions).
  - Board dimensions become  $65 \times 70$  mm (same as old FIB-CB).
  - Package height could be 20 mm (if DC/DCs are used).
- Consider whether everything can work with 1 IpGBT and 1 VTRx+.
  - IpGBT connections will be saturated and limited to 4 e-links for internal use!
- FIB slow controls need to go through the IpGBT's I<sup>2</sup>C master connections (3/IpGBT) and each I<sup>2</sup>C master connects to a 1:4 serial multiplexer.
    - 1 Control Board connects to (up to) 12 FIBs.
  - FPC slow controls planned to be sent via IpGBT e-links (16/IpGBT).
    - 1 Control Board connects to (up to) 12 FPCs (via the FIBs).
      - 4 e-links saved for internal CB use.
      - All e-links from 2<sup>nd</sup> (FIB S/C) IpGBT are also available for internal use.



# OB/Disk: Change summary



Proposed to switch to a single Control Board (CB) from separate FIB-CBs and FPC-CBs.

Switch from:

- 104 FPC-CBs @  $65 \times 47.5$  mm, dissipating  $\sim 1.75$  W per board.
- 32 FIB-CBs @  $65 \times 70$  mm, dissipating  $\sim 16.5$  W per board.

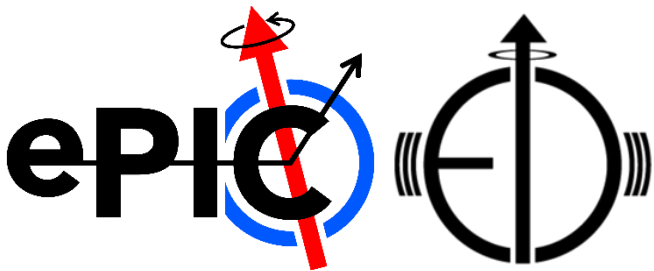
To:

- 104 CBs @  $65 \times 70$  mm, dissipating  $\sim 7.1$  W per board.

**104 CBs @  $65 \times 68.61$  mm, dissipating  $\sim 6.83$  W per board would be a like for like area and power match.**



# OB: FIB quantities

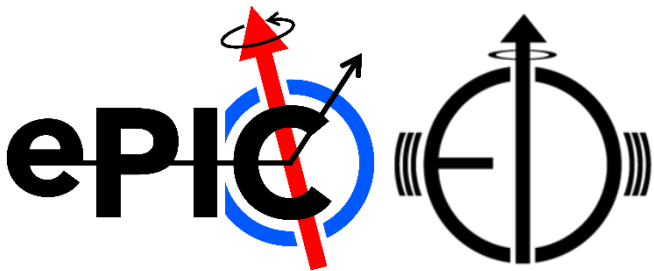


|        | e-side | h-side | Total |
|--------|--------|--------|-------|
| L3     | 46     | 46     | 92    |
| L4     | 140    | 140    | 280   |
| ED/HD0 | 26     | 26     | 52    |
| ED/HD1 | 86     | 86     | 172   |
| ED/HD2 | 86     | 86     | 172   |
| ED/HD3 | 86     | 86     | 172   |
| ED/HD4 | 86     | 86     | 172   |
|        |        |        | 1,112 |

Work in progress



# OB: Control Board quantities

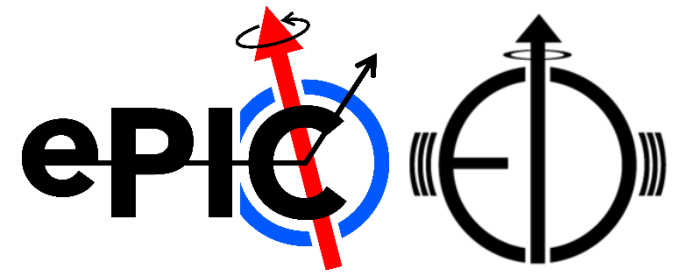


|        | e-side | h-side | Total |
|--------|--------|--------|-------|
| L3     | 4      | 4      | 8     |
| L4     | 12     | 12     | 24    |
| ED/HD0 | 4      | 4      | 8     |
| ED/HD1 | 8      | 8      | 16    |
| ED/HD2 | 8      | 8      | 16    |
| ED/HD3 | 8      | 8      | 16    |
| ED/HD4 | 8      | 8      | 16    |
|        |        |        | 104   |

Work in progress



# Current Source – PSU channels



Current assumptions on the number of SP chain needed in the SVT (OB + Disks) is 1,112 (Same as FIB quantities).

- Each of these need a current of ~2 A.
- If aluminium wire, wire diameter of >5.7 mm needed!
  - 5% power loss over 100m (assuming a 10V supply and temp up to 75 °C).
  - Copper could reduce diameter to 4.6 mm (with 5% power losses).
  - 10% power loss could bring this down to 4.1 mm diameter (for Al).
- >2,000 wires needed (source and return lines) from PSU to SVT.

Work in progress



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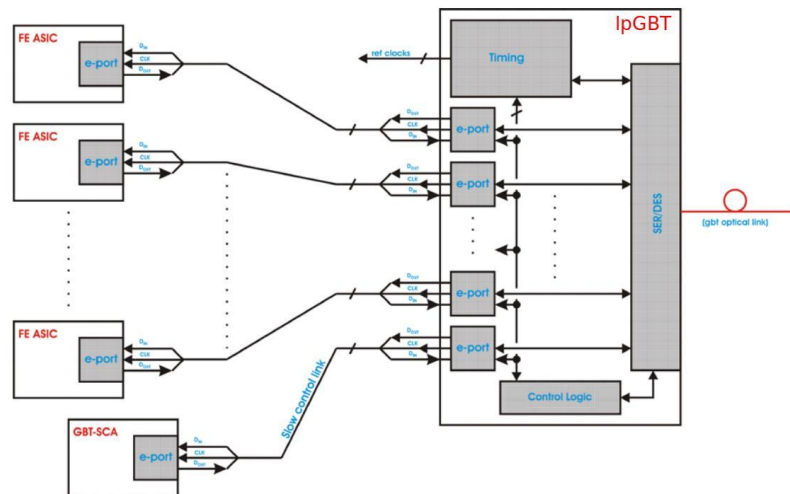
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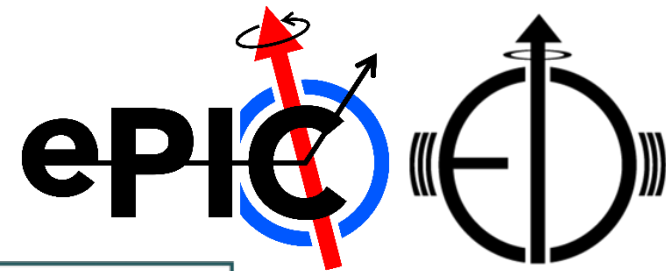
24



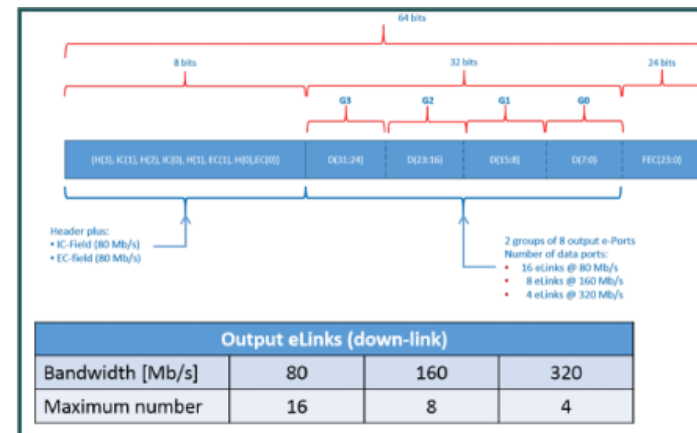
# lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 128bit or 256bit
  - 256bit frame contains 192bits of payload (7.68 Gbps)
  - Up to 24 e-links at either 160 Mbps or 320 Gbps



**Downlink**  
Line Rate: **2.56 Gbps**  
32 out of 64 bits are data:  
Payload = **1.280 Gbps**



**Data Uplink**

192 out of 256 bits are data:  
Payload = **7.680 Gbps**

| Input eLinks (up-link)   |      |     |     |       |     |     |       |     |      |       |     |      |
|--------------------------|------|-----|-----|-------|-----|-----|-------|-----|------|-------|-----|------|
| Up-link bandwidth [Gb/s] | 5.12 |     |     |       |     |     | 10.24 |     |      |       |     |      |
| FEC coding               | FEC5 |     |     | FEC12 |     |     | FEC5  |     |      | FEC12 |     |      |
| Bandwidth [Mb/s]         | 160  | 320 | 640 | 160   | 320 | 640 | 320   | 640 | 1280 | 320   | 640 | 1280 |
| Maximum number           | 28   | 14  | 7   | 24    | 12  | 6   | 28    | 14  | 7    | 24    | 12  | 6    |

| Field             | 5.12 Gbps |       | 10.24 Gbps |       |
|-------------------|-----------|-------|------------|-------|
|                   | FEC5      | FEC12 | FEC5       | FEC12 |
| Frame [bits]      |           | 128   |            | 256   |
| Header [bits]     |           | 2     |            | 2     |
| IC [bits]         |           | 2     |            | 2     |
| EC [bits]         |           | 2     |            | 2     |
| D [bits]          | 112       | 96    | 224        | 192   |
| FEC [bits]        | 10        | 24    | 20         | 48    |
| LM [bits]         | 0         | 2     | 6          | 10    |
| Correction [bits] | 5         | 12    | 10         | 24    |
| # of eLink groups | 7         | 6     | 7          | 6     |

# VTRx+ Front-end Module

- **Versatile**

- Up to 4 Tx + 1 Rx, configurable by masking channels

- **Miniaturised**

- 20 x 10 x 2.5 mm

- **Pluggable**

- Electrical connector

- **Data-rate**

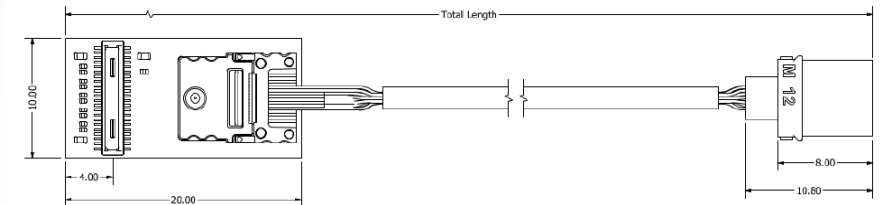
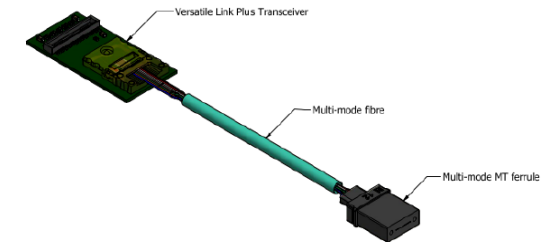
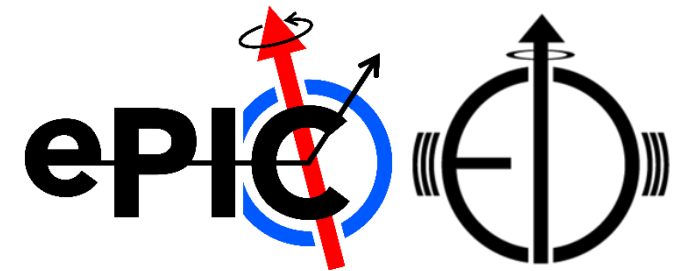
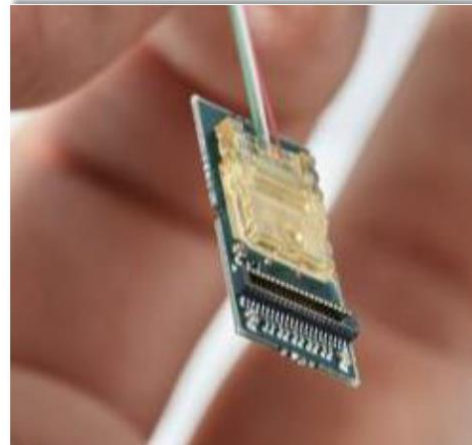
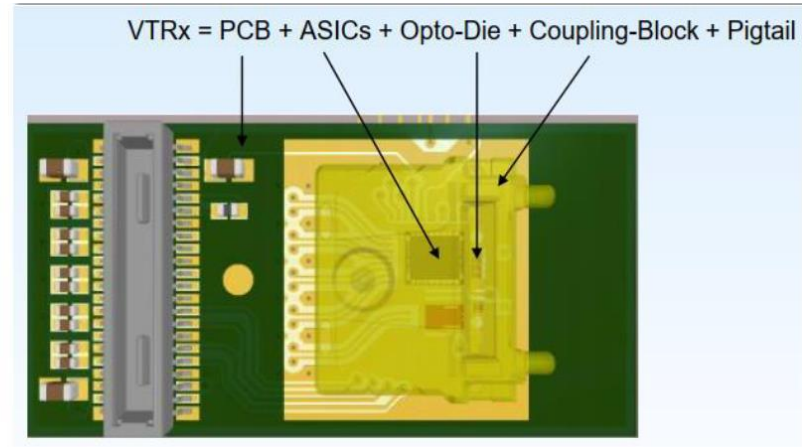
- Tx: up to 4x10 Gb/s, Rx: 2.5 Gb/s

- **Environment**

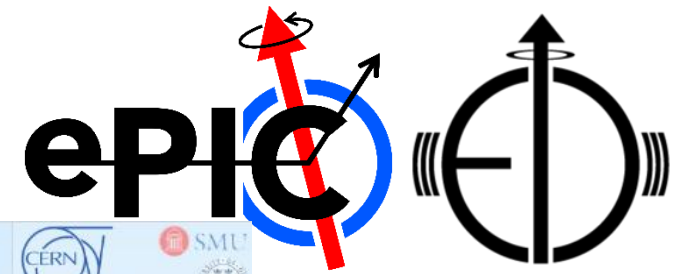
- Temperature: -35 to + 60 °C
- Total Dose: 100 Mrad
- Total Fluence:  $1 \times 10^{15}$  n/cm<sup>2</sup> and  $1 \times 10^{15}$  hadrons/cm<sup>2</sup>

- **Status**

- Pre-production ongoing
- Solving problems with module assembly
  - Alignment of optical components
- Ramping up to 2k modules/month in 2023



# VTRx+ connectors



## 1.2 VTRx+ Pigtail



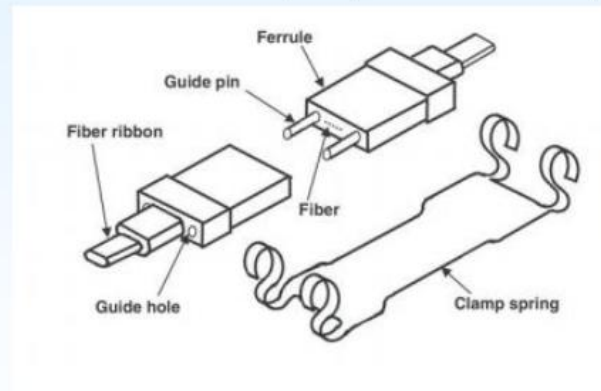
- Pigtail being finalized

- Rad hard fibre
- 5 individual fibres in loose tube
- MT termination
- Not dismountable

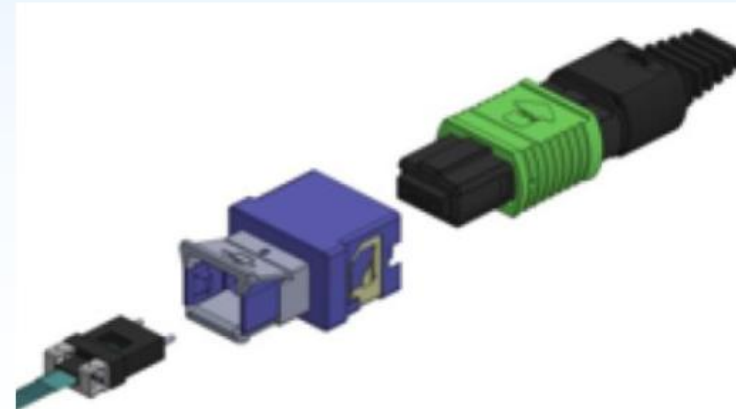


- Connection with MT Spring Clamp

- Dense connectivity at expense of handleability



Or with MT to MPO adapter  
if you have space



From:  
<https://indico.cern.ch/event/799025/contributions/3486288/>



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09 July 2025

TWEPP, 3 Sep 2019

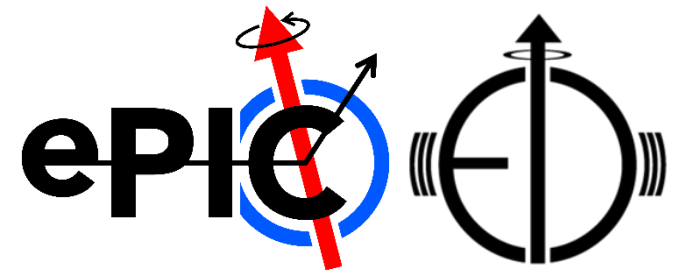
francois.vasey@cern.ch  
ePIC SVTworking meeting @ SBU

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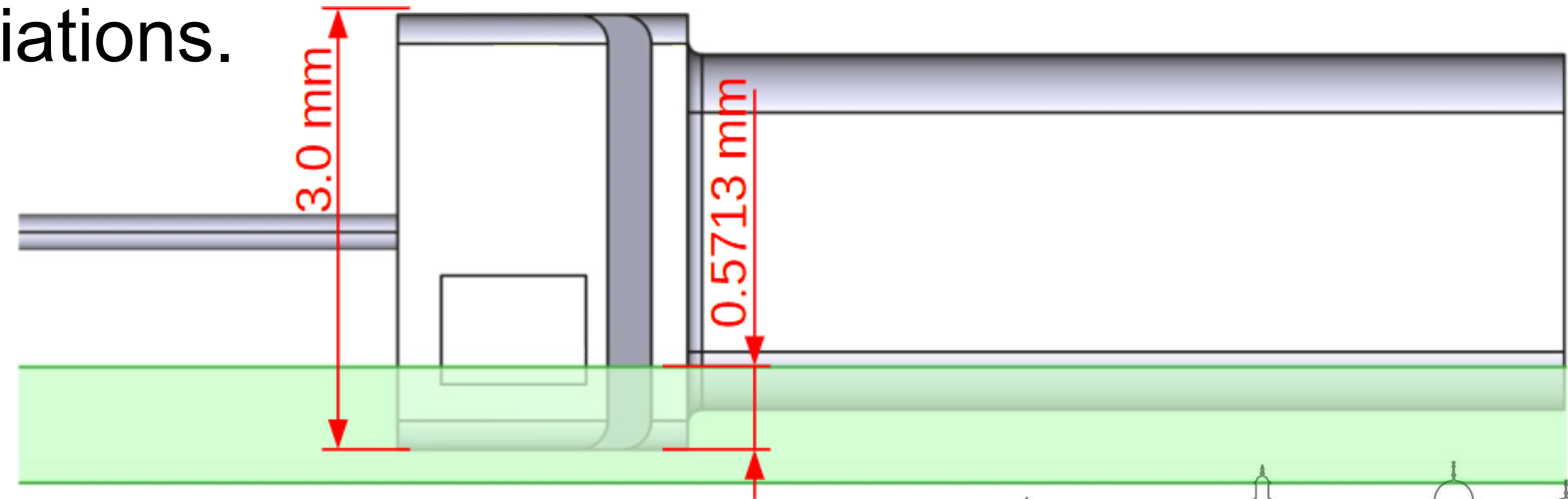
27



# Connector issue



- The connector that CERN supply on the end of the fibres is thicker than the VTRx+ with clip.
- Fibres cannot lay completely flat.
- Need to look at options for mounting the connector to the PCB with adjustable position – to account for connector thickness and fibre length variations.





# Services – VTRX+

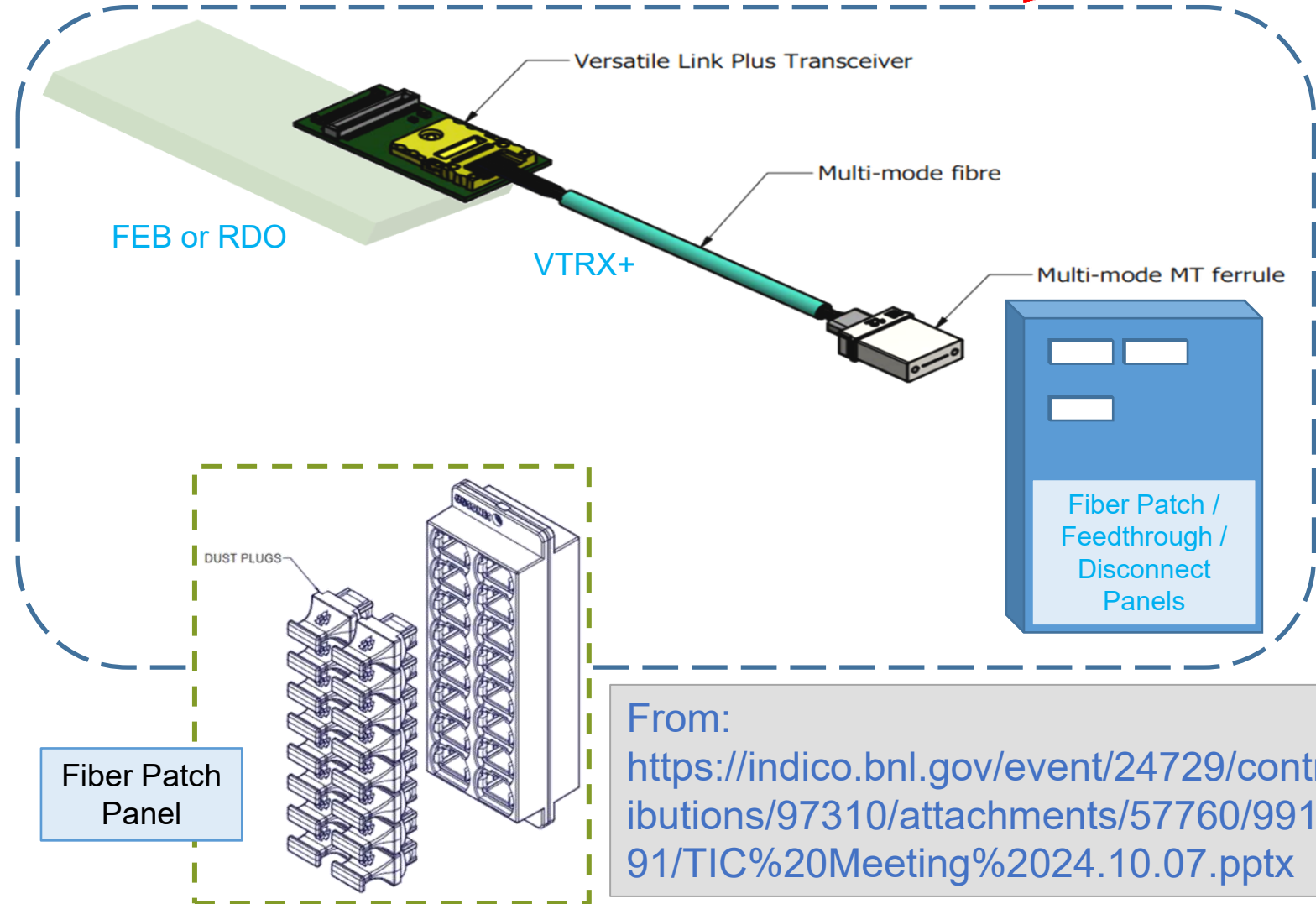
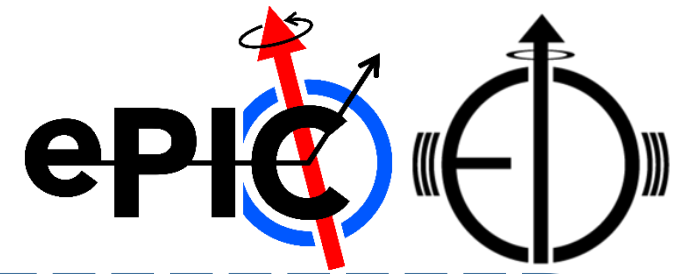
- Recently switch all applicable detectors over from RDOs to VTRX+ modules
- Modules will be placed on each detector
- The modules can only push the signal up to 2m in length so there needs to be a fiber patch to convert to MTP fiber
- Each module gets 1 fiber patch, locations will vary from detector to detector
- Total VTRX+ modules needed listed below

| Sub-Detector | Qty  |
|--------------|------|
| SVT          | 1579 |
| MPGD EE      | 64   |
| MPGD HE      | 64   |
| MPGD IB      | 128  |
| MPGD uRwell  | 384  |
| TOF Disk     | 212  |
| TOF Barrel   | 288  |
| dRICH        | 1242 |
| pfRICH       | 68   |

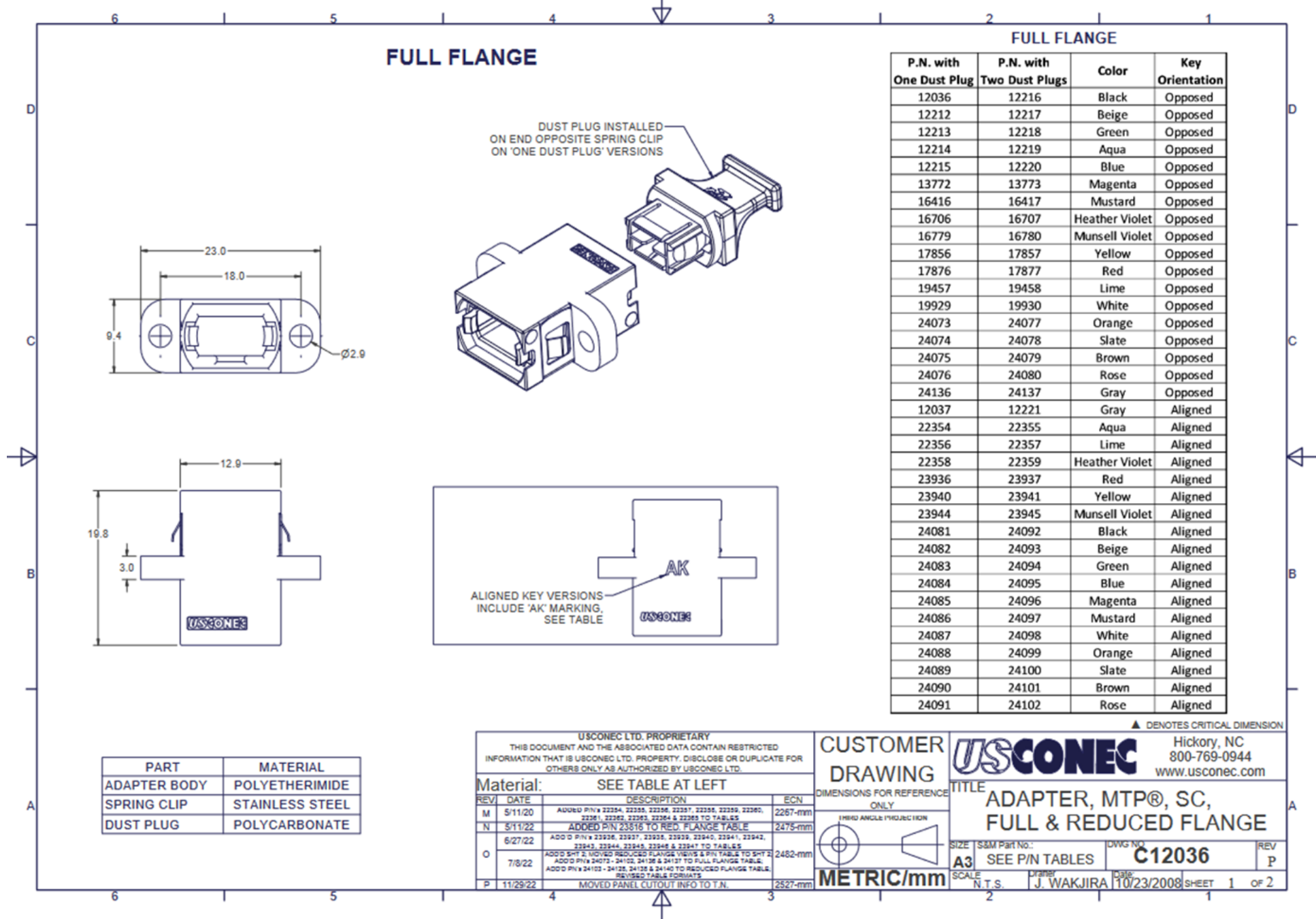


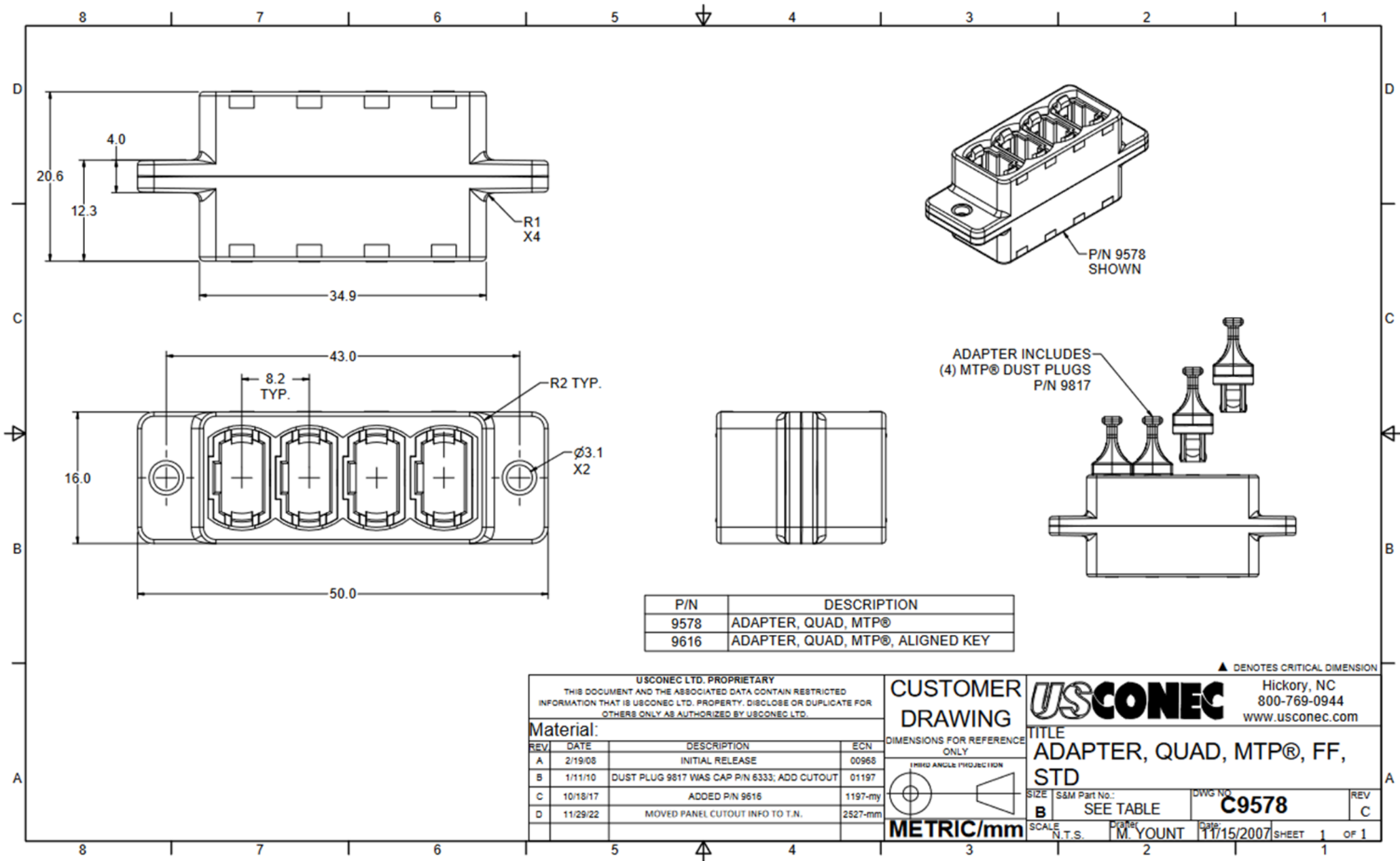
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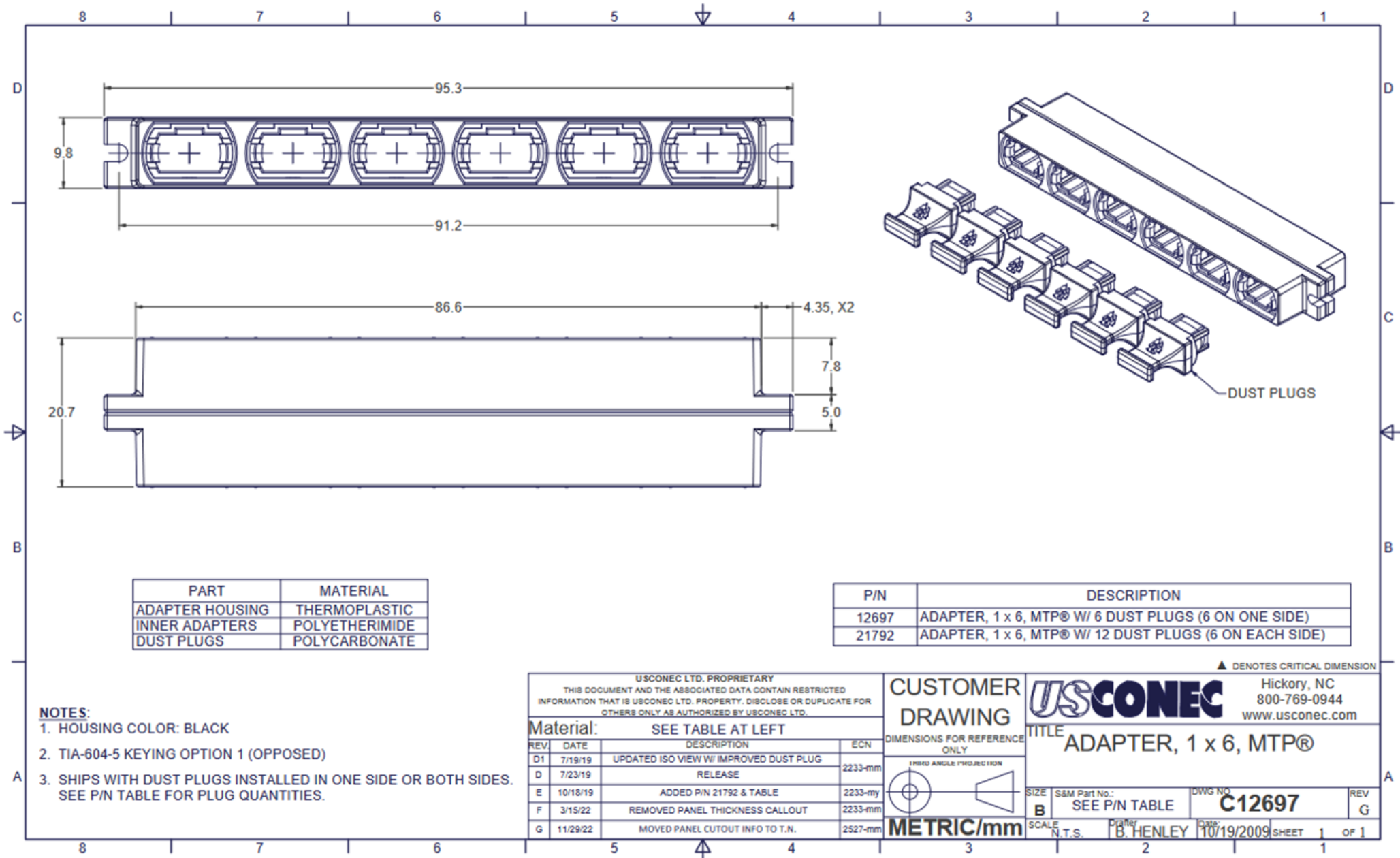


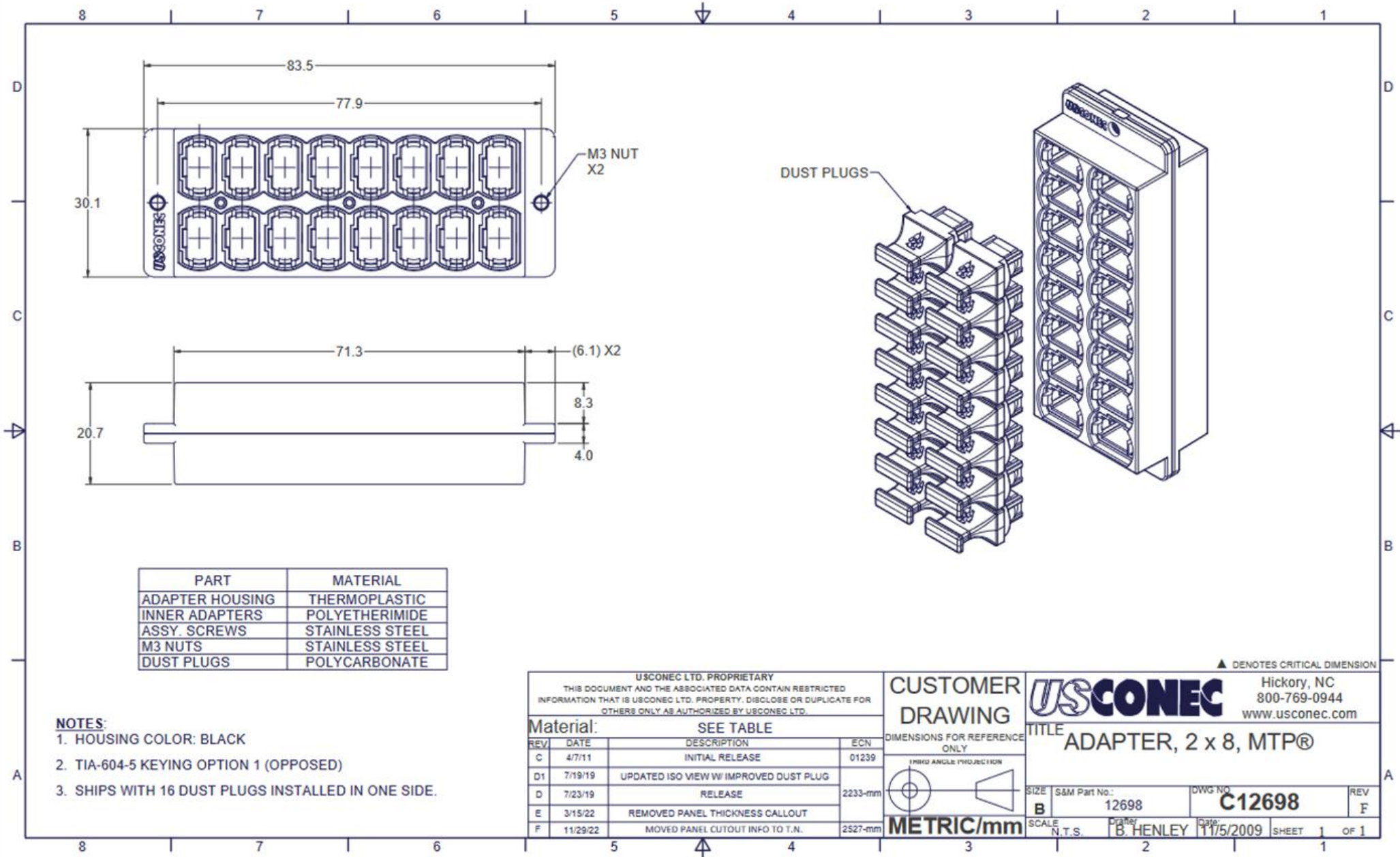
From:  
<https://indico.bnl.gov/event/24729/contributions/97310/attachments/57760/99191/TIC%20Meeting%2024.10.07.pptx>



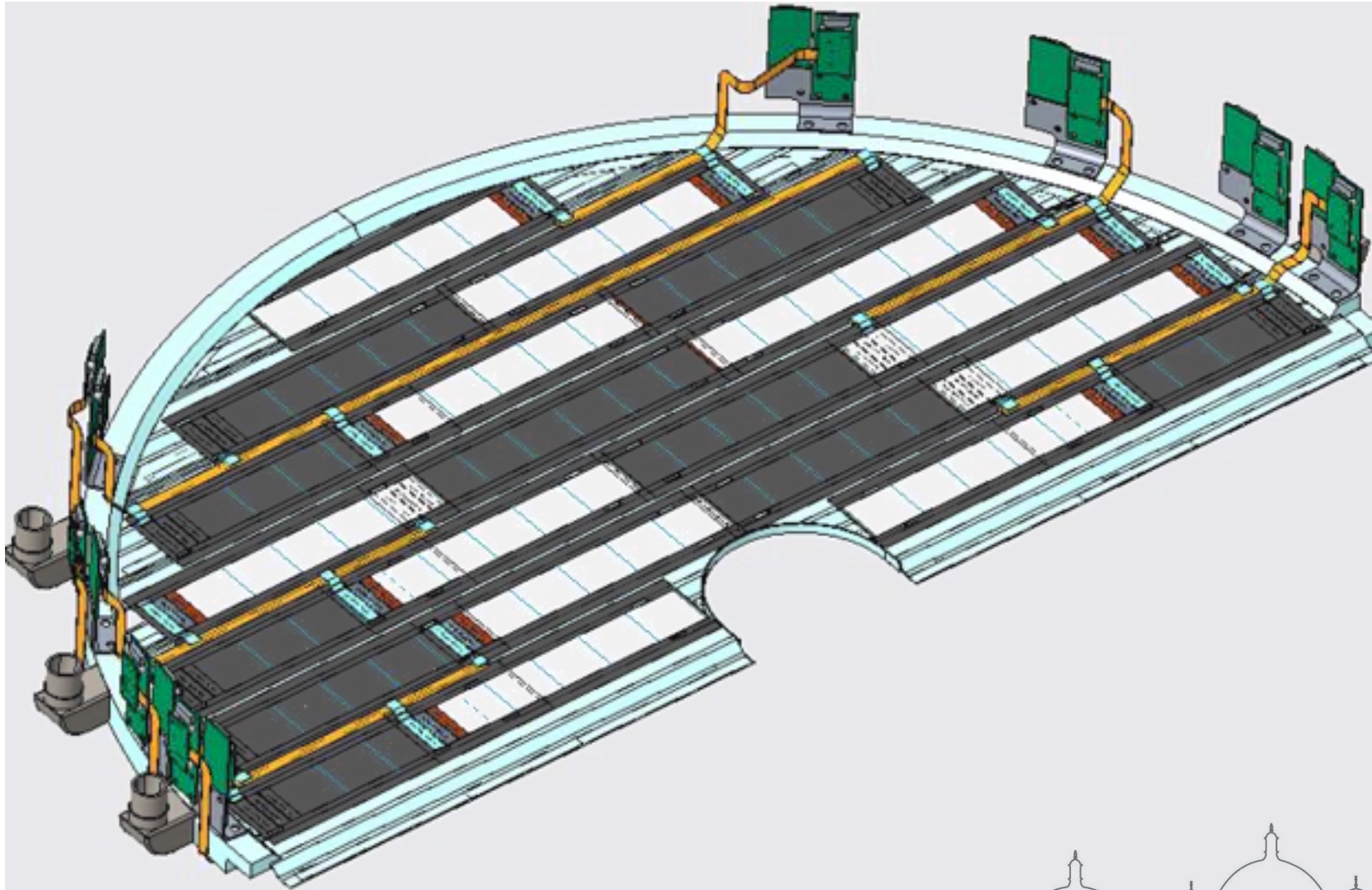
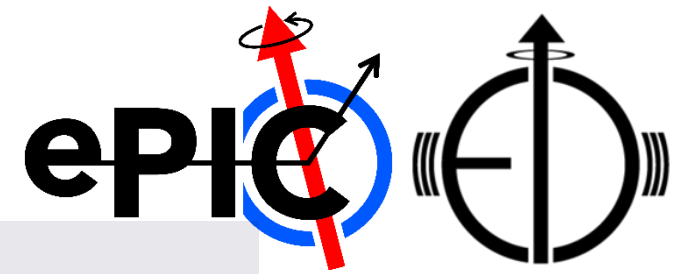








# ED/HD0 – Back



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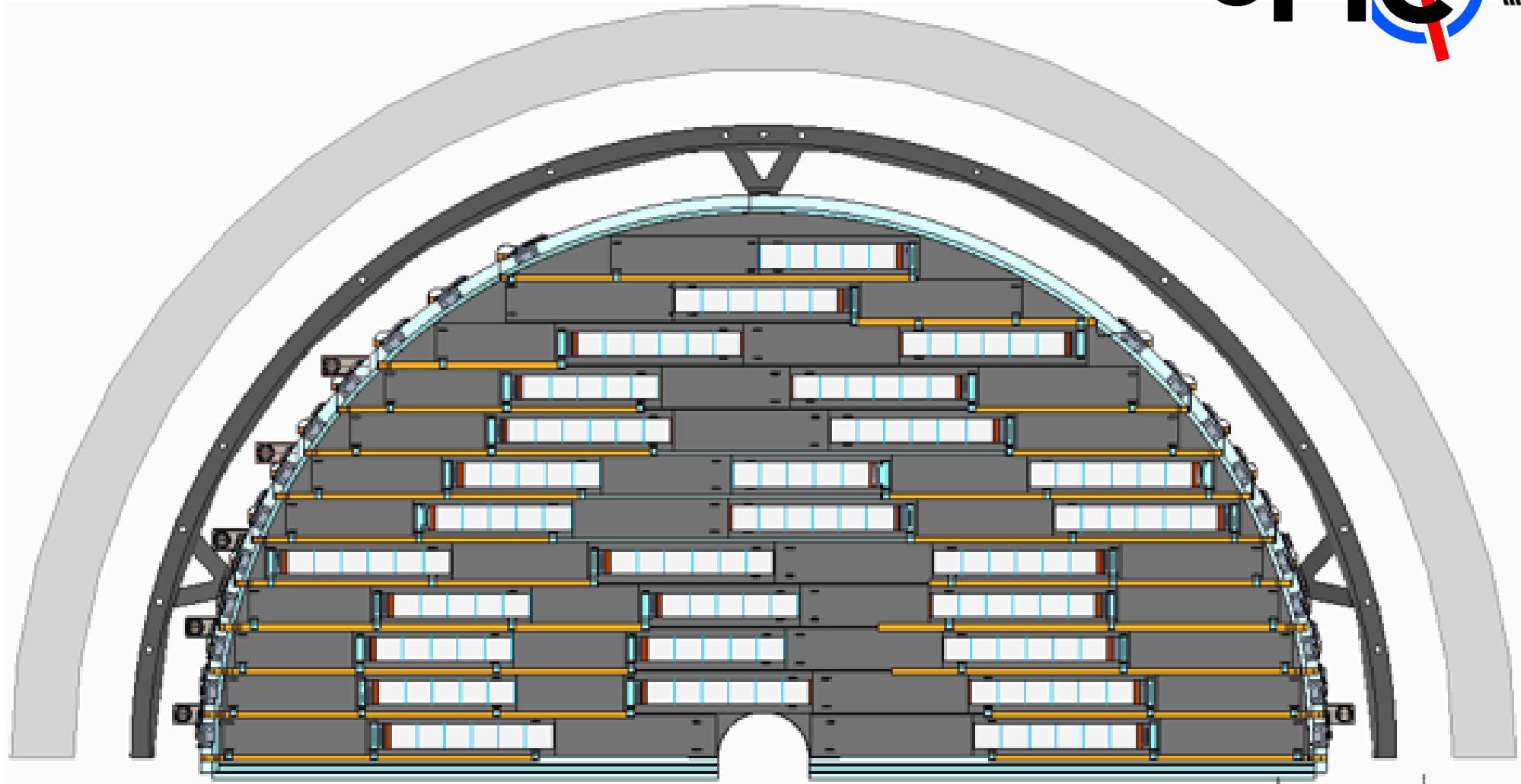
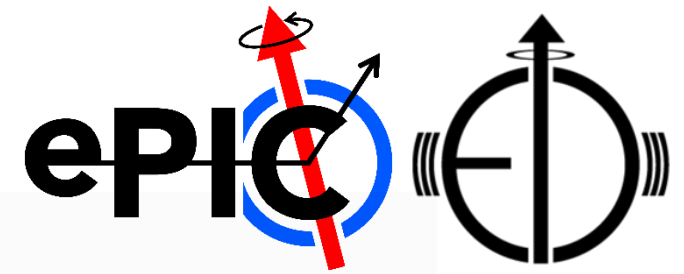
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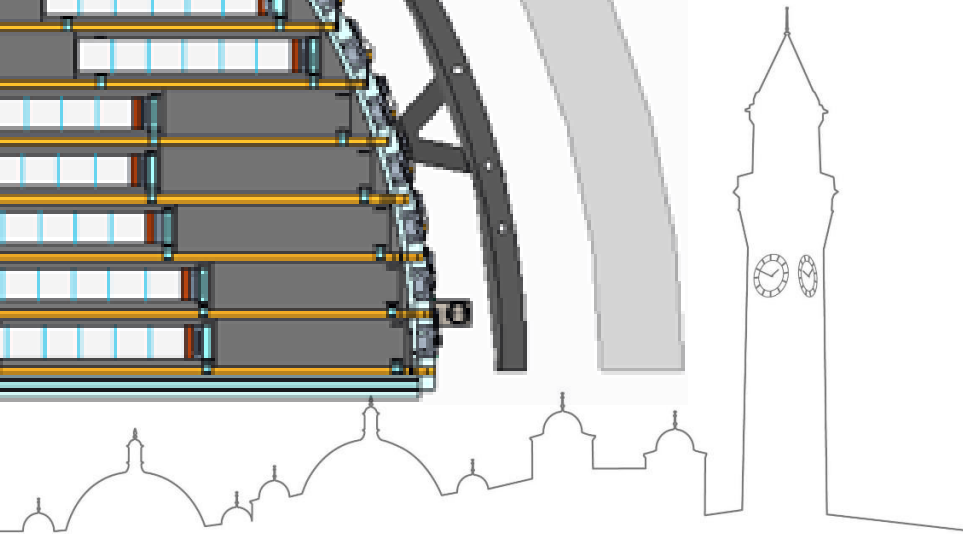
# ED/HD1to4 – Back



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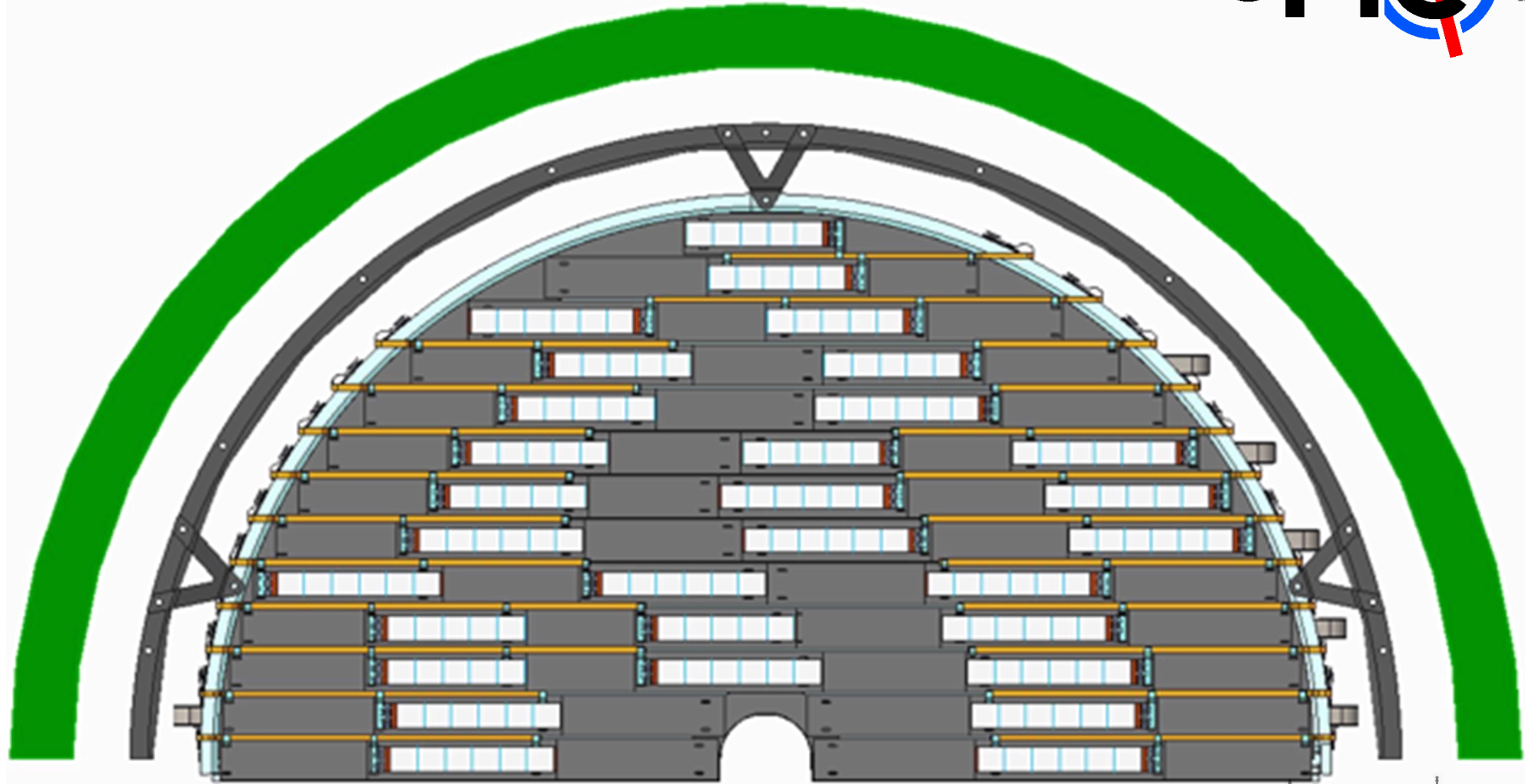
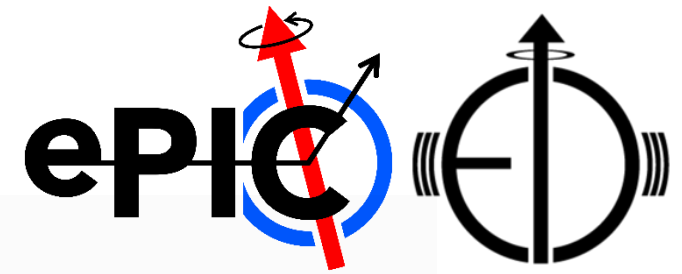
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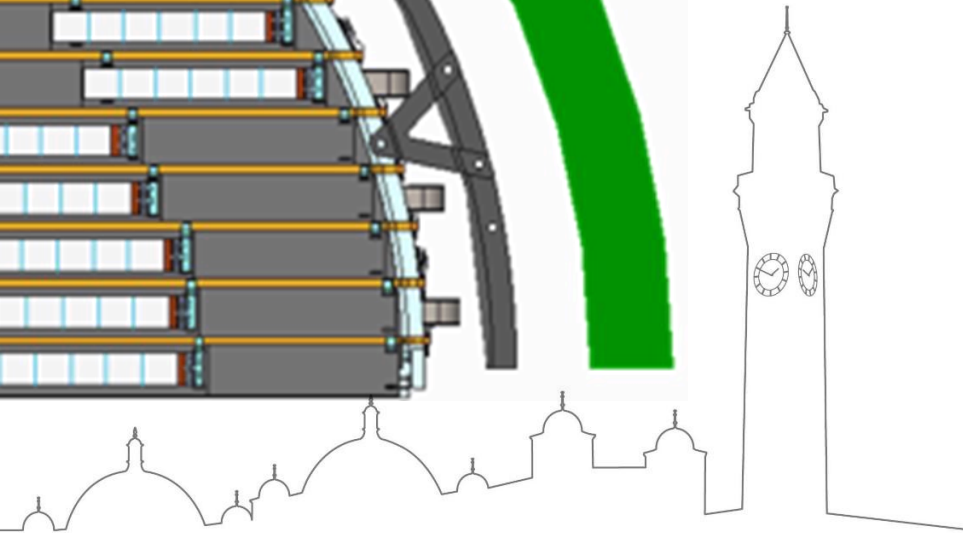
# ED/HD1to4 – Front



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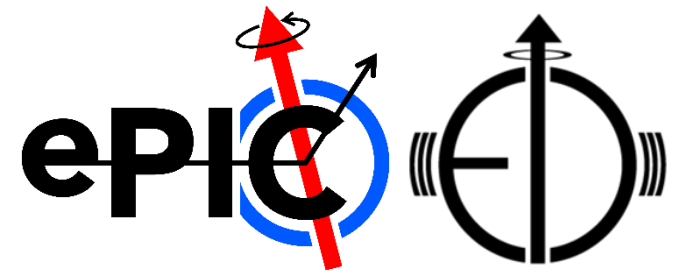
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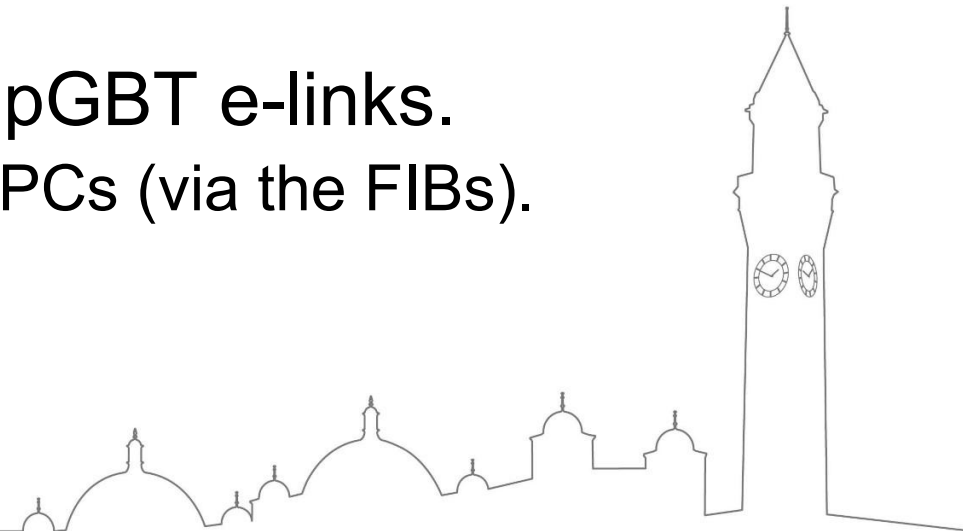


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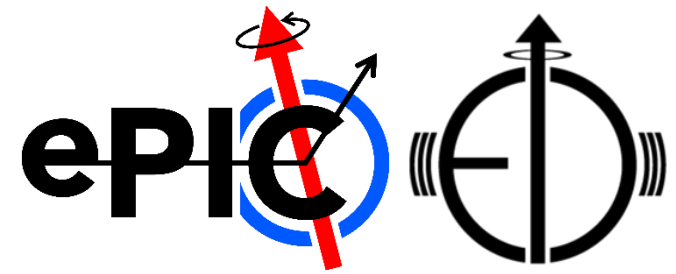
# FPC-Control Board dimensions



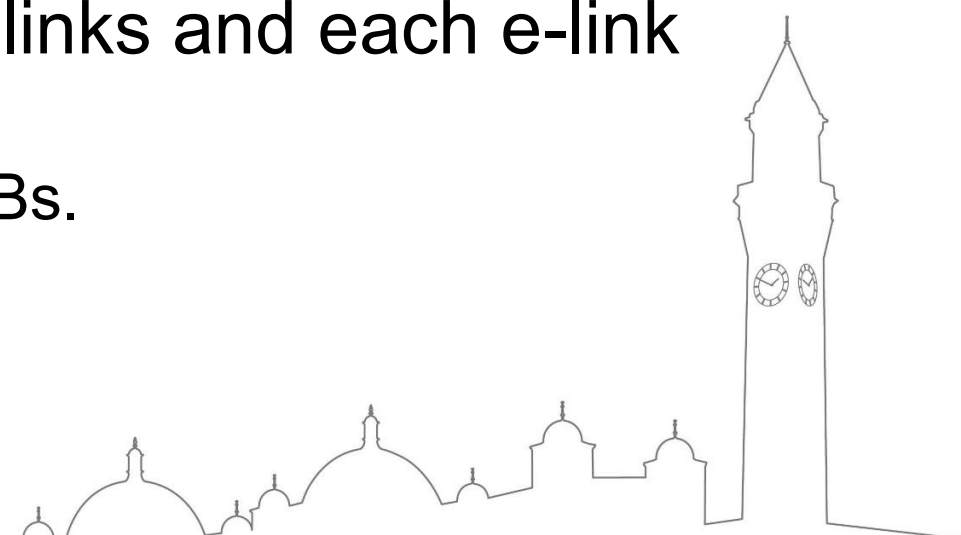
- Assumed 65 \* 30 mm additional area to enable the addition of IpGBT, power regulation & monitoring to the area of the FPC Interface Board (FIB).
- Board dimensions become 65 \* 47.5 mm
- Package height could be 20 mm (if DC/DC are used).
- FPC slow controls planned to be sent via IpGBT e-links.
  - 1 FPC-Control Board connects to (up to) 12 FPCs (via the FIBs).
  - 4 e-links saved for internal FPC-CB use.



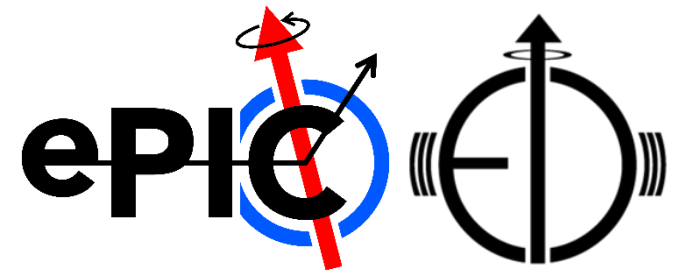
# FIB-Control Board dimensions



- Assumed 65 \* 22.5 mm additional area to enable the addition of 12 serial multiplexers to the area of the FPC-Control Board.
- Board dimensions become 65 \* 70 mm
- Package height could be 20 mm (if DC/DCs are used).
- If FIB slow controls utilise the 12 lpGBT e-links and each e-link connects to a 1:4 serial multiplexer.
  - 1 FIB-Control Board connects to (up to) 48 FIBs.
  - 4 e-links saved for internal FIB-CB use.



# Powering the FPC-Control Board

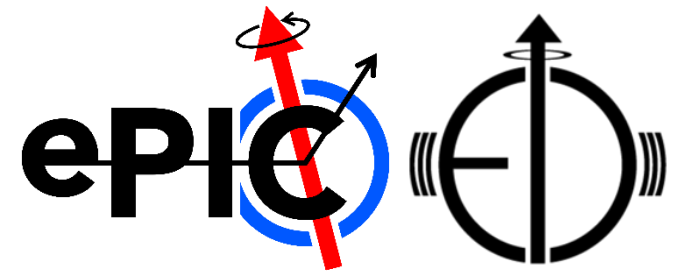


- Only on board powering needs: VTRx+ and IpGBT – ~2W!
  - All 2W dissipated on this board.
- ~104 of these control boards needed for whole SVT.
- Could be supplied by 54V @ 40mA.
- 0.25 mm wire diameter needed.
  - Assuming aluminium wire and a V-drop of 10% over 100m.
- ~208 wires needed (source and return lines) from PSU to SVT.





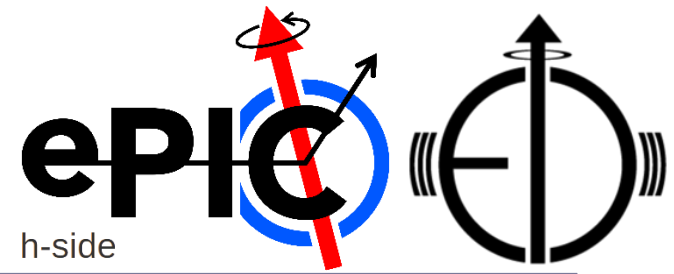
# Powering the FIB-Control Board



- Only on board powering needs: (many) serial multiplexers.
- External powering needs: up to 48 VTRx+ – ~36W!
  - Centralised power for up to 48 FIBs.
  - About 22W burnt off on the board – (water) cooling needed!
- Few of these control boards needed for whole SVT (~32).
- Could be supplied by 54V @ 0.75A.
- 1.1 mm wire diameter needed.
  - Assuming aluminium wire and a V-drop of 10% over 100m.
- ~64 wires needed (source and return lines) from PSU to SVT.



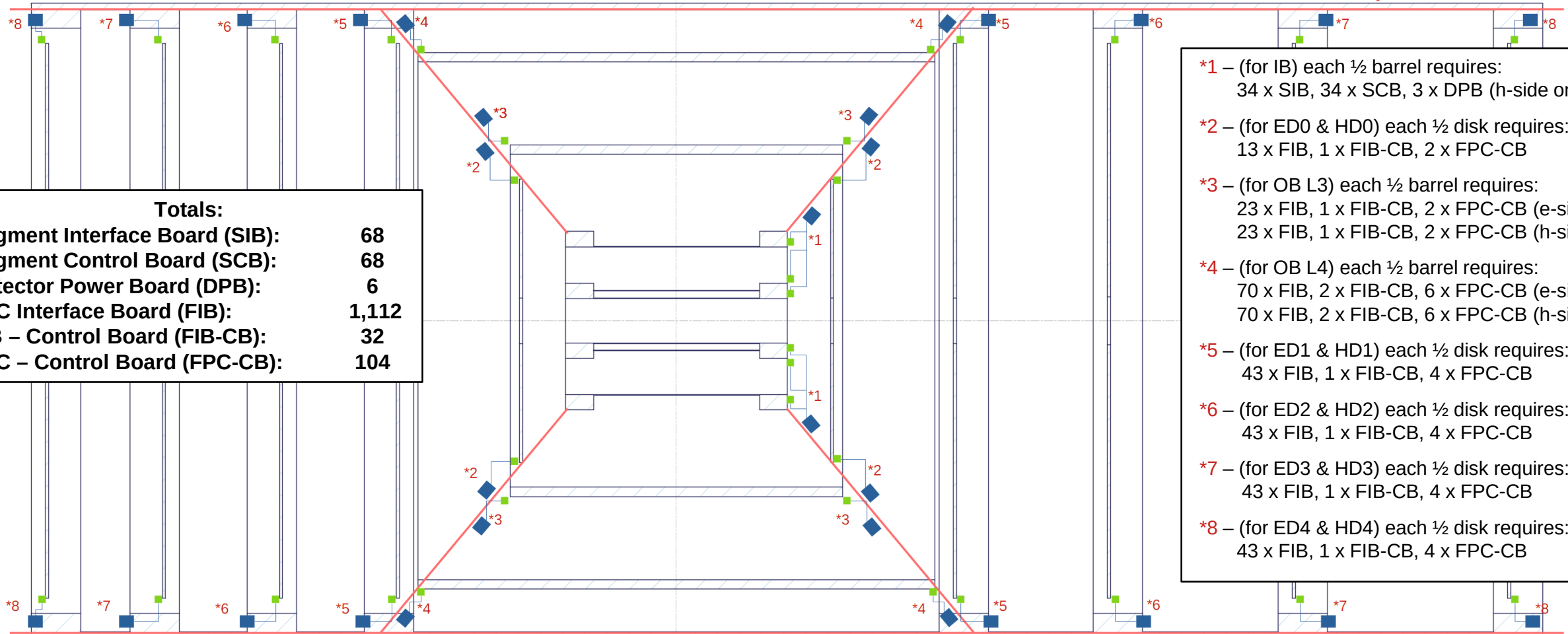
# Old OB/Disk RDO board layout



Out of date

e-side

h-side



## Totals:

|                                |       |
|--------------------------------|-------|
| Segment Interface Board (SIB): | 68    |
| Segment Control Board (SCB):   | 68    |
| Detector Power Board (DPB):    | 6     |
| FPC Interface Board (FIB):     | 1,112 |
| FIB – Control Board (FIB-CB):  | 32    |
| FPC – Control Board (FPC-CB):  | 104   |

- \*1 – (for IB) each ½ barrel requires:  
34 x SIB, 34 x SCB, 3 x DPB (h-side only)
- \*2 – (for ED0 & HD0) each ½ disk requires:  
13 x FIB, 1 x FIB-CB, 2 x FPC-CB
- \*3 – (for OB L3) each ½ barrel requires:  
23 x FIB, 1 x FIB-CB, 2 x FPC-CB (e-side)  
23 x FIB, 1 x FIB-CB, 2 x FPC-CB (h-side)
- \*4 – (for OB L4) each ½ barrel requires:  
70 x FIB, 2 x FIB-CB, 6 x FPC-CB (e-side)  
70 x FIB, 2 x FIB-CB, 6 x FPC-CB (h-side)
- \*5 – (for ED1 & HD1) each ½ disk requires:  
43 x FIB, 1 x FIB-CB, 4 x FPC-CB
- \*6 – (for ED2 & HD2) each ½ disk requires:  
43 x FIB, 1 x FIB-CB, 4 x FPC-CB
- \*7 – (for ED3 & HD3) each ½ disk requires:  
43 x FIB, 1 x FIB-CB, 4 x FPC-CB
- \*8 – (for ED4 & HD4) each ½ disk requires:  
43 x FIB, 1 x FIB-CB, 4 x FPC-CB



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[Back to new version.](#)

- Carbon fibre support structure (tube and cone)
- Electronics boards (Interface Boards)
- Electronics boards (Control Boards/Power Boards)