



AncBrain Hardware Emulation

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in collaboration with BNL team

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- **eRD113 FY25:**

- Slow Control, Synchronization and Monitoring Path of the ancillary ASIC (aka ancillary ASIC Brain):
 - Hardware Description Language (Verilog/SystemVerilog) code of the Slow Control, Synchronization and Monitoring Path of the ancillary ASIC allowing timing analysis and physical implementation (P&R),
 - Simulation test-bench and functional verification achieved with models of lpGBT and MOSAIX interfaces,
 - FPGA emulation of the functionality developed based on the hardware description of the slow control, synchronization and monitoring component of the ancillary ASIC compatible with lpGBT and EIC-LAS interfaces, allowing elimination of bugs and validation of code for implementation in Si

- **LBL deliverable:**

- FPGA emulator for the Control Manager developed based on the hardware description of the slow control, synchronization and monitoring component of the ancillary ASIC
 - FPGAs allow designers to create a hardware model of the ASIC design, enabling them to test and verify functionality before committing to the expensive and time-consuming process of ASIC manufacturing. This early verification helps catch design flaws, reduce development risks, and accelerate overall design cycle
 - Allow development of testing platform including control software and hardware interfaces w/o actual chip

Defining Expectations from the Hardware Mock-up

Key Outputs:

- **Proof-of-concept signal integrity:** Verify that the lpGBT $\rightleftharpoons$ AncASIC $\rightleftharpoons$ LAS signaling scheme (SCL @160MHz/320MHz/80MHz CML, slow-control SC_In/Out, 5MHz Manchester link, broadcast SYNC/RESET with delay line, etc.) works on real copper traces and connectors.

⇒ Start with standard cables.

⇒ Replace by FPCs when available (timescale uncertain, but likely after 9/2025)

- **Co-verification with FPGA model:** Run the SystemVerilog AncBrain RTL (in the FPGA) against the discrete hardware so we can close the loop on register access timing, Manchester encoding, CRC/parity handling, error injection, and broadcast delay-line skew.

⇒ Start with lpGBT and FPGAs running AncBrain and MOSAIX RTL.

⇒ Replace by AncASIC MPW1 (after 9/2025) and MOSAIX/LAS when available (after 11/2025)

- **Early power/thermal sanity:** Exercise NBVG & SLDO dummy loads → measure LDO drop-out, negative-bias levels, watchdog/over-temperature trip logic

⇒ Separate from AncBrain hardware emulation (after 9/2025)

- **Foundation for later radiation testing.**

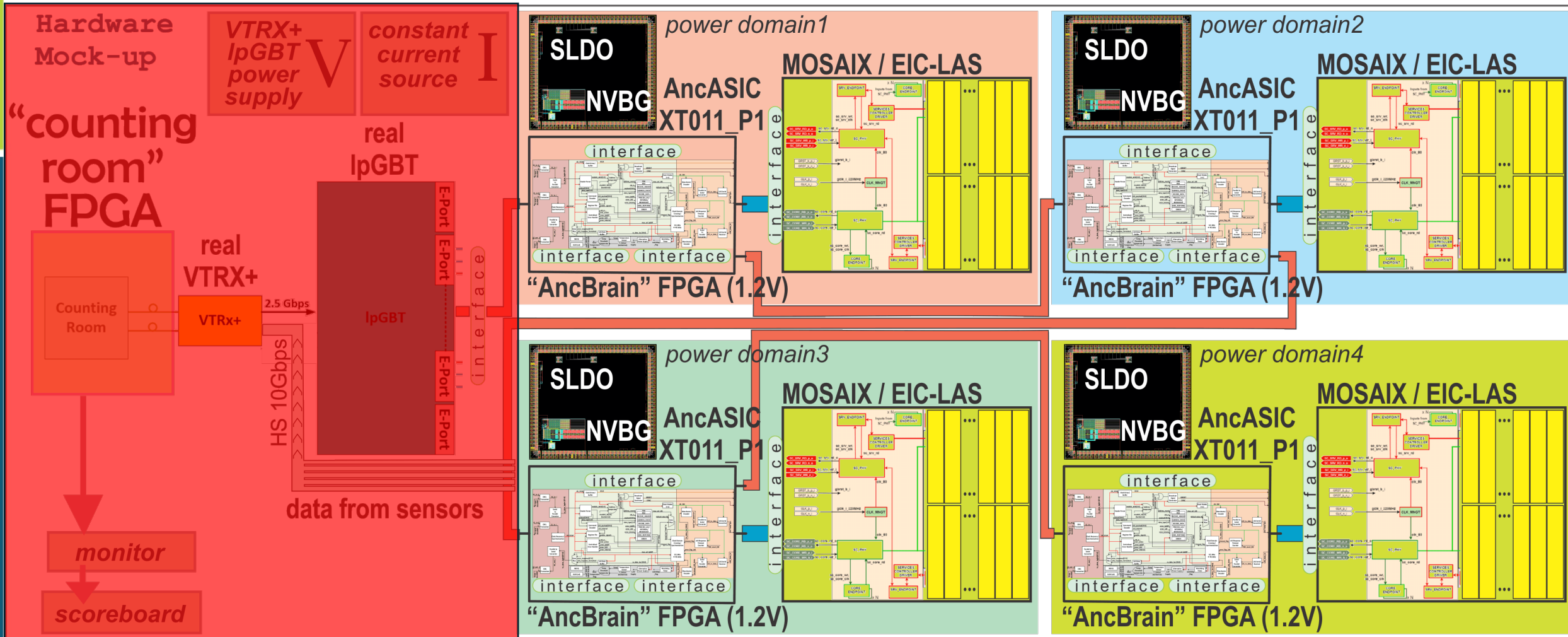
⇒ After 3/2026

Assumptions:

- receive MPW1/MPW2 in 9/2025
- receive MOSAIX in 10/2025
- Submit AncBrain in 8/2025 and receive in 3/2026

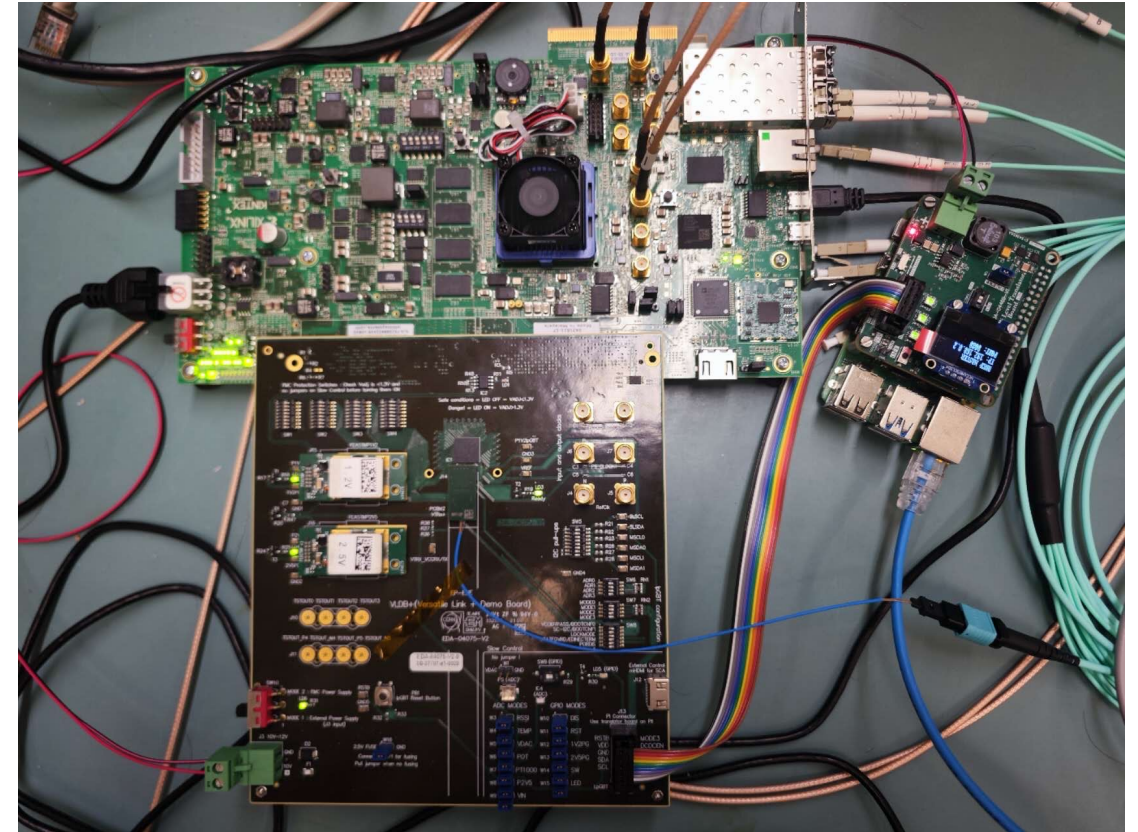
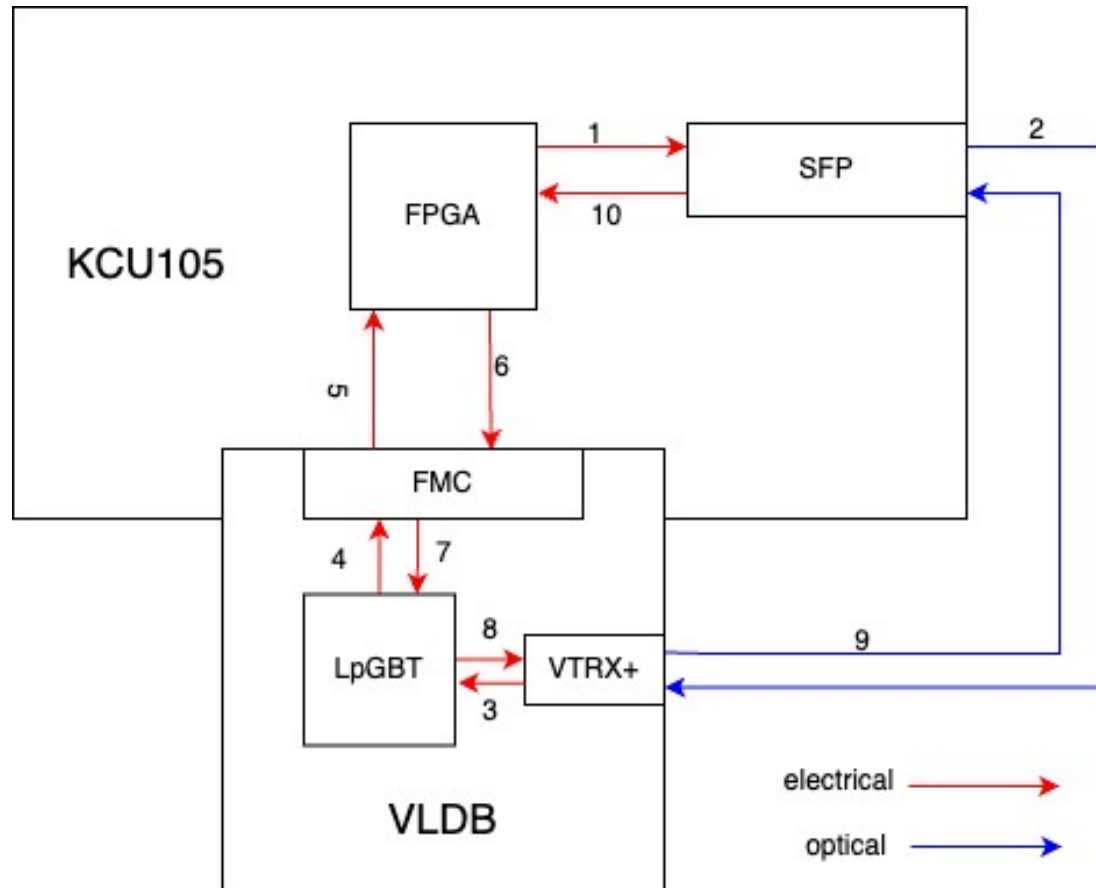
- **Finalize (functional) requirements of AncBrain - BNL team**
 - In view of Marcello's identified need of passing MOSAIX output and/or monitoring dark currents
- **Code sharing**
 - **Software emulation code – BNL team**
 - ⇒ **First commit onto Github on 5/22/2025**
 - ⇒ **Newer version on Github on 6/25/2025**
- **Decision on AC/DC coupling for slow control data**
 - **Physically verified if possible – LBNL team**
 - ⇒ **DC: place multiple FPGAs at different DC levels and DC-connect their CML interface, establish reliable I/O**
 - ⇒ **AC: place multiple FPGAs at the same DC level and AC-connect their CML interfaces, establish robust synchronization with up to 4ns delay due to signal transmission from the first to the last AncASIC.**
 - Determine the resources needed to achieve such synchronization**
- **Powering of AncASIC**
 - Power on sequence implementation in FPGA
 - Handling emergency implementation in FPGA

Design Verification – hardware emulation



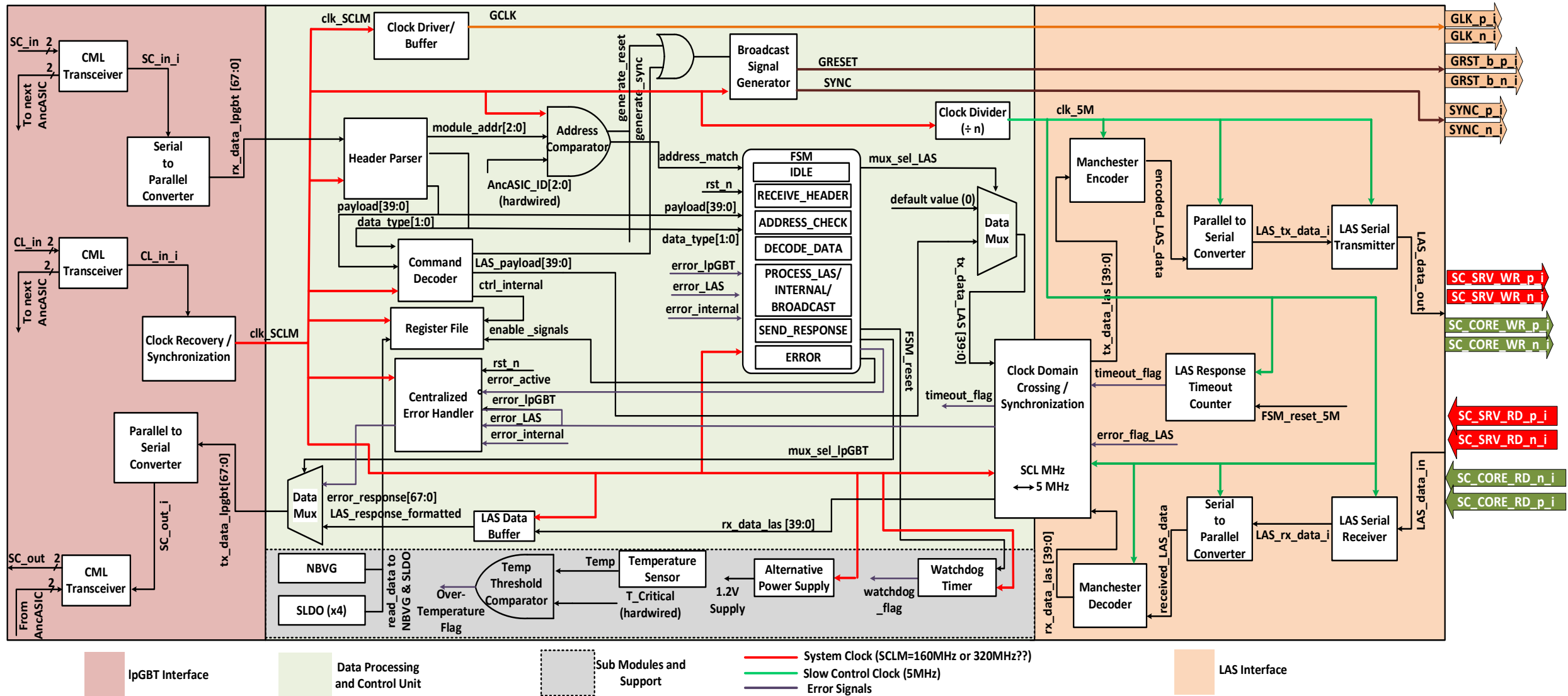
- **Software Mockup (BNL) – needed for functional verification before implementation**
 - to verify code coverage, find exceptional situations, and reduce risks → single step implementation.
- **Hardware mockup (LBL)– needed to perform verification in experiment like environment**

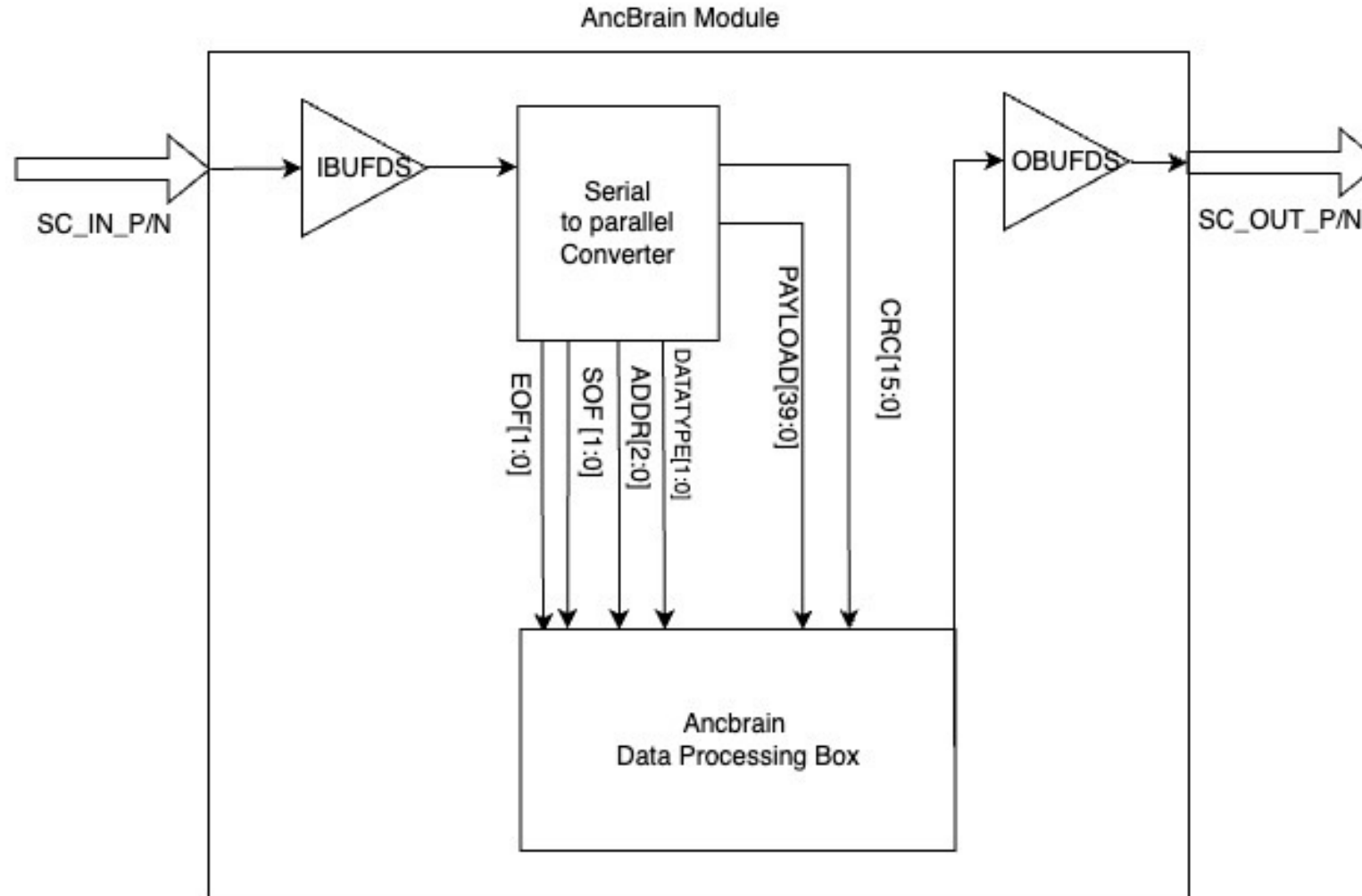
“Control Room FPGA + RDO”



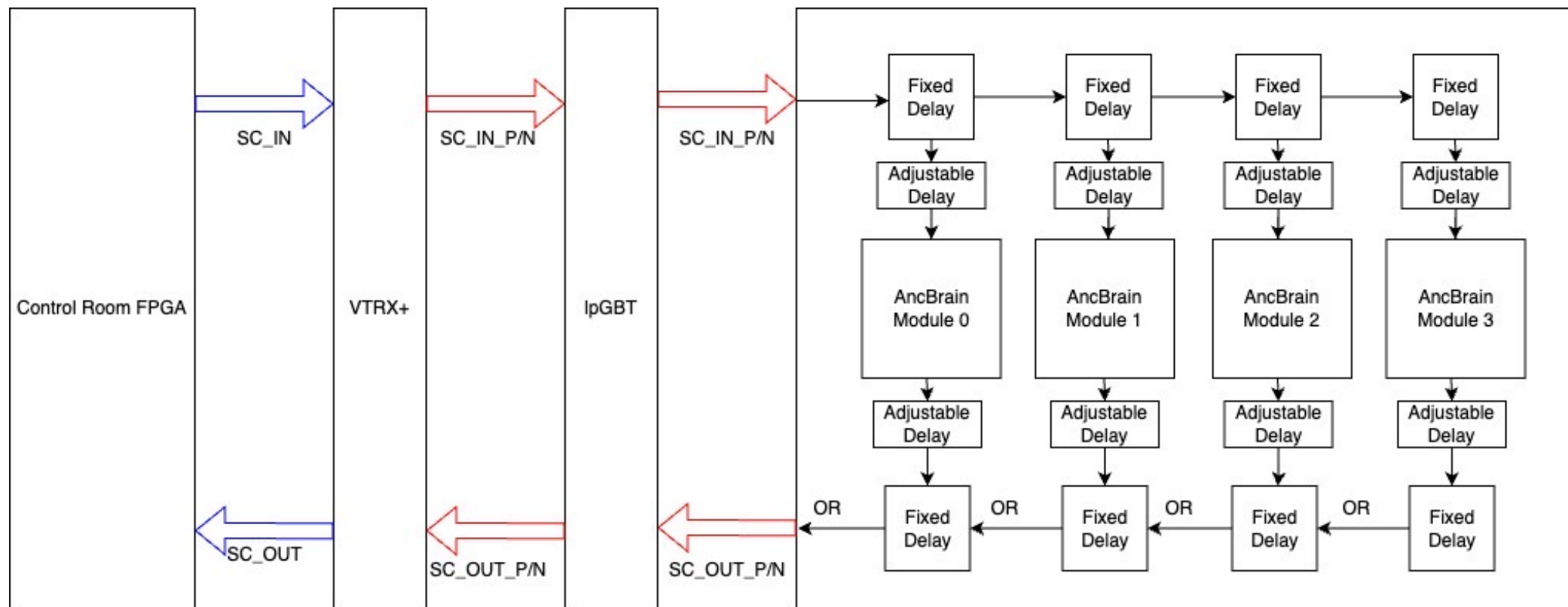


EIC-AncBrain Block Diagram

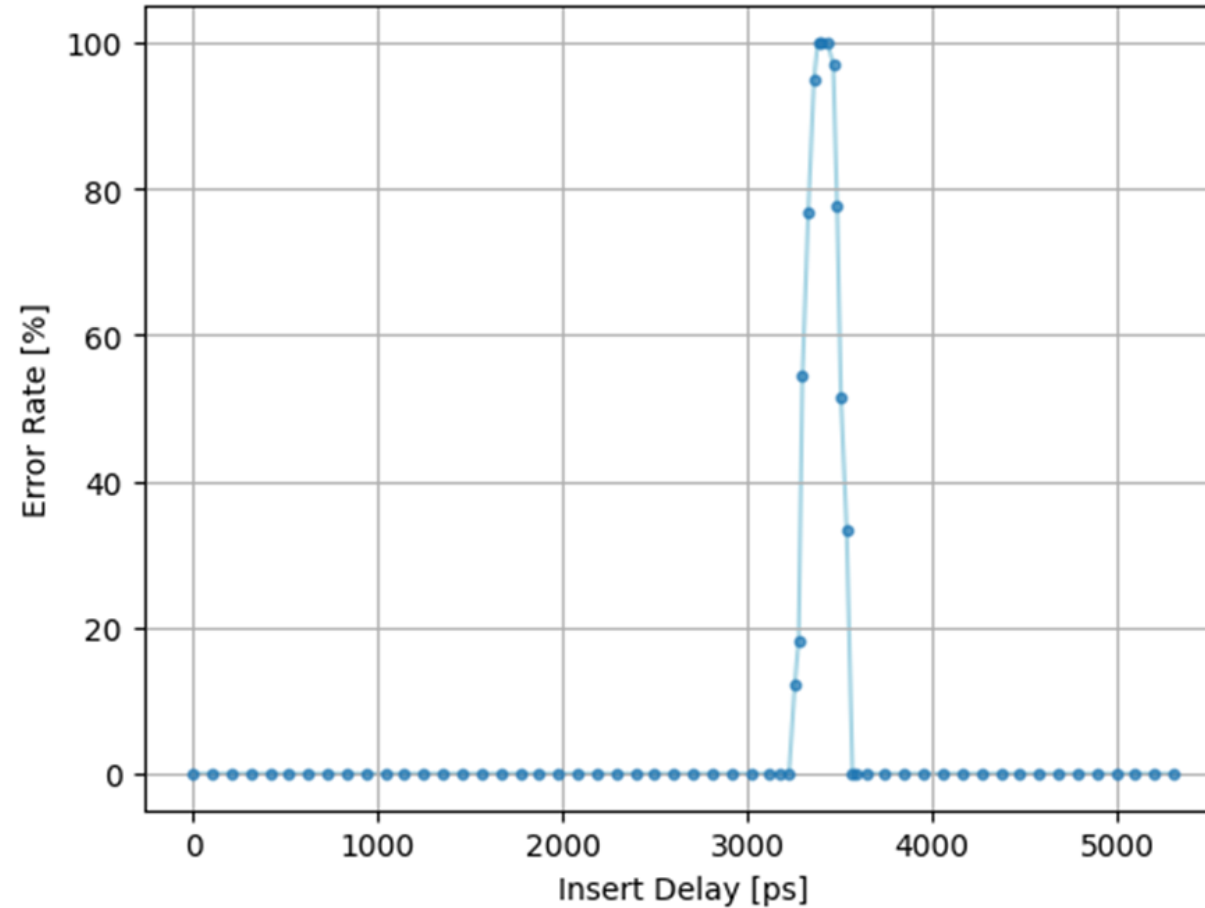




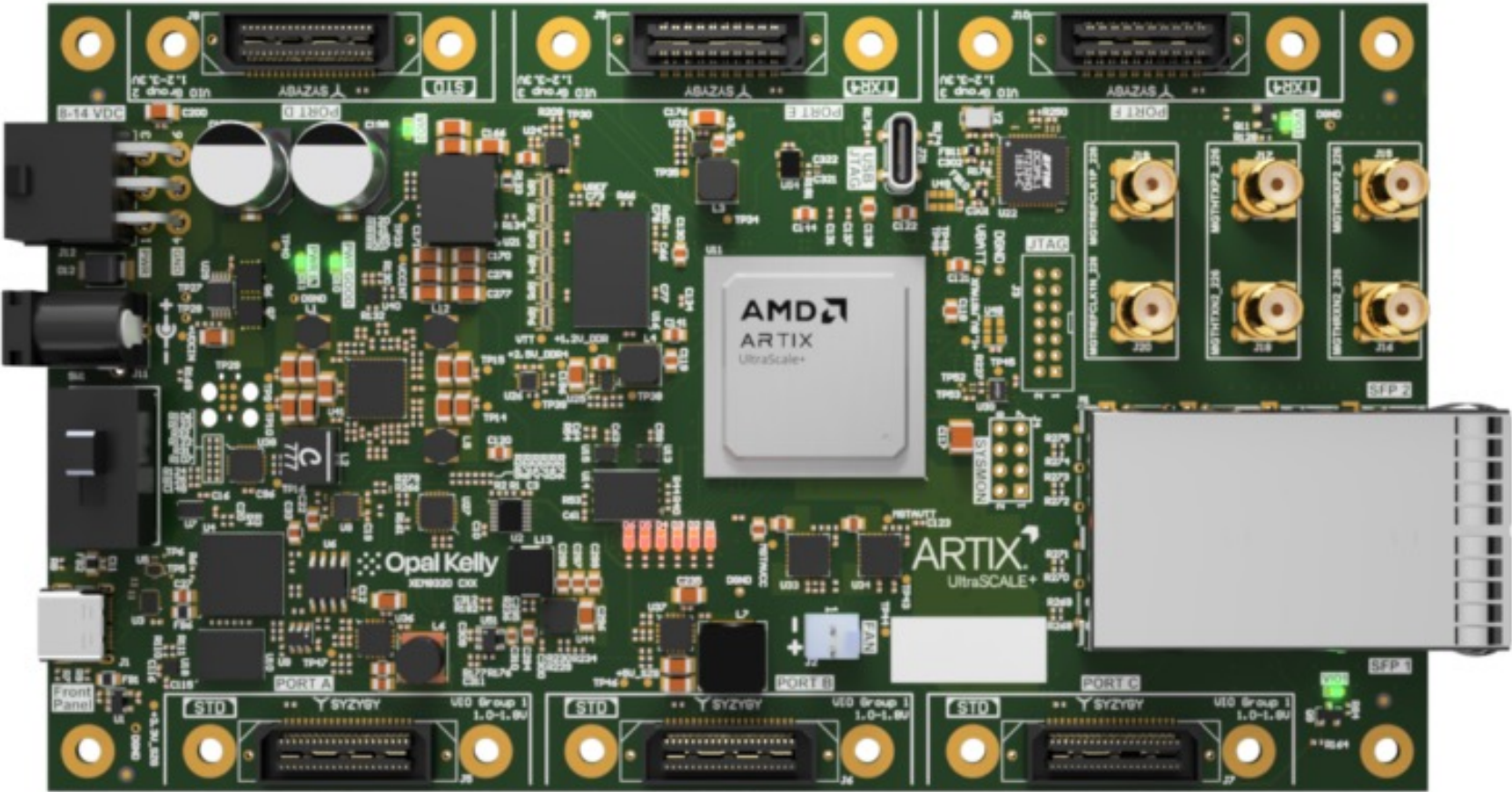
Multidrop Investigation



SC_Out Delay Scan – lpGBT Receiver Metastability



XEM8320 GTY on SMA/SYZYGY



FPGA GT TX/RX using CML transceivers

RX Analog Front End

Functional Description

The RX analog front end (AFE) is a high-speed current-mode input differential buffer (see Figure 4-1). It has these features:

- Configurable RX termination voltage
- Calibrated termination resistors

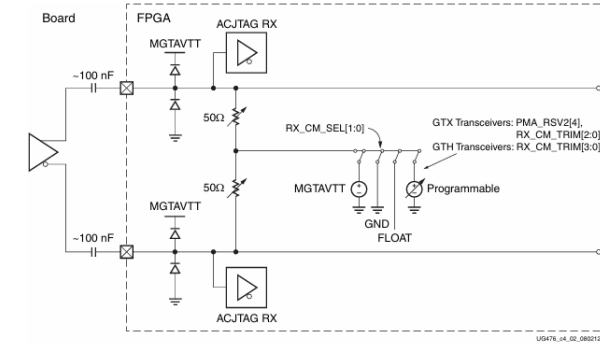


Figure 4-2: RX Analog Front End

Note: The ACJTAG blocks in Figure 4-2 are part of the JTAG test chain.

TX Configurable Driver

Functional Description

The GTX/GTH transceiver TX driver is a high-speed current-mode differential output buffer. To maximize signal integrity, it includes these features:

- Differential voltage control
- Pre-cursor and post-cursor transmit pre-emphasis
- Calibrated termination resistors

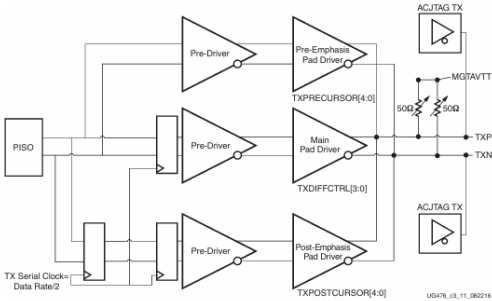
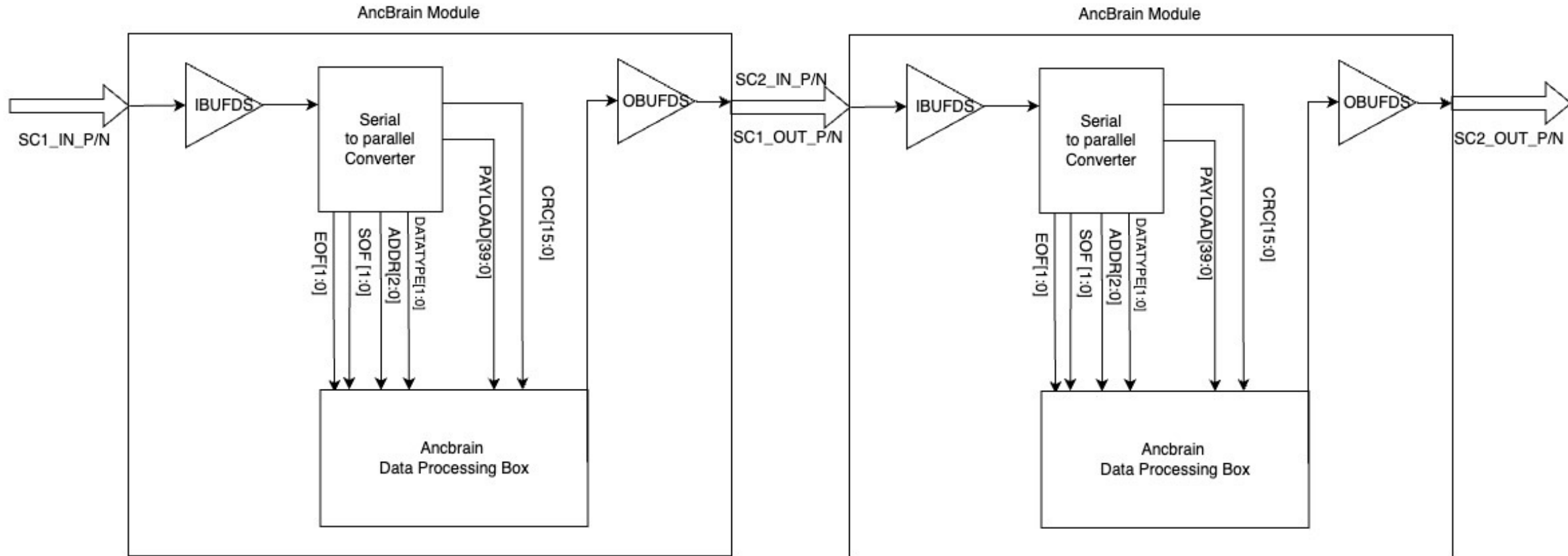


Figure 3-29: TX Configurable Driver Block Diagram

Note: The ACJTAG blocks in Figure 3-29 are part of the JTAG test chain.

DC/AC Coupling Investigation



- AC coupling successful – no surprise
- DC coupling between 8320's at different potential (stacked PSs, separate PC and clock source) **in progress**

Summary and Outlook

- Working on FPGA-based AncBrain hardware emulation platform
 - Have established readout using KCU105 FPGA/lpGBT/VTRX+ for AncBrain hardware emulation
 - Multidrop => managed to have a working setup but will discontinue due to decision to go with daisy chain
 - AC vs DC coupling => in progress
 - Converting ASIC RTL into XEM8320 FPGA => have started, will complete in ~2 weeks
 - Develop control software and hardware interfaces => allow early development before the actual chip arrives in 3/2026
- Integrate AncBrain emulator with AncASIC MPW1, MOSAIX and FPC
 - MPW1:
 - Carrier card design and assembly (schematic design from BNL?): before 10/2025
 - Mount and test MPW1: 10/2025-3/2026 (TBC)
 - CML transceivers: AC vs DC
 - NVG: goals TBD
 - SLDO pre-regulator: goals TBD
 - MOSAIX
 - Emulator: hardware (Altera Aria10 FPGA and lpGBT/VTRX+) acquired, ITS3 FW under investigation
 - MOSAIX: after 11/2025