Sensor and AncASIC Update

Iain Sedgwick

UK WP1 F2F Meeting
June 26th 2025

Introduction

SVT Silicon Scheme

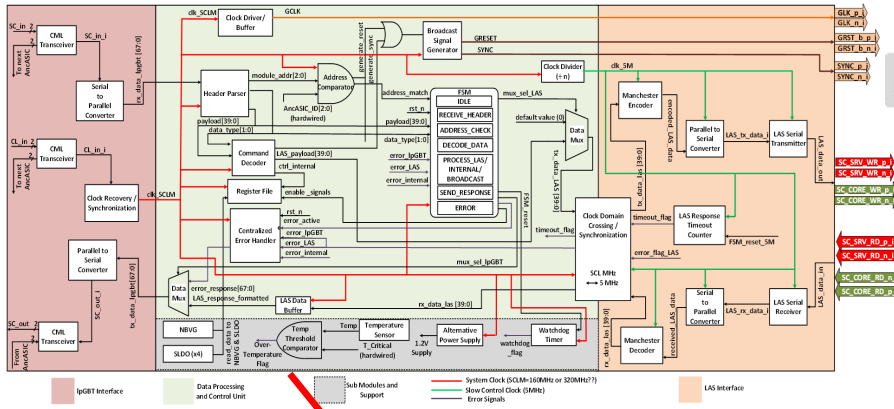
- Plans
- Why AncASIC?

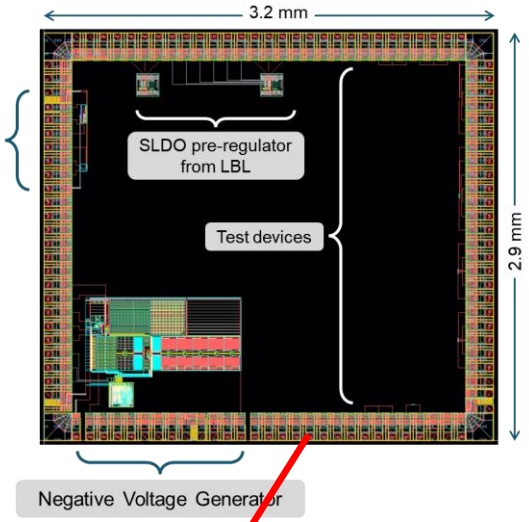
MOSAIX and EIC-LAS Update

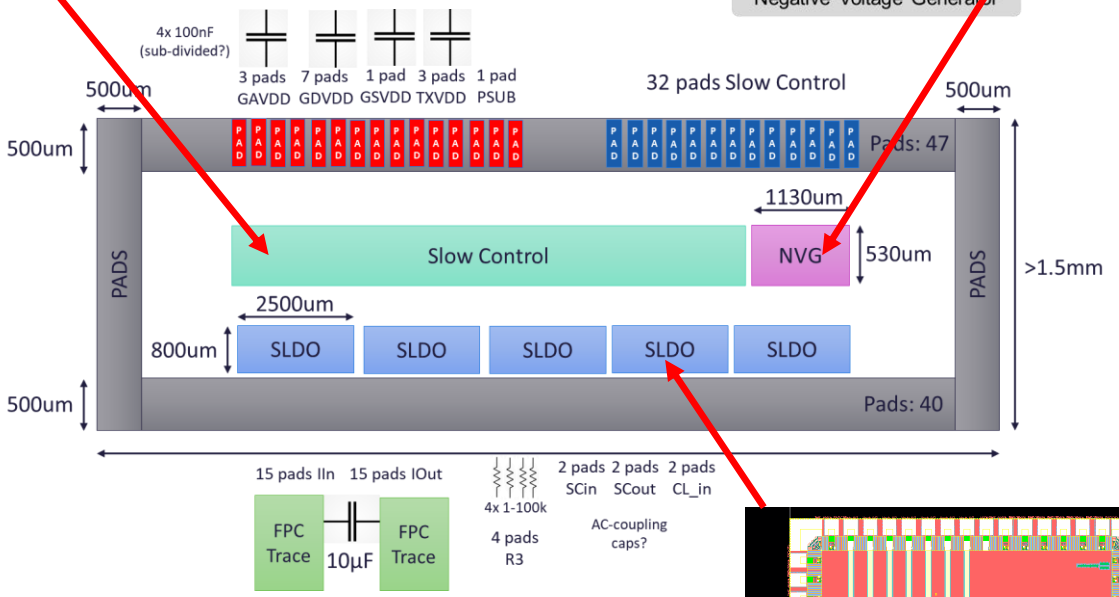
- ER1: MOSS
- ER2: MOSAIX

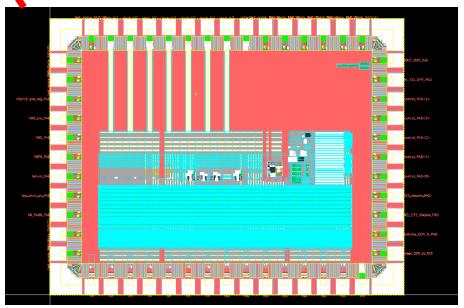
AncASIC Update

- Technology
- Chips Submitted
- Future Plans









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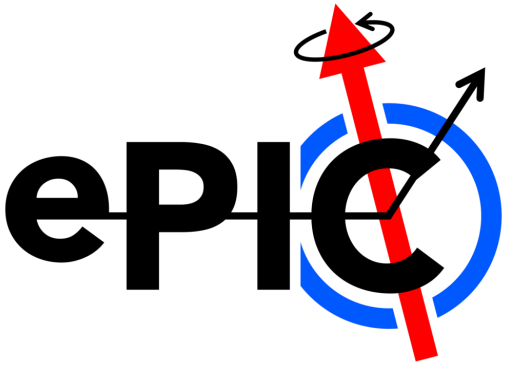
Based on slides from the 10th DAC Meeting - https://indico.bnl.gov/event/26584/



SVT Silicon Scheme

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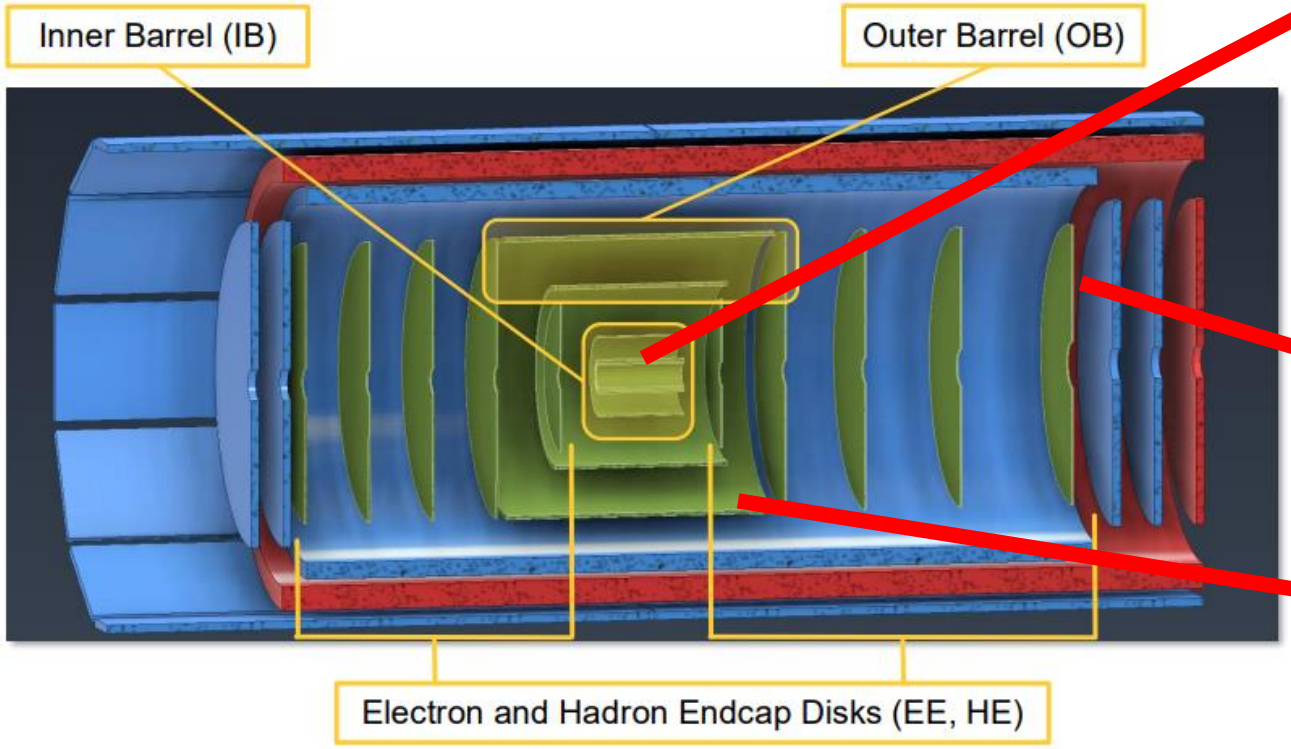
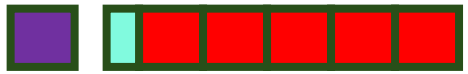
Introduction
SVT Silicon Scheme



Inner Barrel

- Thinned silicon bent around beampipe
- Use wafer-scale MOSAIX from ITS3

Outer Barrel and Discs



- Smaller Version of MOSAIX with minimum necessary changes (EIC-LAS)
- Supporting AncASIC

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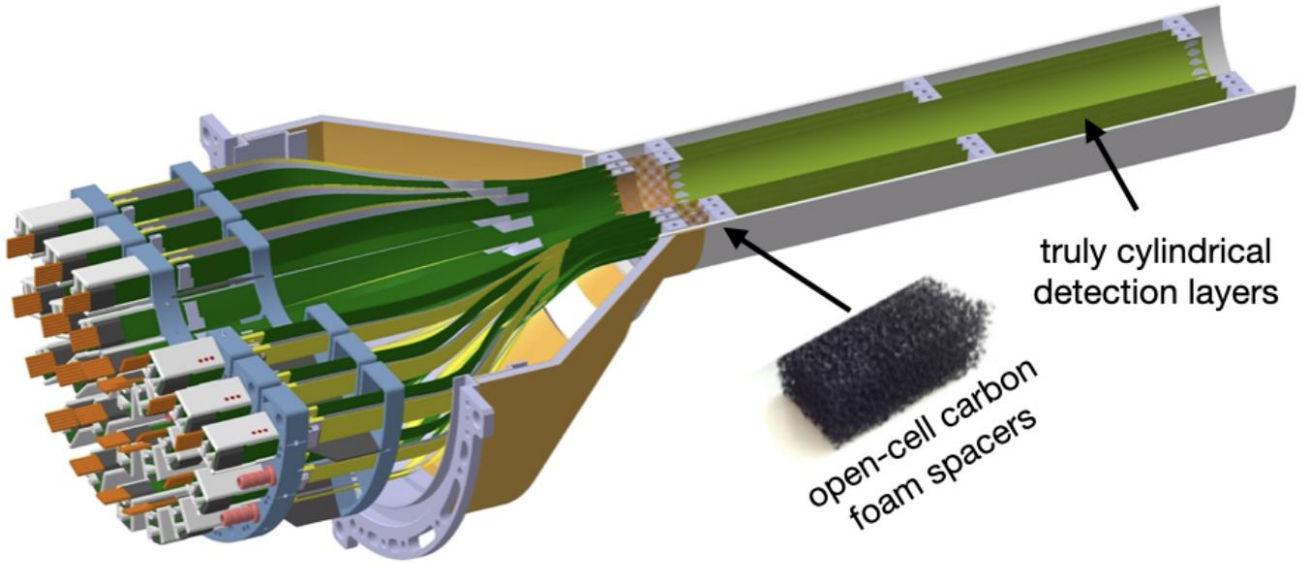
Ancillary ASIC

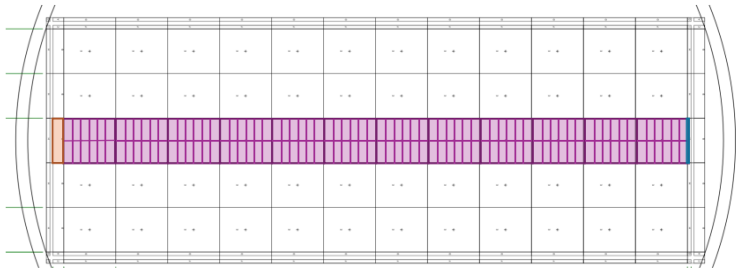
Why AncASIC?

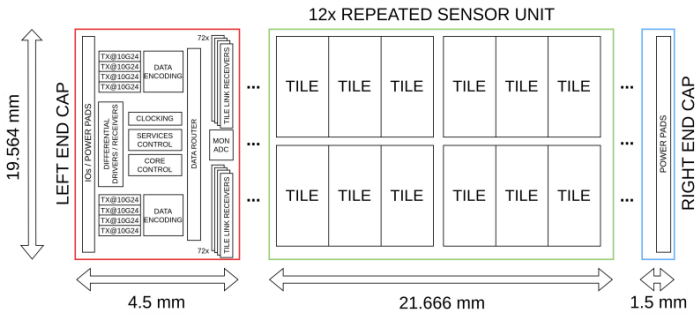
- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control
  - Point-to-point powering
  - Precise negative back bias
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency
- For these reasons, develop supporting ASIC instead



https://ep-news.web.cern.ch/content/alice-its3-clears-major-milestone

MOSAIX





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https://indico.cern.ch/event/1381495/contributions/5988486/attachments/2869319/5164357/TWEPP2024.PVL.v11.pdf

Ancillary ASIC

Why AncASIC?

- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control → Serialised Slow Control interface from EIC-LAS to lpGBT
  - Point-to-point powering → SLDO for serial powering
  - Precise negative sensor bias → Local Negative Voltage Generator
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency

→ Develop independent supporting chip
  - Development decoupled from MOSAIX availability
  - No modification of MOSAIX needed
  - 110nm XFAB process
    - 4 MPW runs a year
    - Cost effective
- For these reasons, develop supporting ASIC instead

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Ancillary ASIC

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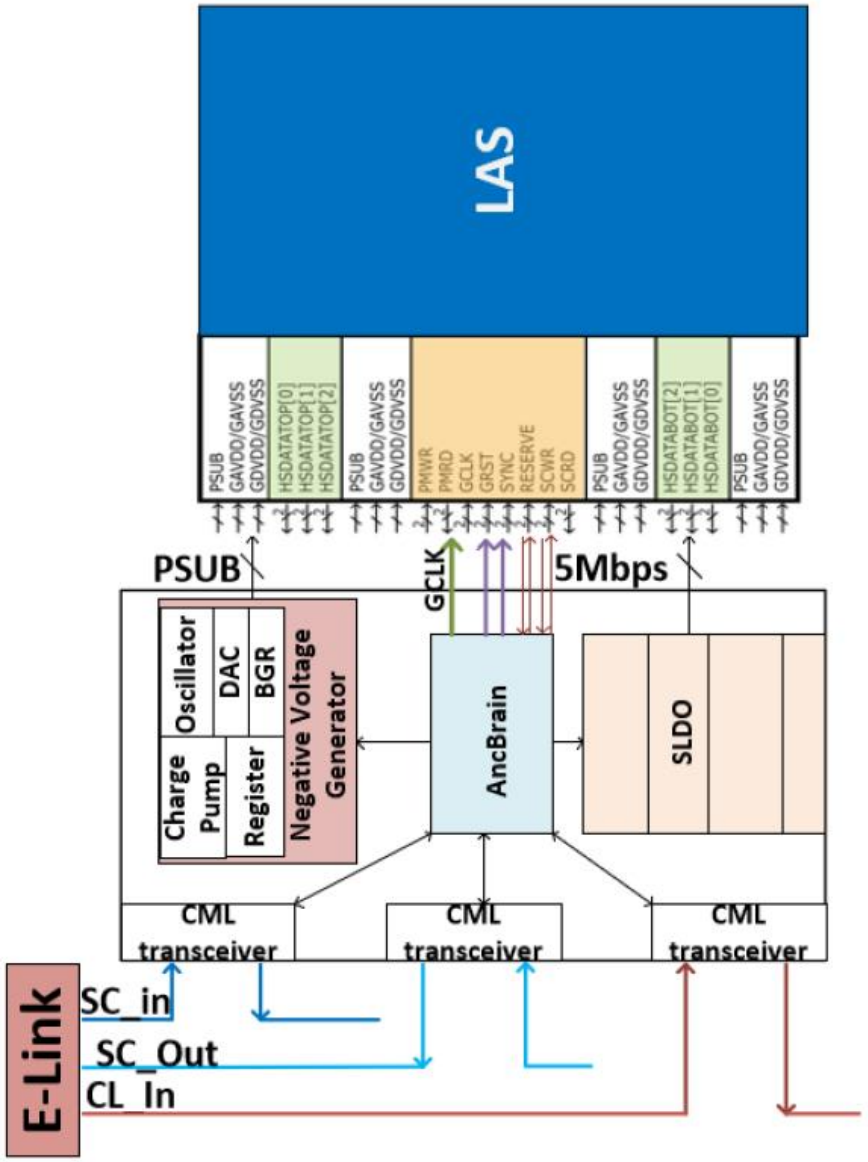

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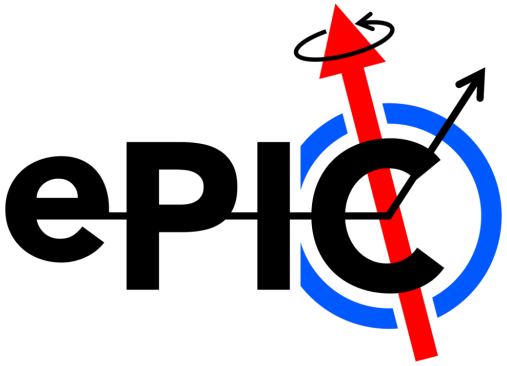

MOSAIX and EIC-LAS Update

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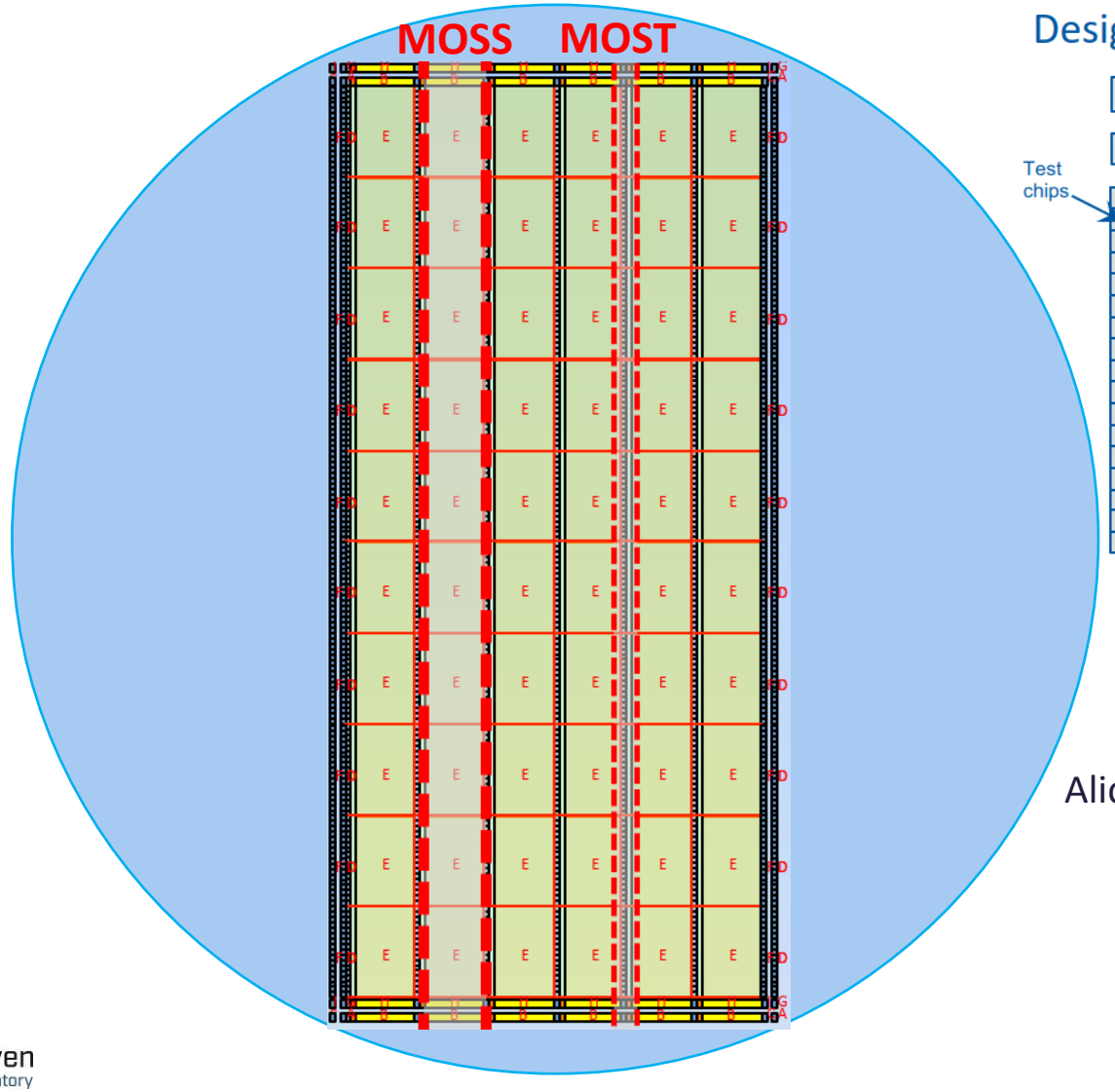
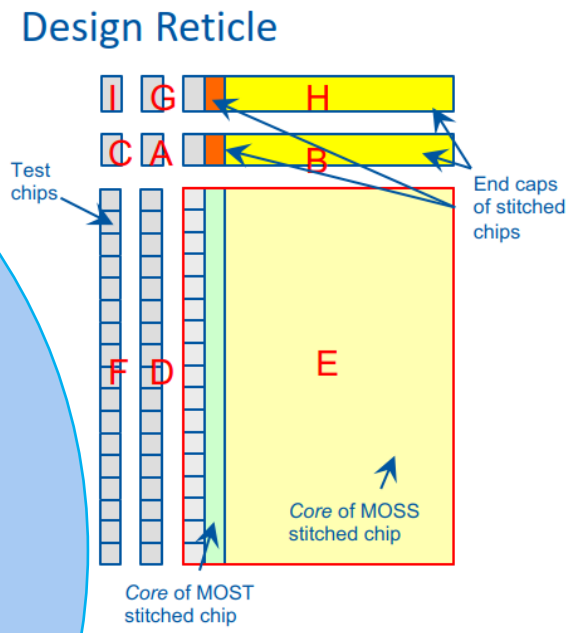
ER1: MOSS and babyMOSS

- Main objective: Learn and prove stitching
- Two large stitched sensor chips (MOSS, MOST)
- Different approaches for resilience to manufacturing faults
- Small test chips (Pixel Prototypes)





Alice/ITS3

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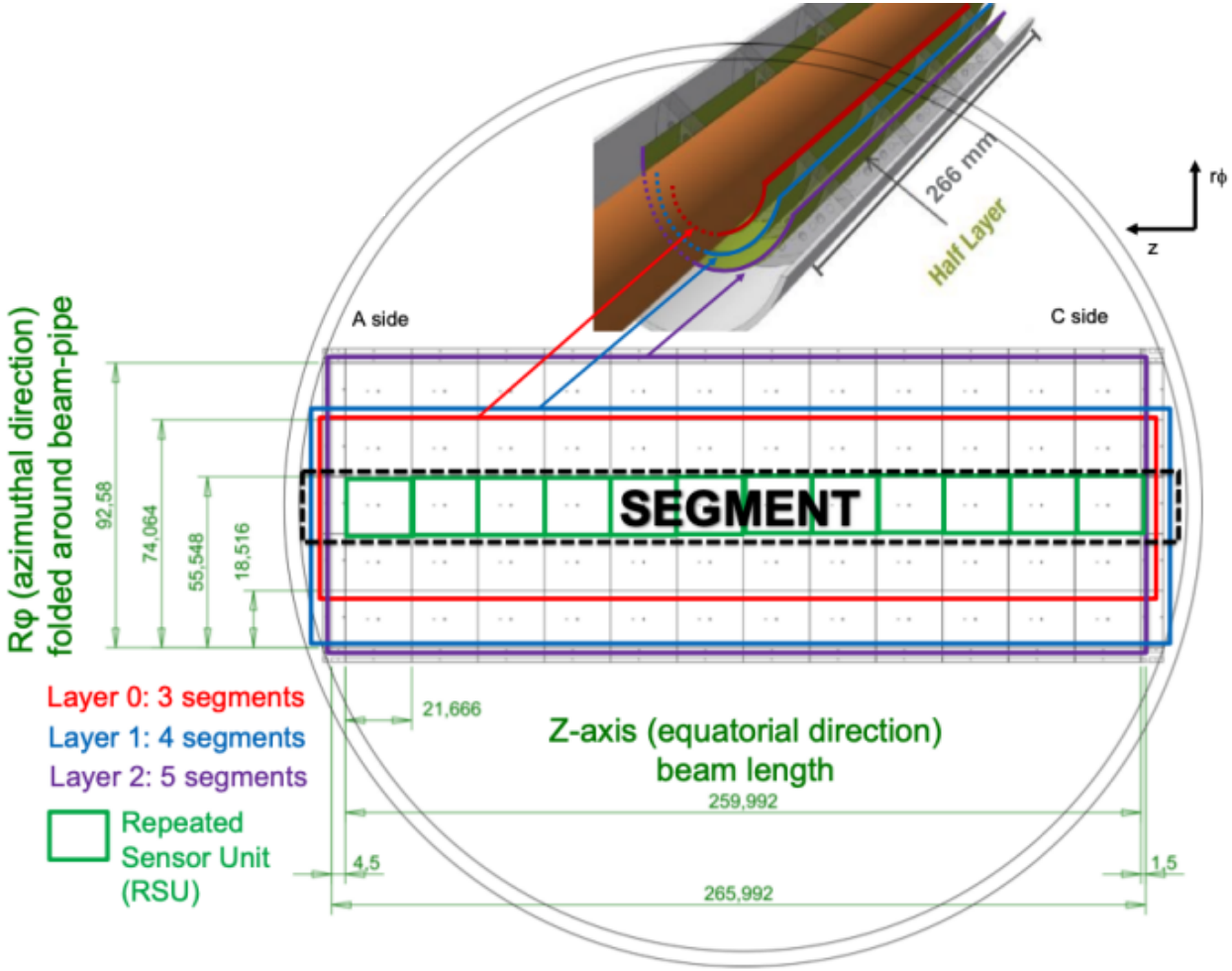
ER2: MOSAIX

- MOSAIX is a full feature prototype of the sensor for ALICE ITS3
- Wafer scale sensor design using the stitching technique
- Process: TPSCo 65 nm CMOS Imaging Sensors(customized)

- MOSAIX design leading to production sensor (ER3)



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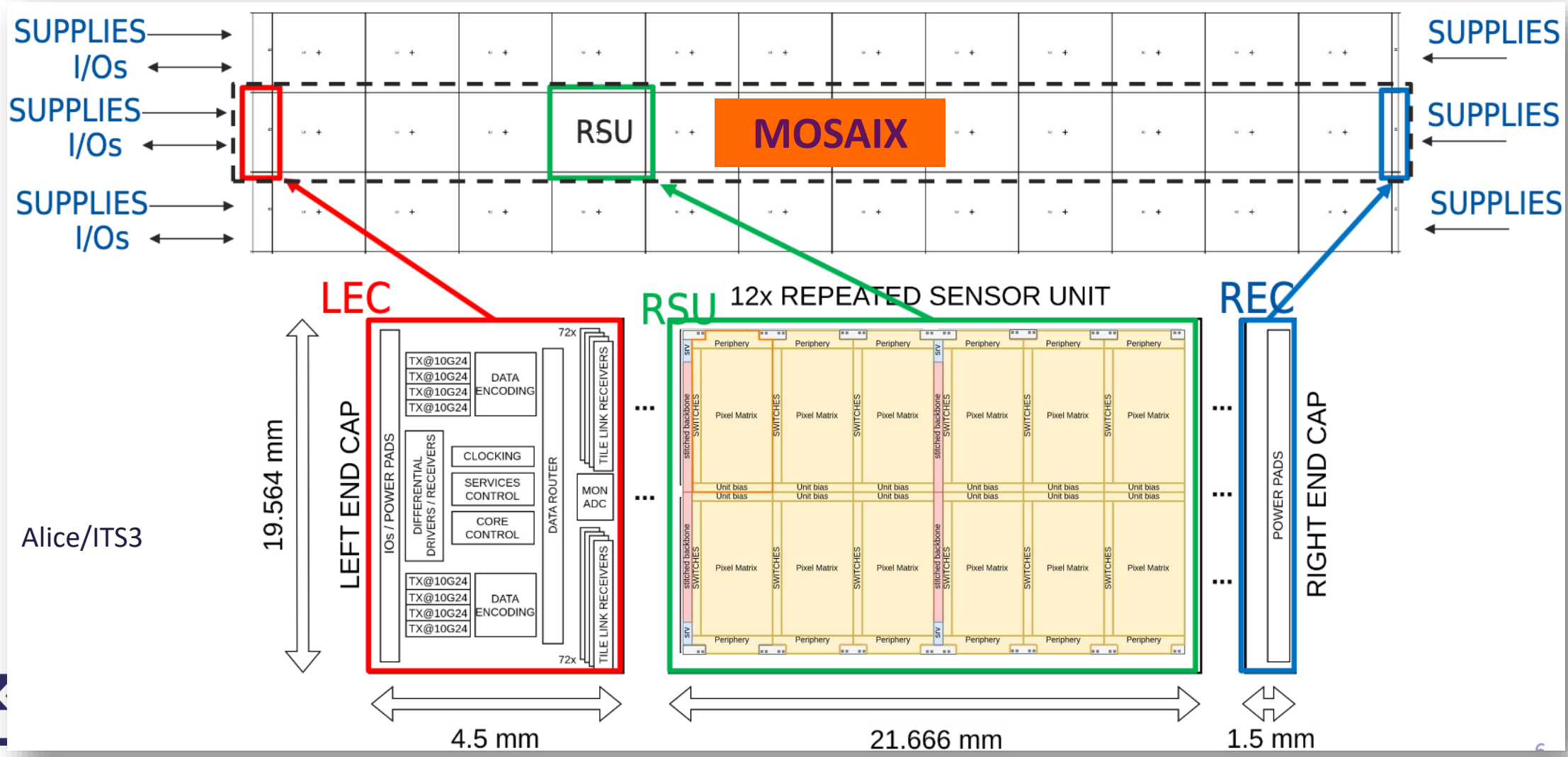
ER2: MOSAIX



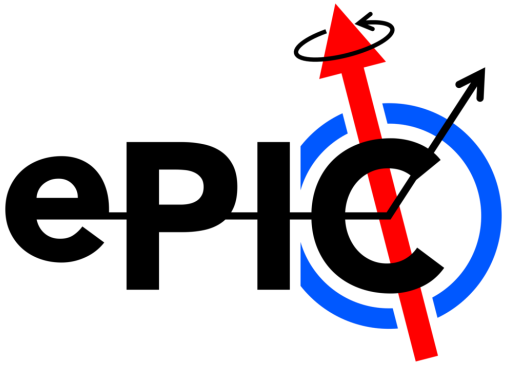
Alice/ITS3

MOSAIX: Status and Outlook

RSU, LEC, MOSAIX

- All components and top level now designed and implemented.
- DOING: refinements of Quality of Results (QoR), powering signoff and polishing of physical integrity.
- Verification

- Functional verification on RTL models completed.
- DONE: complete signoff reviews of simulations of SBB and MOSAIX powering transients.
- DOING: verification with GLN models, SEU simulations, power aware simulations.
- Physical Rules on full wafer gds in very good state



MOSAIX to EIC-LAS

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MOSAIX to EIC-LAS

Inner Barrel

MOSAIX segment

- 12 RSUs
- 8 data links
- 7 slow control links
- Direct powering

Improve yield and coverage →

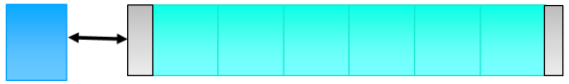
Lower material budget →

Lower material budget, fit integration requirements →

Lower material budget, fit integration requirements →

Outer Barrel, E/H Endcaps

EIC-LAS and ancillary chip



- **5 or 6 RSUs**
- **Single data link**

EIC-LAS

- Multiplex slow control
- Serial powering

Ancillary ASIC

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MOSAIX: Power

Only goes one way…

- Some (all?) of the latest MOSAIX power numbers for the LEC exceed our estimates
- Our previous power number for the LEC was 411mW typ and 570mW in max

Summary: MOSAIX Power

ITS3 TDR Table 3.10

	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left end cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Impact on EIC-LAS

The foreseen modifications on LEC will reduce this power / potential issue

No changes foreseen for the RSU. However, MOSAIX-RSU power is expected to perform as planned.

- Final numbers can only be provided after MOSAIX has been tested, which is expected in early 2026.

LEC Power post implementation

Scenario	LEC Power [mW] Typ	LEC Power [mW] Max	LEC Power Density [mW/cm^2] Typ	LEC Power Density [mW/cm^2] Max
3 x 10 Gbit/s	697	904	792	1027
6 x 5 Gbit/s	1043	1358	1185	1543

LEC Area 0.88 [cm^2]

RSU Power post implementation

	Power [mW] Typ	Power [mW] Max	Power density [mW/cm2] Typ	Power density [mW/cm2] Max
Matrix (12)	45.36	89.71	11.5	22.8
Biasing Unit (12)	4.32	4.32	168.0	168.0
Periphery (12)	74.88	84.96	434.4	492.9
SBB Unit (4)	14.40	14.40	1200.0	1200.0
RSU Total	**138.96**	193.39	**32.8**	**45.6**

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MOSAIX Power

So what does that mean?

- Our previous power number (based on the MOSAIX Engineering Review) for the LEC was 411mW typ and 570mW in max

Condition	Typ Power (mW)	Max Power (mW)
Our previous estimate	411	570
Latest MOSAIX (3x 10G)	697	904
Latest MOSAIX (6x 5G)	1043	1358
Latest MOSAIX (1x 5G)	391	493

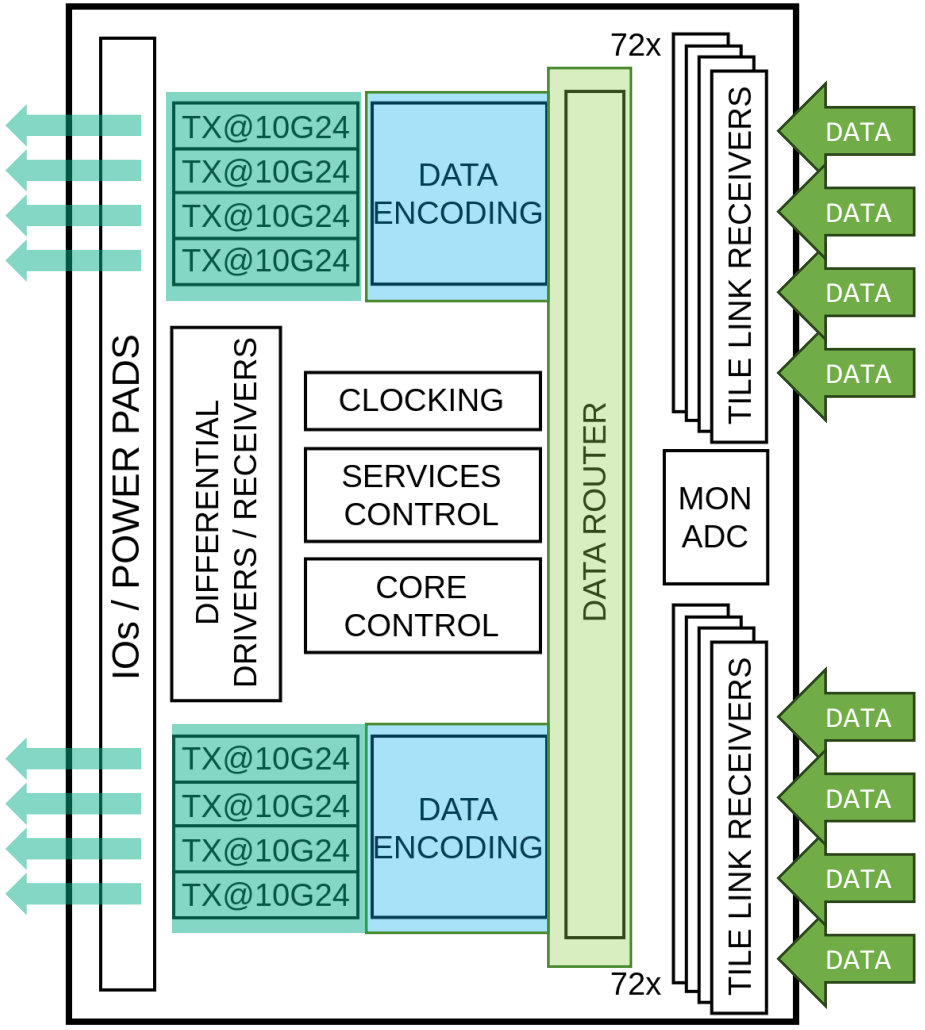
- So if we can reduce to 1 5G link, we will be around our original estimate.
- But this is just my first attempt to integrate these values
  - Need to re-simulate
  - Does the expected data imply 1 link is OK? Who is simulating this?

MOSAIX to EIC-LAS : LEC Modifications

Reduce LEC to one channel

- Bypass Serializer LDOs
- Study on the performance before and after removing LDOs.
- Dedicated decap cells, star routing (supply), and functional adjustments (no LDO controls).

- Data Encoding and Router (serialization of the data to a single channel)
- Challenge to adapt/change
- Slow control needs to be modified



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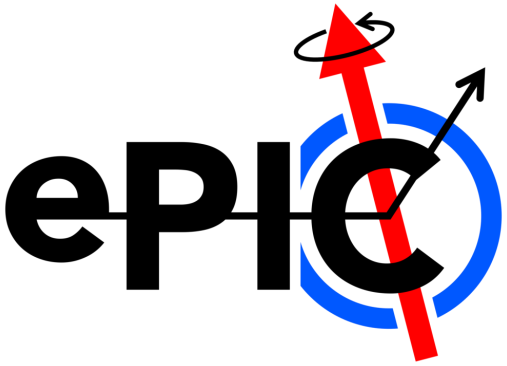

AncASIC Update

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Technology Selection

XFAB XT011

- 110nm BCD-on-SOI Technology
  - SOI – permits floating grounds for negative voltage generation
  - Thick copper top layer – very low resistance for power dissipation
  - High gate density – suitable for AncBrain
  - All design sites have experience with XFAB
  - Radiation hardness untested
    - ePIC radiation requirement low [1]
    - Derived from a previously tested technology [2]
    - Test structures in fabrication

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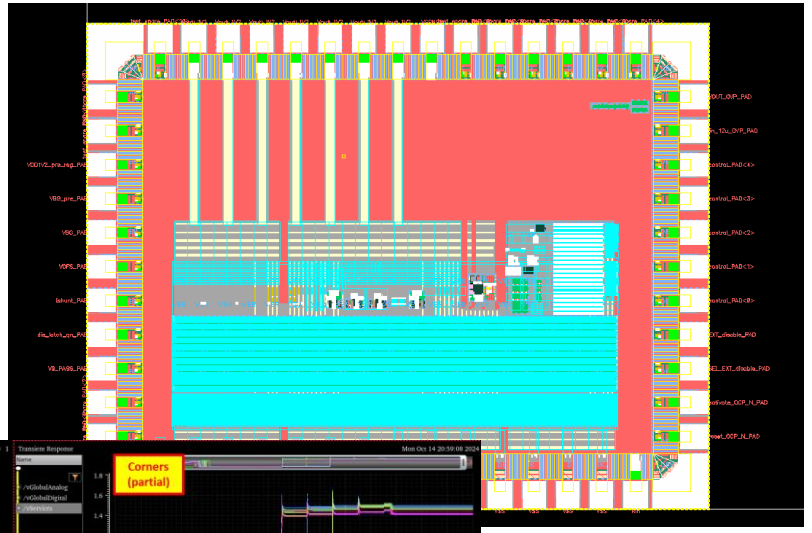
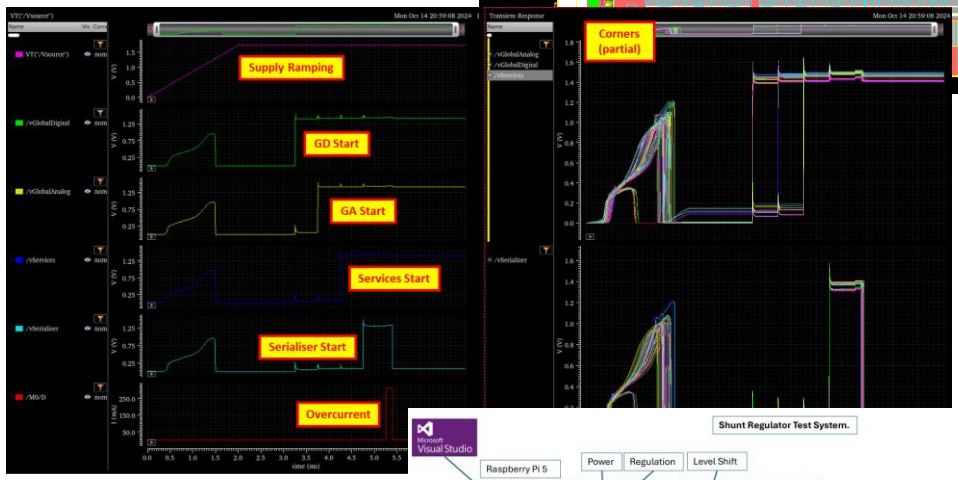
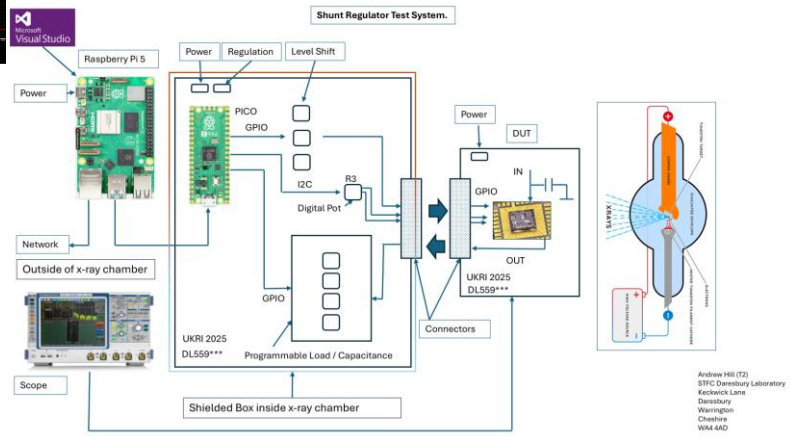
Shunt LDO

SLDO

- Serial powering required for services reduction
- Reviewed with external participants
- SLDO test structure (including pre-regulator) submitted March 2025 (UK funded, submitted via Europractice)
- Expected back September 2025
- Test system in preparation







Prototype currently in fabrication!

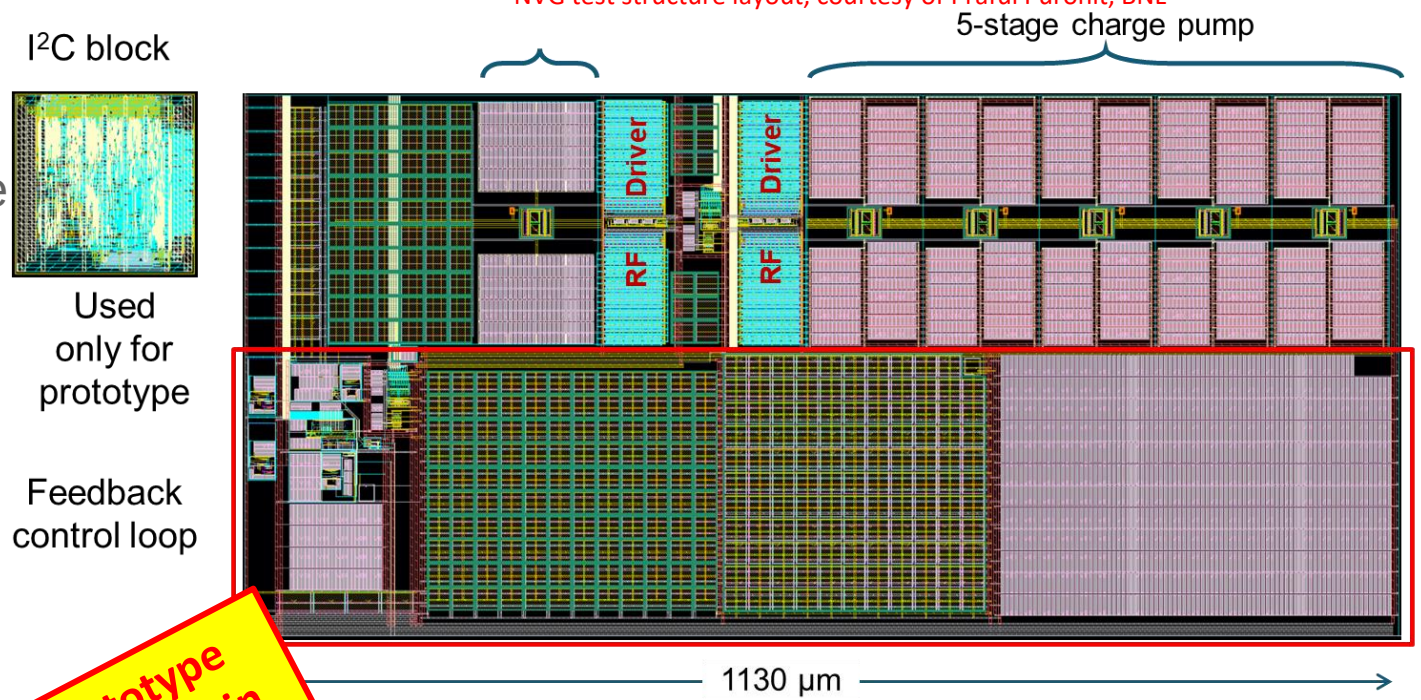
SLDO Test System Plan, courtesy of Andrew Hill, UKRI-STFC Daresbury Laboratory

Negative Voltage Generator

NVG

- Local generation of sensor bias voltage needed due to combination of serial powering and low bias level (~1V)
- Reviewed with external participants
- Test structure submitted March 2025
- Also included transistor test structures and other blocks
- Expected back September 2025
- Test system in preparation

NVG test structure layout, courtesy of Praful Purohit, BNL

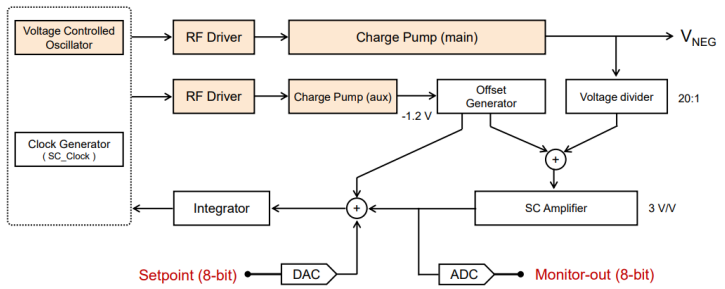


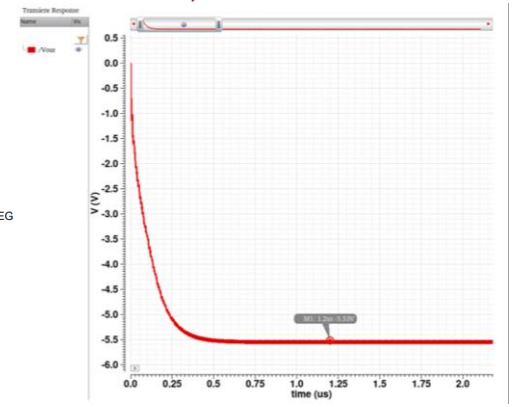
Prototype currently in fabrication!

* Size (not including the I²C block)

ive Voltage Generator (NVG)

(With feedback control)





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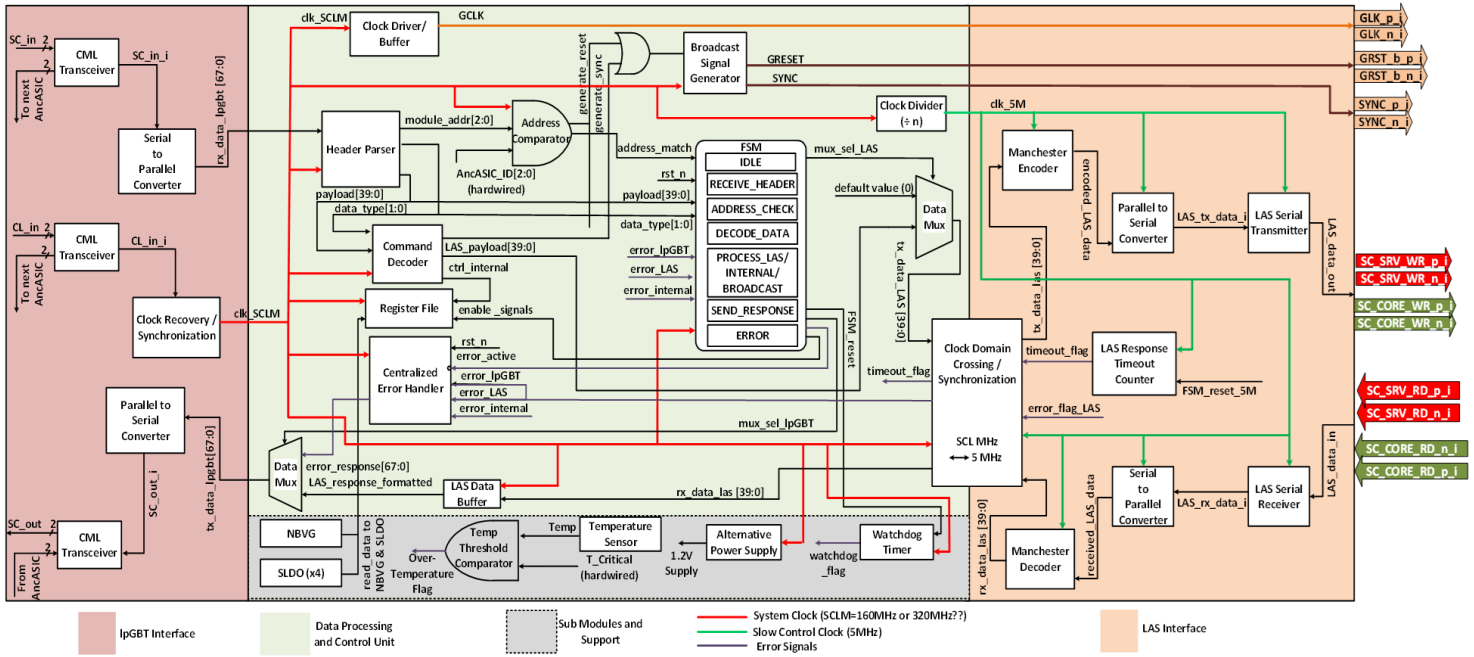
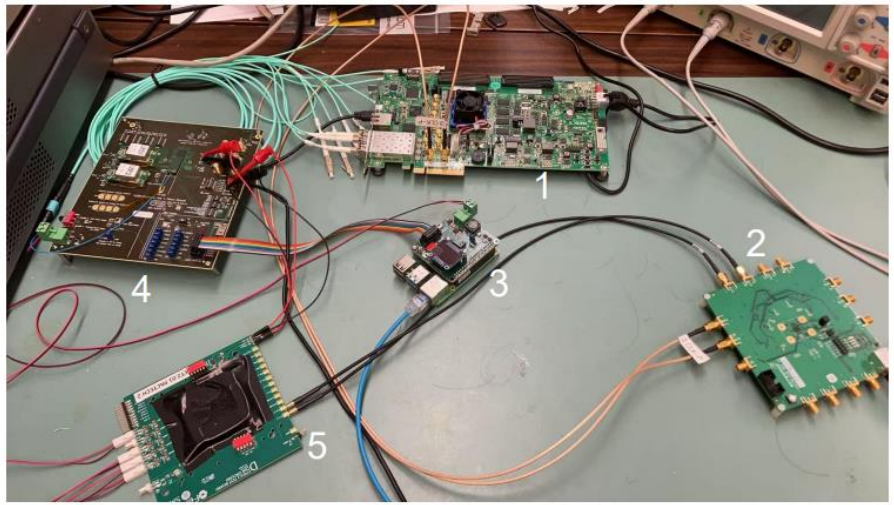
AncBrain

AncBrain

- Required for services reduction and control of NVG and SLDO
- Core modules complete, working on tests with MOSAIX emulator
- Plan to submit as part of first AncASIC
- Hardware emulator in preparation between LBNL, ORNL and BNL

AncBrain Plan, courtesy of Arif Iqbal, BNL

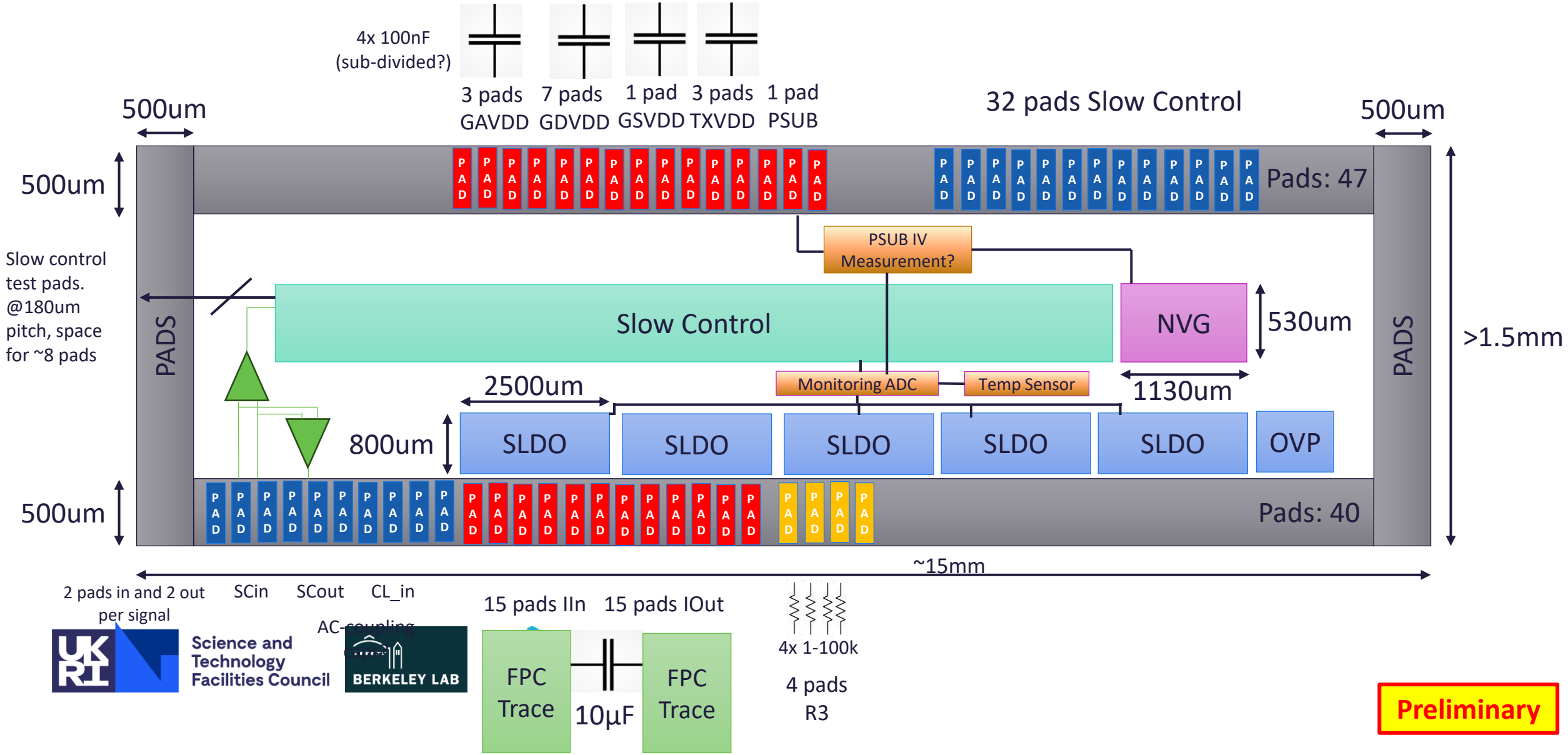




1. KCU105
2. Clock generator
3. PiGBT (status monitor only)
4. VLDB+
5. ETROC2 test board

Hardware mockup, courtesy of Zhengwei Xue, LBNL

Current AncASIC Plan



Progress, Next Steps and Challenges

Progress and Next Steps

- AncASIC requires three main blocks. Prototypes for 2 have already been submitted:

• MPW1 (NVG)	March 2025
• MPW2 (SLDO)	March 2025

Work has started on the next components, and planning for further phases:

• Complete MPW1/2 Test Systems	September 2025 (to match out-of-fab date)
• Complete MPW1/2 Testing	March 2026
• Complete AncBrain Design and Validation	Q3 CY2025
• Submit AncASIC V1	September/November 2025
• Complete AncASIC V1 Test System	March/June 2026
• Complete AncASIC V1 Testing	Aug/December 2026
• Complete AncASIC V2 Design Modifications	Q1 CY2027
• AncASIC V2 Production	Q1 CY2027

Complete
In Progress
Not started

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Conclusion


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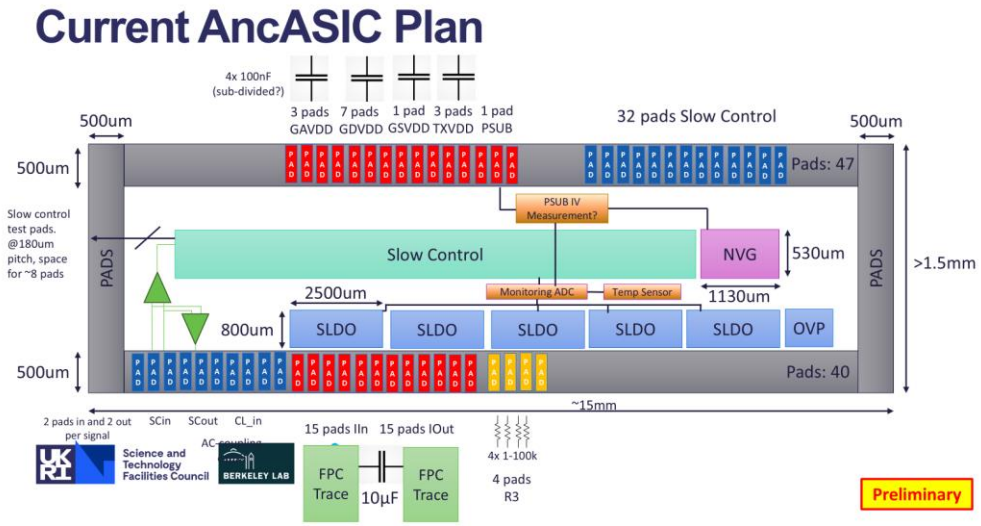
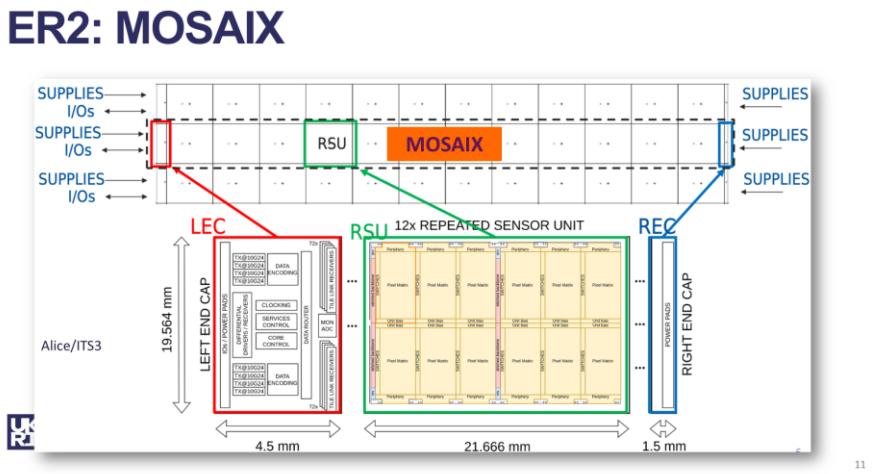
Conclusion

AncASIC Status

- **AncASIC**
  - Design progressing well
  - First test structures in fabrication
  - AncBrain design under way
  - Next steps are testing, AncBrain completion and full integration
  - DSA to be agreed (although some movement)

- **MOSAIX/EIC-LAS**
  - Submission very soon
  - CERN/DOE agreement still needed





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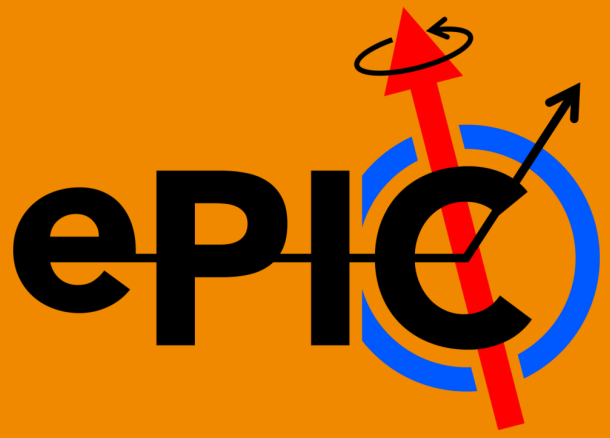

Questions?

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References

[1] *Radiation and Rate Environment*, Gonella L., ePIC Collaboration Meeting, Argonne, Jan 9 2024, https://indico.bnl.gov/event/20473/contributions/84983/

[2] S. Fernandez-Perez, M. Backhaus, H. Pernegger, T. Hemperek, T. Kishishita, H. Krüger, N. Wermes, *Radiation hardness of a 180nm SOI monolithic active pixel sensor*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 796, 2015, Pages 13-18, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2015.02.066.