AncAsic testing & other test activities

20250626

M.Borri et al

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Outline

- Latest progress from EPIC-SVT-WP2 inc. MPW2-sLDO
- Update on UK involvement on ITS3 prototype tests
- Progress on X-ray irradiations of ER1 RAL prototypes

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AncAsic prototypes

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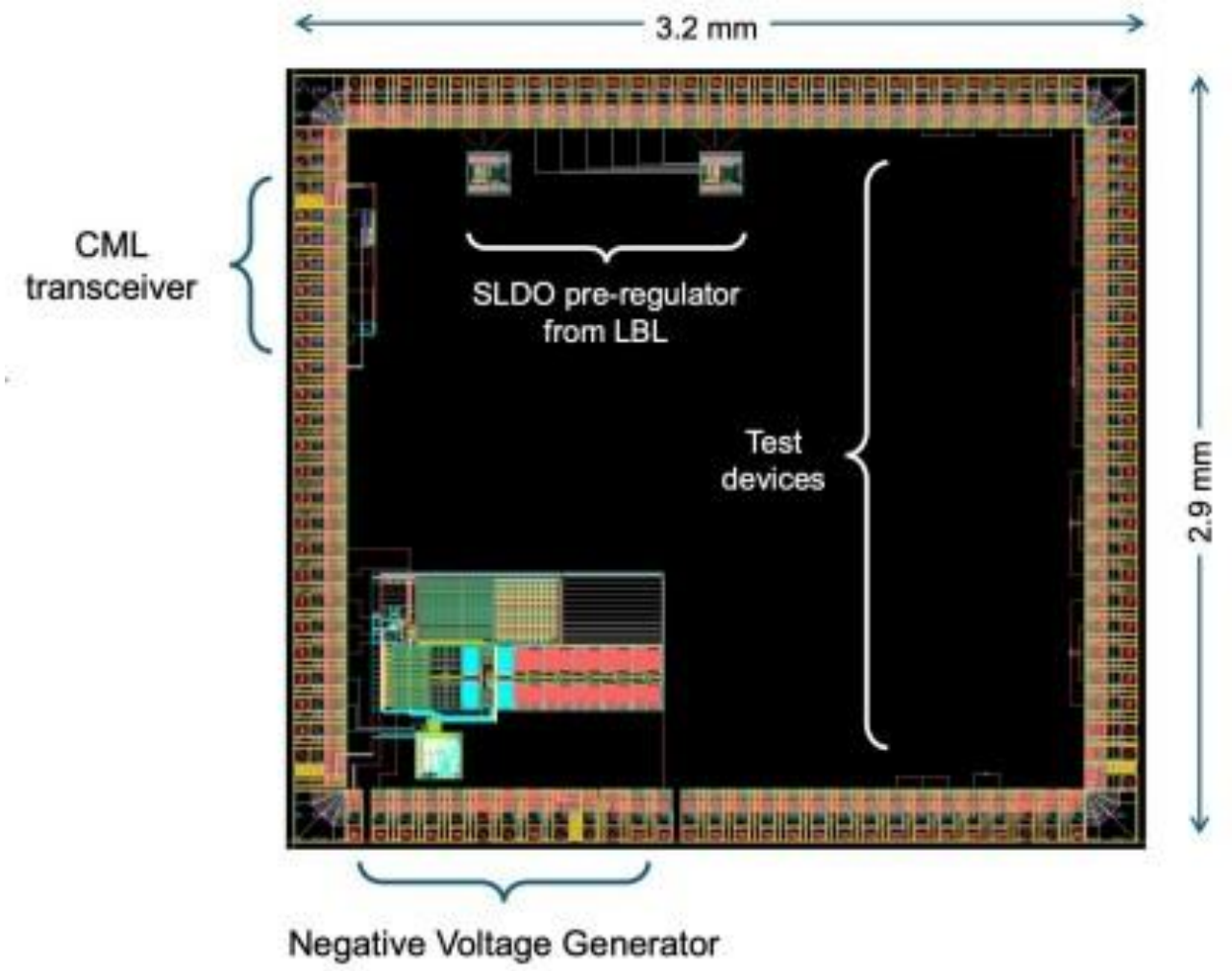
MPW1 – AncASICXT011 P1

- Designed by BNL and LBNL
- It includes:
  - SLDO pre-regulator;
  - NVG;
  - CML transceiver;
  - Transistor Test structures;
- ~10 different IC blocks on the same Si die



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MPW1 – AncASICXT011 P1

AncASIC testing task list

MPW1 AncASICXT011_P1

	Task	Start date	End date	Quantity	Testing details, conditions	Comments	Equipment	Responsible group/person (interested person/
	MPW1 tapeout/submission (WP1 task)		09/25					**WP1**
	MPW1 testing		03/26 ?					
1	**Test specs definition**		09/25					**WP1, WP2**
2	**Carrier board PCB design + manufactu**	06/25	09/25	~45				**LBL** - Zhengwei Xue **(BNL** schematics by er
3	**Chip+PCB assembly, wirebonding**	10/25	10/25	~45				**LBL** - - production might need funding support
4	**Test system HW (control)**		10/25	?				**?** - not sure if needed (LANL I2C control for NV
5	**SLDO Pre-Regulator characterization**	10/25	03/26 ?				Standard lab equipment(power supply, IV mete	**LBL** - (UK? - maybe later)
	Output Ripple/Noise				Load Capacitance - 1pF, **10pF**, 100pf, 1	Number in red is the expected value.Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)				ESR - **3.5k**			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
6	**NVG characterization**	10/25	03/26 ?				Standard lab equipment(power supply, IV m	**LBL** - **(CTU)(LANL I2C)** - Joellen Renc
	Output Ripple/Noise				Load Capacitance - RANGE?			
	Transient Response (overshoot and settling time)				Frequency - RANGE?			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Standard Supply Variation	Plus and Minus 20%		
					Ramp Rate - RANGE?			
	Test in combination with APTS/DPTS/ER1					Use NVG to generate back bias for alreadyexisting APTS and DPTS chips		
7	**CML transciever**	10/25	03/26 ?					**LBL** -
8	**Transistor Test Structures characterizati**	10/25	03/26 ?	?			Standard lab equipment(power supply, IV, L	**BNL** -**(LBL)(CTU)**
	Ids vs Vgs						TTS characterization IV setup	
	Vt extraction							
					Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
					Standard Radiation Range	0 - 1MRad in 100kRad steps		
					Standard Supply Variation	Plus and Minus 20%		
9	**Irradiation**	10/25	03/26 ?	?				**BNL** (Cobalt60, X-ray ?) -**(LBL)** (X-ray) - **(CT**
					X-raysCobalt60	Chips powered during the irradiation, temperature monitoring		
					Standard Radiation Range	0 - 1MRad in 100kRad steps		
10	**SEE/SEU Tests in a proton beam**	10/25	03/26 ?	?			Proton beam with XY table	**BNLLBLCTU**

Note: ~10 IC blocks per DUT; total DUTs: 45 units; equates to 4-5 DUTs per block;
Not many DUTs to test…
No UK involvement to date.

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MPW2 sLDO

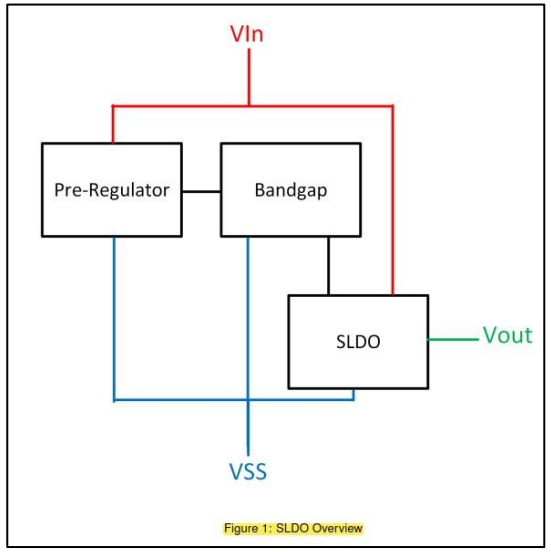
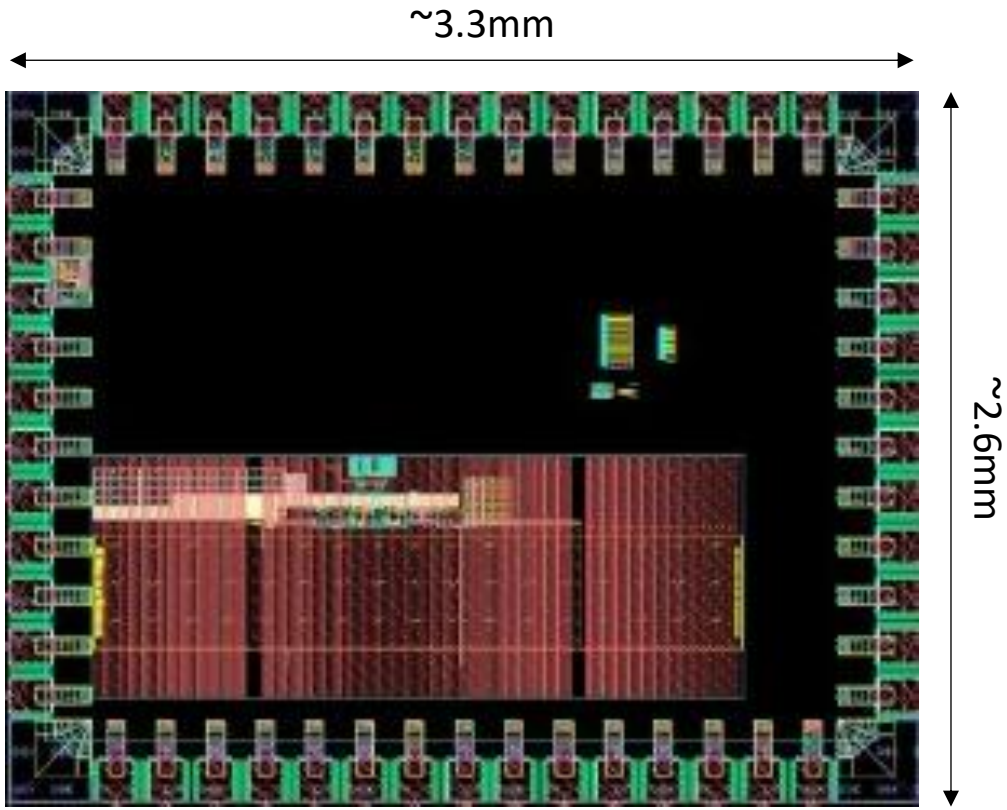


Figure 1: SLDO Overview

- Designed by UK institutes and LBNL
- It includes SLDO with 3 main block:
  - **SLDO**: The Shunt LDO circuit itself.
  - **Bandgap**: A bandgap used to generate biases for the SLDO circuit
  - **Pre-regulator**: An LDO and bandgap sitting in front of the other blocks which power them and help with their start-up



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MPW2 sLDO

AncASIC testing task list

MPW2 SLDO

	Task	Start da	End dat	Quantity	Testing details, conditions	Comments	Equipment	Responsible group/person (interested person/group)
	MPW2 tapeout/submission (WP1 task)		09/25					WP1
	MPW2 testing		03/26 ?					
1	**Test specs definition**		09/25					**WP1, WP2**
2	**Carrier board PCB design + manufa**	06/25	09/25	~50		PCB and test system design inc. micro-		**Daresbury** - Andrew Hill
3	**Chip+PCB assembly, wirebonding**	10/25	10/25	~50		Wirebonding of DUTs onto carrierboards		**University of Birmingham (UK) -** James Glover, C.S. Tse
4	**Test system HW (control)**	06/25	10/25	5?				**Daresbury** - Andrew Hill
5	**SLDO characterization**	10/25	03/26 ?			Three institutes involved in sLDO testing:Univer	Standard lab equipment(power supply, IV m	**University Of Birmingham -** J.Glover; L.Li; **Brunel Univeristy** - L.Teodorescu; **Daresbury Lab** - M.Borri; **(LBL)** 3 institutes to date
	Output Ripple/Noise				Load Capacitance - 1pF, **10pF**, 100pf,	Number in red is the expected value.Others are for exploring the parameter space		
	Transient Response (overshoot and settling time)				ESR - **3.5k**			
	PSRR and line regulation				Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber	
	Start-up				Standard Radiation Range	0 - 1MRad in 100kRad steps		X-rays at Daresbury; Protons at Birmingham cyclotron (TBC);
					Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s			
6	**Irradiation**	10/25	03/26 ?	?				**Daresbury Lab - X-rays - M.Borri** **Univerisity of Birmingham (UK) - (TBC) Protons (Cyclotron) - J.Glover; L.Li;** **(BNL)** (Cobalt60, X-ray ?) - **(CTU)** (X-ray, Cobalt60) - **(LBL)** (X-ray) - Added by M.Borri More available
					X-raysCobalt60	Chips powered during the irradiation, temperature monitoring		X-rays at STFC Daresbury Lab; Protons at Birmingham cyclotron (TBC);
					Standard Radiation Range	0 - 1MRad in 100kRad steps		

Note: 1 IC block per DUT; Total DUTs: ~50 units;
Generous number of DUTs to test...
Test activity to be distributed mainly to 3 UK institutes.
Possibility to include further institutes, especially for irradiations (LBNL or CTU).

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MPW2 sLDO – more on tests requirements

Mode1:

- **PwrUp**: ramp up the supply voltage to the target level, measure and record the output trace from Vout; (Bham, Brun, DL)
- **PSRR**: measure and record the Power Supply Rejection Ratio (PSRR) at the Vout pin; (Brun, DL)
- **RampRate**: set 100us,1ms,10ms,100ms ramp-rates and measure Vout vs time; (Brun, Bham)
- **DAC Scan**: Scan DAC codes. Record the value of Vout and plot against the code; (Bham, Brun, DL)
- **Irradiations**: monitor Vout, Iout, Ii; (DL X-rays)

3.5.2 Required Tests

This section details the tests that need to be performed on MPW2_SLDO. All the tests below need to be performed in the conditions outlined in Table 2. The only exceptions to this are the DAC Scans and irradiation tests. To simplify these, we will select a single condition. To ease early testing, a first pass of the tests can be carried out at room temperature. Temperature stability can be re-visited later.

Condition	Values
Load Capacitance	10nF, 100nF, 1uf, 10uF
Load Current	40mA, 500mA, 900mA
Temperature Range	-20°, 27°, 60°, 105°

Table 2: Test Conditions

Bham

Mode0:

- **Powerup and overcurrent test**: Apply a excess current to the output and check that it returns to tri-state: Vout, Iout, Iin.(Brun)

@Brunel:
Climate chamber?
Network analyser?

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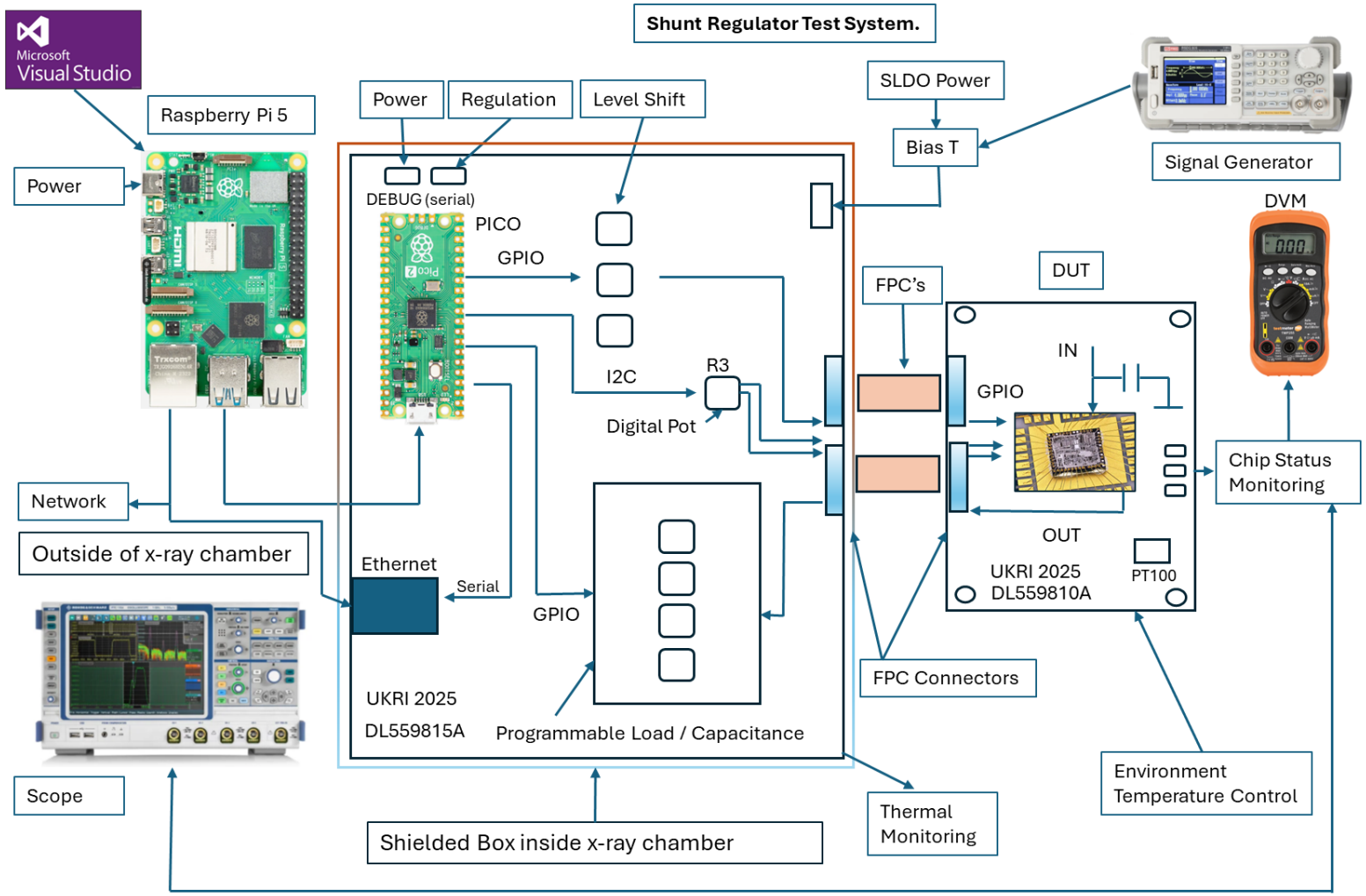
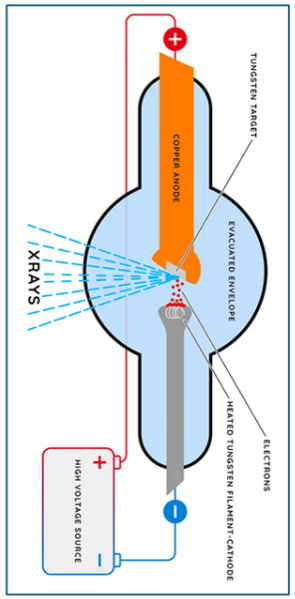
MPW2 sLDO – test system





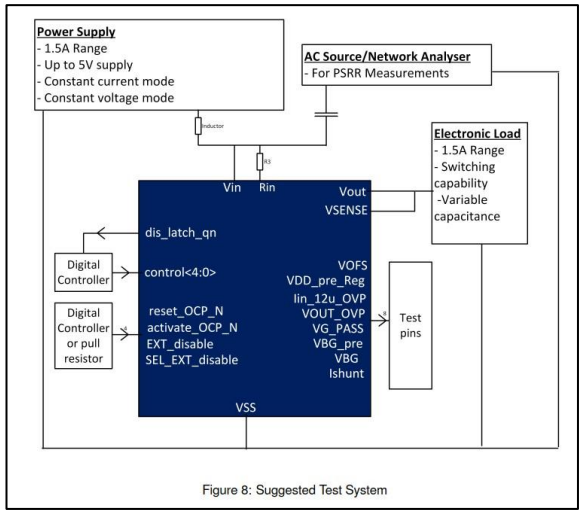


Figure 8: Suggested Test System

DUT carrier PCB:
- Schematics complete;
- Layout complete;
- To be reviewed;

DAQ PCB:
- Schematics complete;
- Layout in advanced stage;

Pico2 programming:
Aug./Sept.

Andrew Hill (T2)
STFC Daresbury Laboratory
Keckwick Lane
Daresbury
Warrington
Cheshire
WA4 4AD

Unclear how to procure PCBs due funds uncertainty

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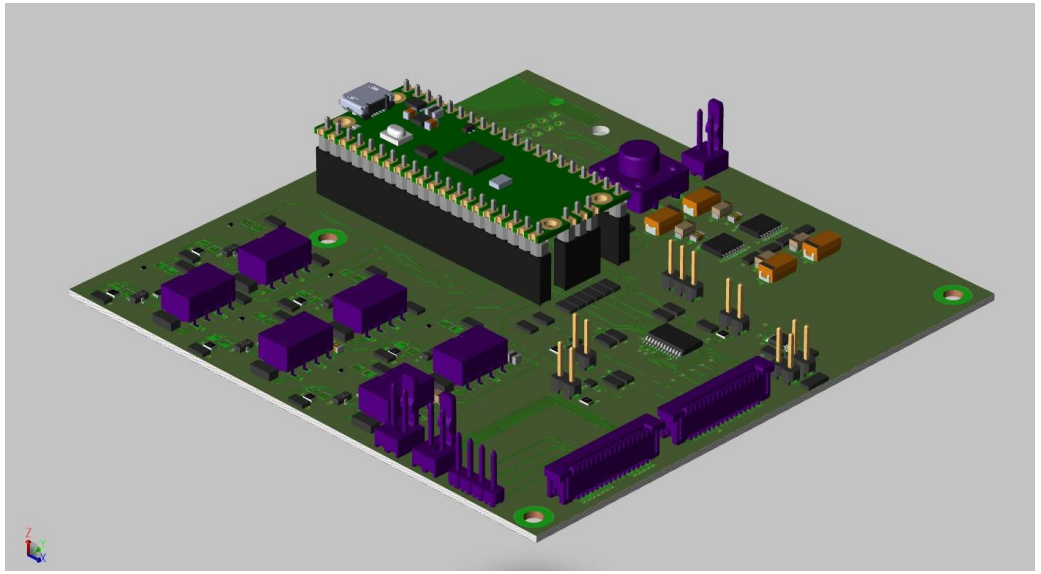
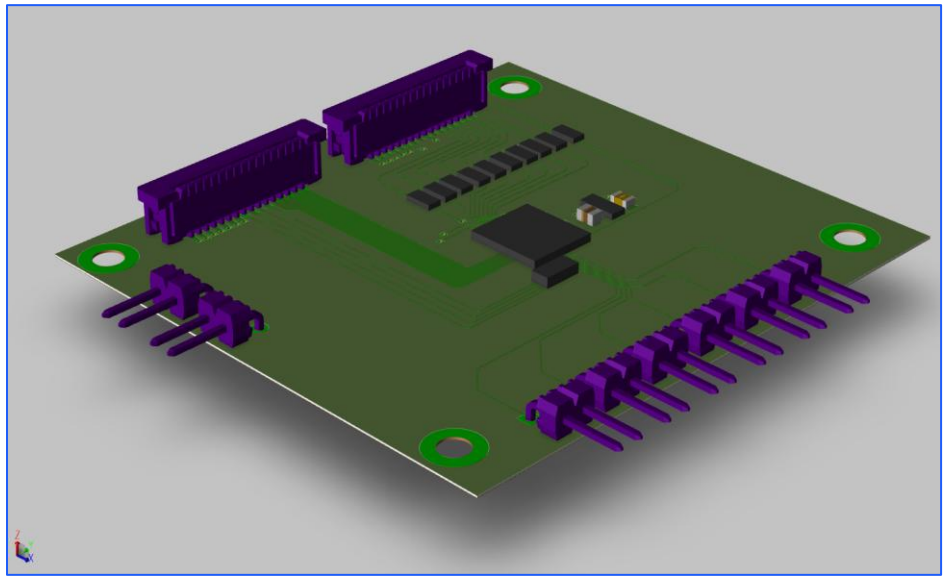
MPW2 sLDO – test system

DAQ PCB



DUT carrier PCB



In progress – to be reviewed

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MPW2 sLDO - Conclusion

- UK-EPIC-SVT is taking part in EPIC-SVT-WP2;
- Datasheet for MPW2 SLDO available inc. test requirements;
- Test plan being developed with EPIC-SVT-WP2;
- Test system design in advanced stage;
- EPIC-SVT-WP2 asks questions about time-scales:
  - Hard to give an answer until UKRI Infrastructure fund is confirmed;
  - Assuming Business As Usual (BAU);

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ITS3 prototypes

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UK involvement on ITS3 prototype tests

- Three institutes involved to date:
  - University of Birmingham;
  - University of Liverpool;
  - Daresbury Laboratory;

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Sensor testing @ Birmingham

- Previously: strong contribution to APTS tests.

- Minimal involvement on ER1 due to not being ITS3 member.

- Now revamping effort under ITS3 umbrella:
  - Help to build the power ramping and impedence measurement system in Liverpool and get basic training in babyMOSS test.
  - **Working on the compliance letter with ITS3 group and preparing the test setup for babyMOSS.**
  - **Joining the test beam of babyMOSS at CERN PS. Analysis of April data in progress.**
  - Participated in the **ITS3 in person meeting in Chamonix for ER2 testing plan**, Expressed the desire of UOB for more in depth cooperation in ER2 stage.

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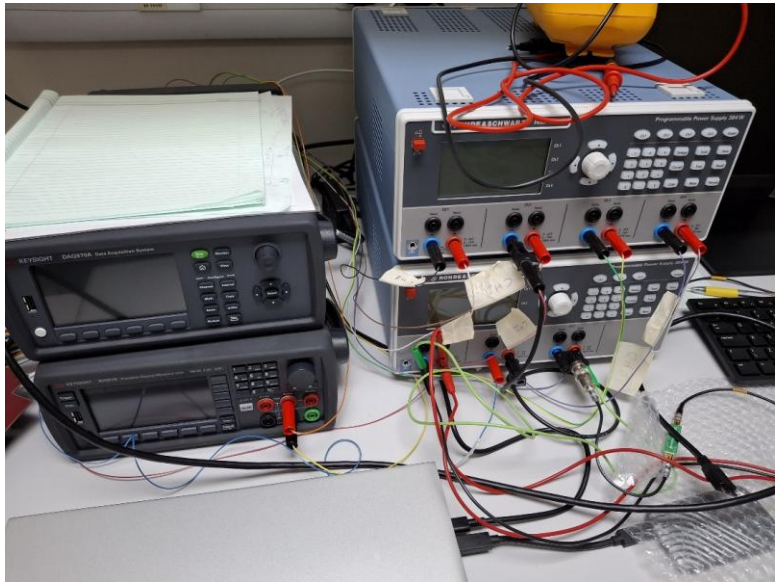
Sensor testing @ Liverpool

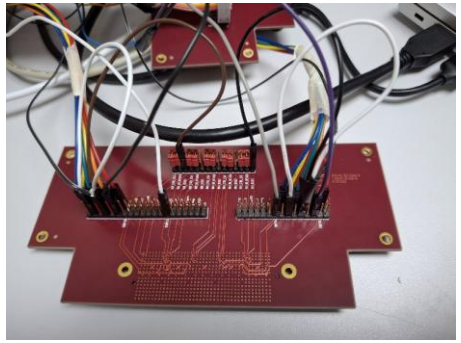


ER1

- Test system based on MLR1 DAQ and raiser board in operation since July 2024
  - babyMOSS tests focusing on fake-hit rate as a function of strobe clock length
- babyMOSS impedance and power ramp test system full functional since March 2025
  - Approximately 40 newly assembled babyMOSS prototypes (from BNL and Bonn) to be tested in the coming months
- Hands-on babyMOSS session for Long (Birmingham) and Lochana (Brunel)

ER2

- Testing plans for ER2 MOSAIX agreed with ITS3 project leaders; details under discussion
  - babyMOSAIX wire-bonding (TBC)
  - babyMOSAIX powering and functional tests
  - X-ray irradiation campaign in collaboration with Daresbury
  - ER2 software development
  - Test beams at CERN
- Procurement of ER2 test system underway



Team Expansion

- Hiring of a postdoc (application deadline: June 24th)
- PhD student based at CERN from October for one year (expected 0.5 FTE ALICE service work on ITS3, TBC)
- Sensor characterisation projects for MPhys/BSc students submitted for September start

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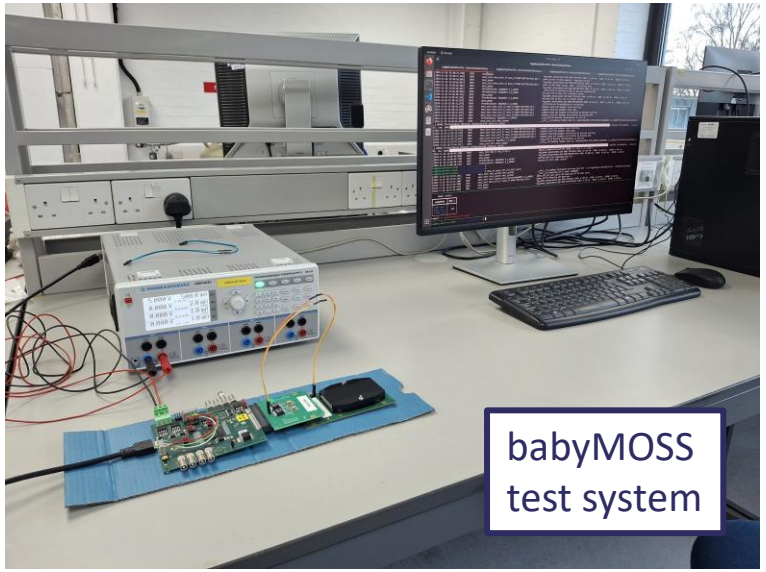
Sensor Testing @ DL

- ER1:
  - **babyMOSS test system** at DL since Nov 2024
  - Measured the fake-hit rate vs strobe length for different chip biases
  - Training session for L.Ranatunge (Brunel)



- ER2:
  - **Requested a MOSAIX test system**
    - Two DAQ boards, one for readout, one for chip emulation
    - Can turn into two separate test systems once MOSAIX chips arrive
  - Testing plans under discussion:
    - babyMOSAIX powering, impedance and functional
    - **TID irradiation at DL** with a Tungsten X-ray tube delivering X-rays up to 60 keV of energy, with Liverpool

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ER1 RAL DUT – X-ray irrads

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Overview of DUT

DUT designed by RAL CMOS group as part of ER1

The DUT contains 3 blocks:

- Dual-Mode Phase Locked Loop (PLL)
- I2C
- Continuous Time Linear Equaliser (CTLE) (Tested HERE)

For CTLE, we measured:

- Supply currents Vs TID;
- Eye amplitude Vs TID;

Irradiations went beyond the EPIC SVT TID requirements (~100's krad);

Irradiations explored the robustness of the 65nm process beyond the EPIC SVT requirements.

Improve and develop in-house irradiation capabilities

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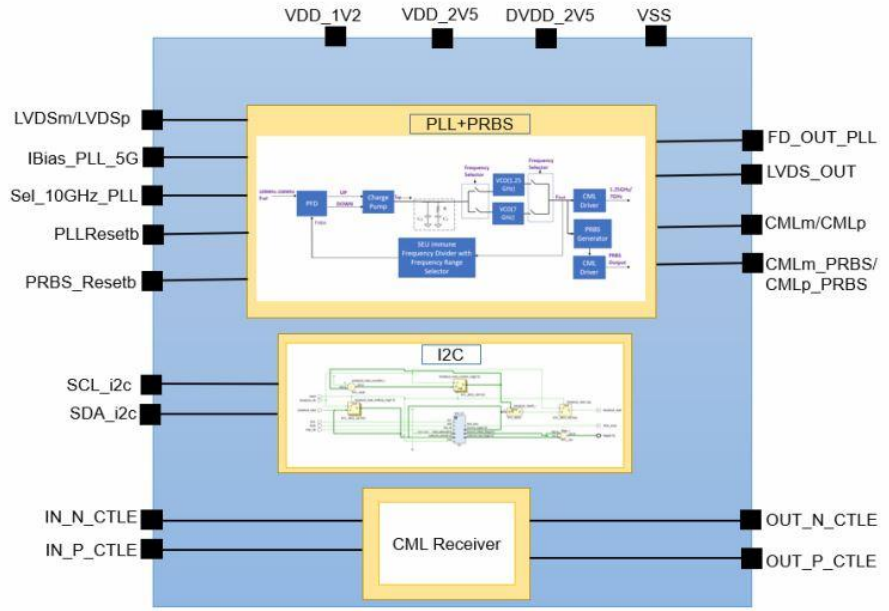
Functional Block Diagram:



Previously reported on irradiations of DUT2, Now updating collaboration with DUT5 results

X-ray irradiations setup

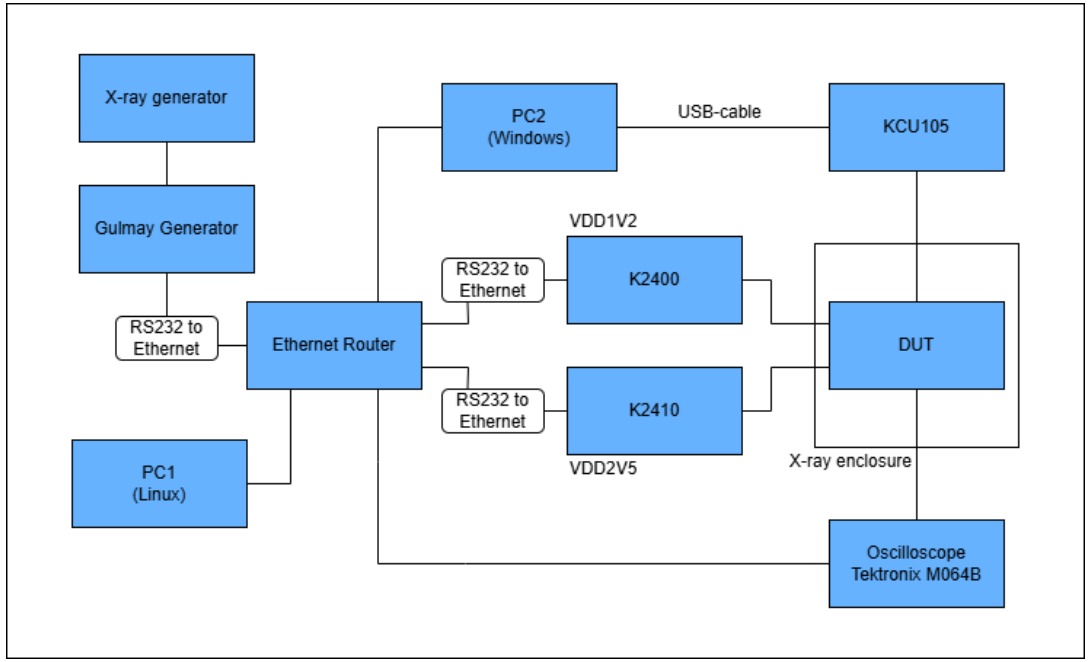
CTLE input: 4GBits/s 2GHz signal via KCU105 and SMA cables.

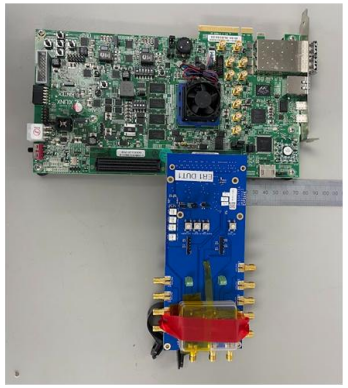
CLTE output: measured with oscilloscope.

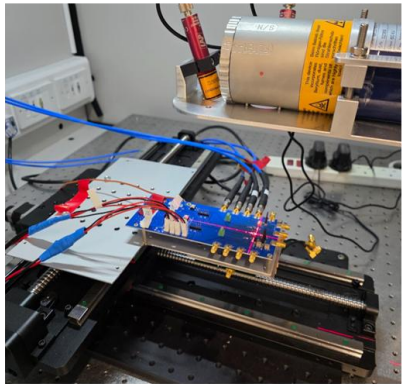
DUT (inc. CTLE): supply current and voltage monitored.

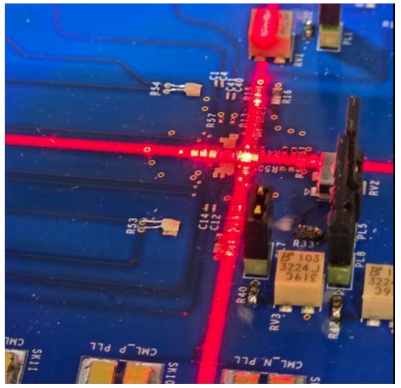
Automated irradiation:
Dose Rate = 104 krad/min;
Irradiation step lasts 48.6 minutes;
(i.e. TID ~5.0544 Mrad)

Irradiation performed until the eye amplitude of the CTLE output reaches 1/10 of initial amplitude









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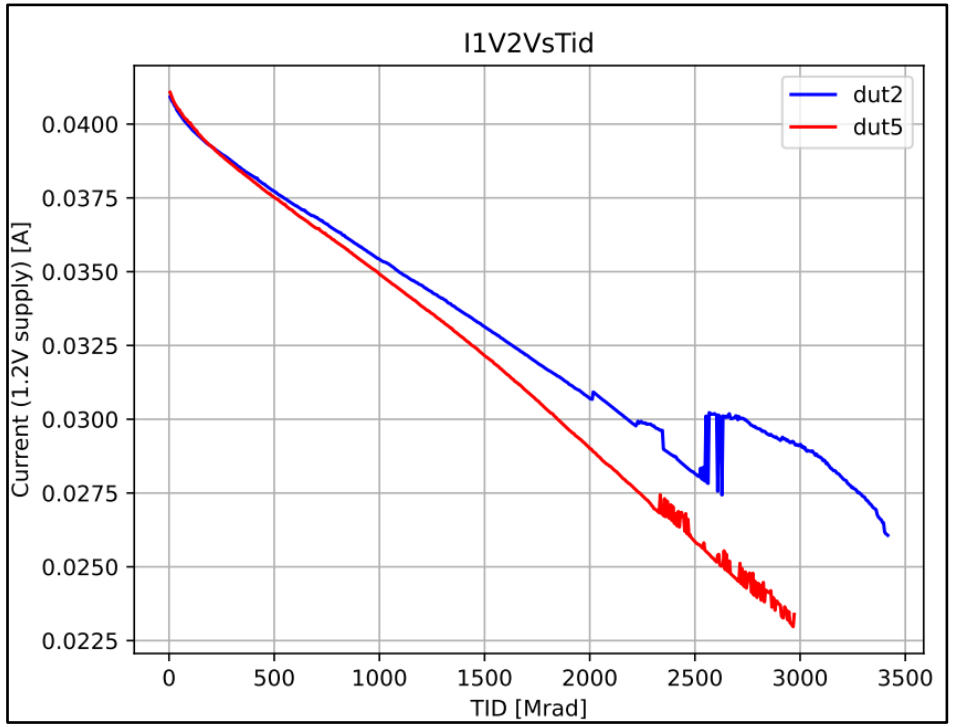
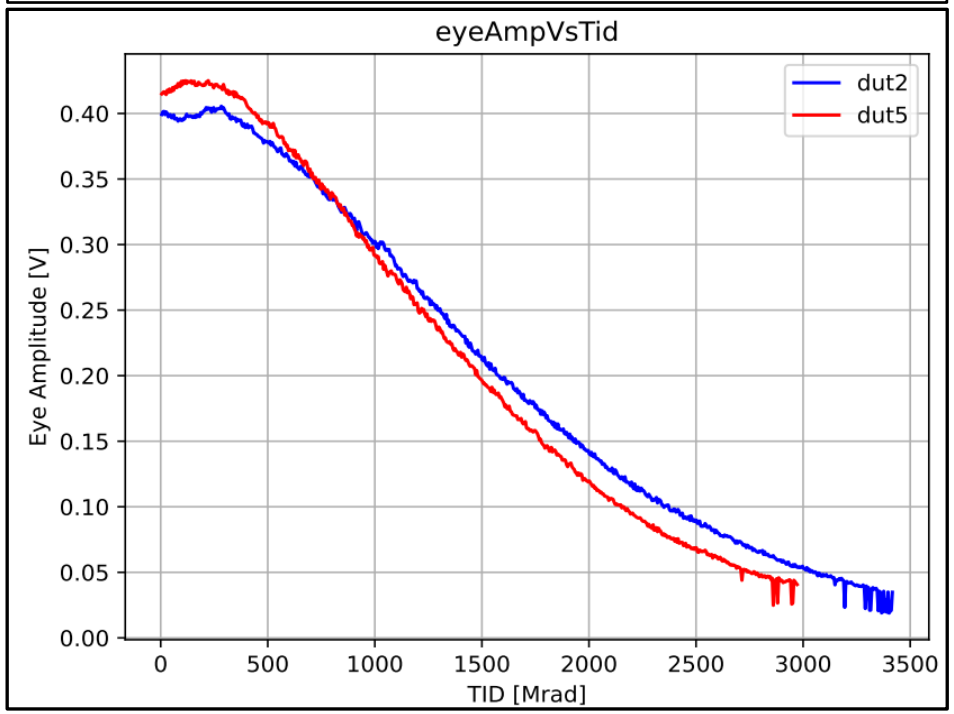
DUT5 – key results



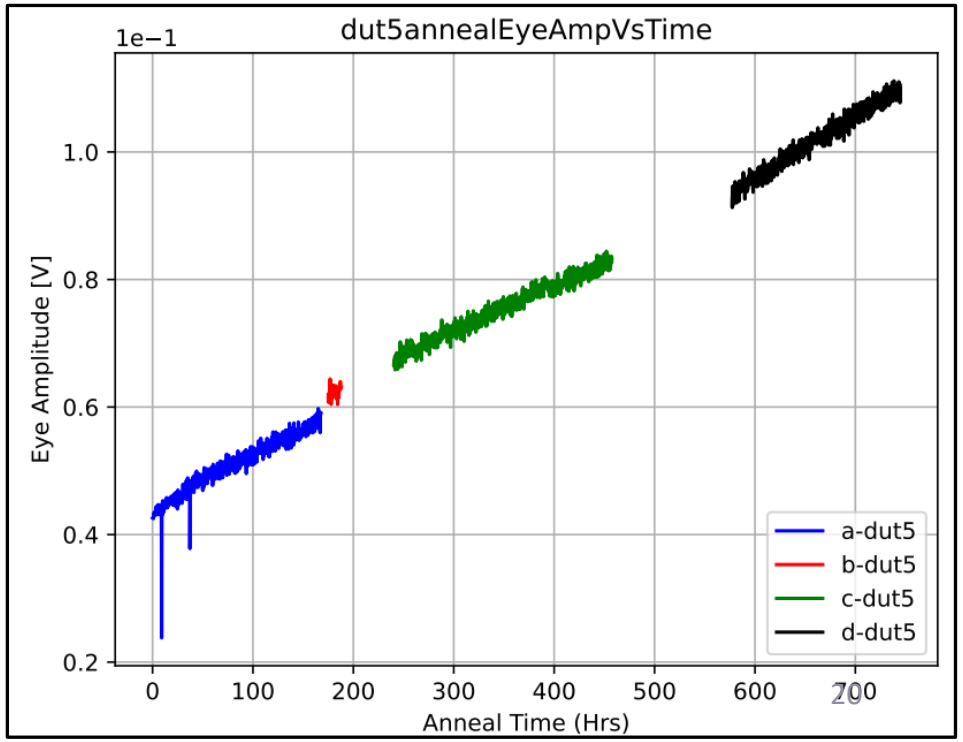


Irradiation period 02/05/2025 - 23/05/2025 (i.e. ~21 days)

CLTE eye amplitude of DUT5 reached ~1/10 at ~2.972 Grad.

Results compared to DUT2, macroscopic trends comparable.
Part to part variation observed.

DUT5 annealing monitored after irradiation (ongoing)



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ER1 RAL DUT - Conclusion

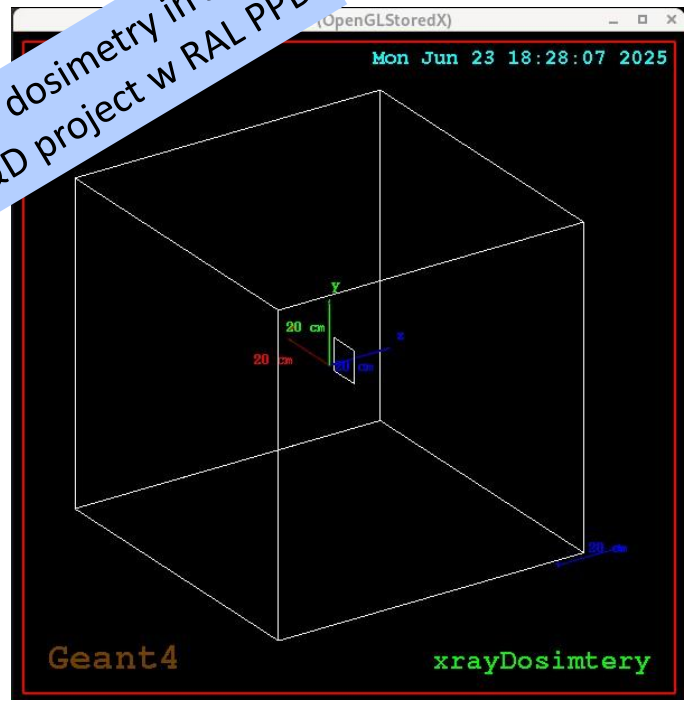
- Completed irradiation of DUT5;
- Ambition to irradiate one more DUT in time for IEEE NSS in Nov. 2025;
- Developing skills on TID irradiations synergetic to MPW2-SLDO and MOSAIX;
- In parallel, started to work on a dosimetry project to improve dose estimate to SiO2. [w RAL PPD]
- All this work is free-of-charge to the project
  - L.Godfrey, apprentice

IEEE NSS 2025, poster proposal, submitted

TID irradiations of a 65 nm CTLE prototype for ePIC SVT

M.Borri, J.Glover, L.Godfrey, W.Helsby, A.Hill, S.Mathew, I.Sedgwick, C.S.Tse

Xray dosimetry in SiO2: R&D project w RAL PPD



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Overall conclusion

- MPW2 SLDO will be received in Sept and electrical tests will follow.
- Involvement in MOSAIX testing via ITS3 work is being arranged.
- X-ray irradiations at DL are being carried on ER1 RAL DUTs.

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