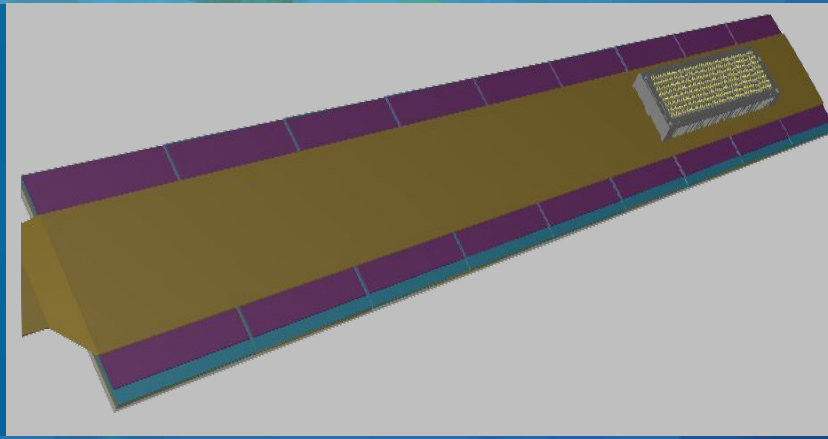
The ePIC Barrel Imaging Calorimeter

AstroPix Wafer QC, Modules and Staves



Manoj Jadhav
Argonne National Laboratory

Sanghoon Lim
Pusan National University

for the Wafers, Modules, and Stave Green Team

BIC General Meeting
June 17, 2025

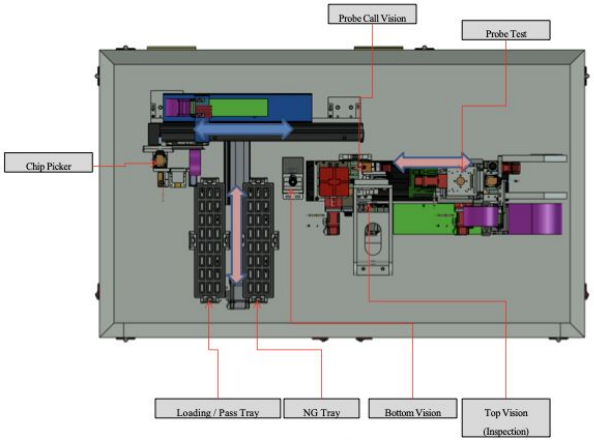
News

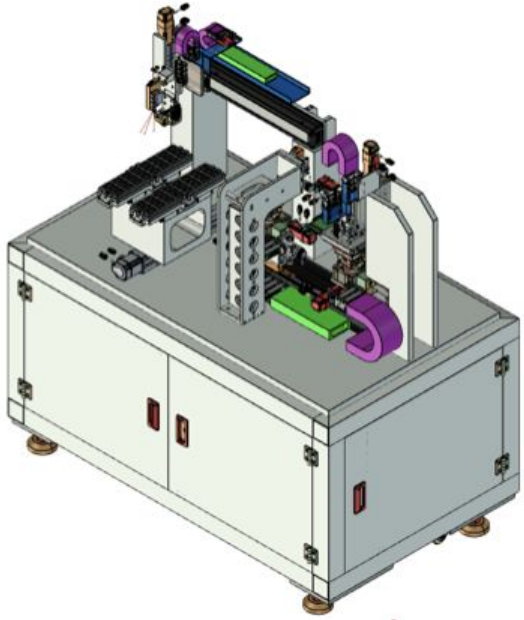
- Wafer QC and Module/Stave meetings
  - wafer QC meeting - 5 pm CT (Indico webpage)
  - Module/Stave meeting - 4:30 pm CT (Indico webpage)
  - Alternative weeks on **Mondays**

- Work in progress
  - AstroPix Chip QC test stands under production
  - Module and Stave support test articles delivered to Argonne
  - AstroLinx (Module PCB) design is uploaded to Box (Plan a review soon)
  - Module carriers and handling tools design in progress
  - Wire-bonding procedure under discussion

Wafer/Chip Probing

- Wafer/chip level testing prior to module assembly
- Quality Control Testing
  - IV measurements, power on, SEU check, Register check, FIFO test, analog and digital scan, threshold tuning, calibration checks
- Test stand production started
  - Delivery expected in August 2025
  - V3 probe card design ongoing
  - Allow us to validate the chip QC testing on ~80 v3 chips during PED phase
- V5 design update will be ready in the fall





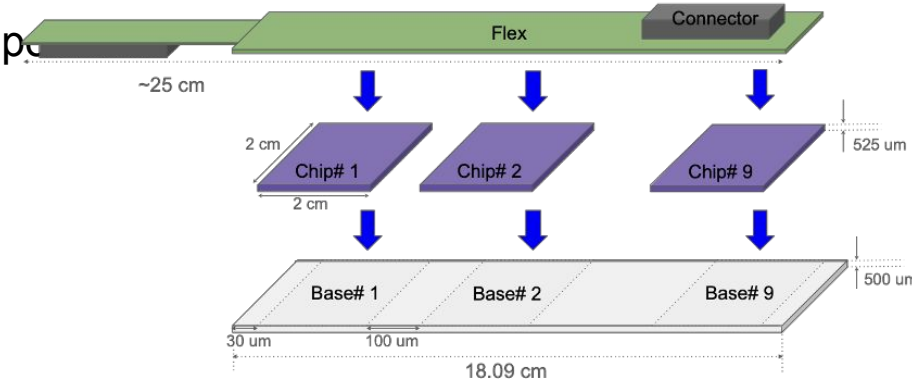
- Dummy chip with pad structure for assembly

Modules

Design

- AstroPix Module comprises of 3 layers/comp
  - **Base Plate (Aluminum)**
  - **Nine AstroPix Chips**
  - **Flex PCB**
- **Failsafe design** - easy to rework on Stave

AstroLinx: Module PCB



Not Scaled

1.7 mm - Connector

1.7 mm - AstroLinx

0.1 mm - Glue

0.525 mm - AstroPix

0.1 mm - Glue

1 mm - Module Baseplate

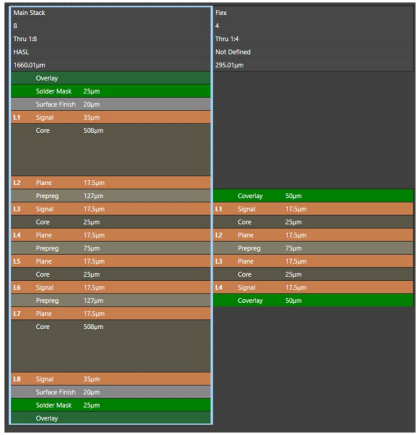
Iterated stackup with AstroLinx design and mechanics module baseplate/stave/tray design to fit within envelope

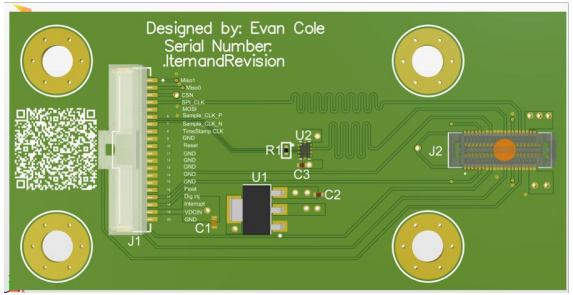
Modules

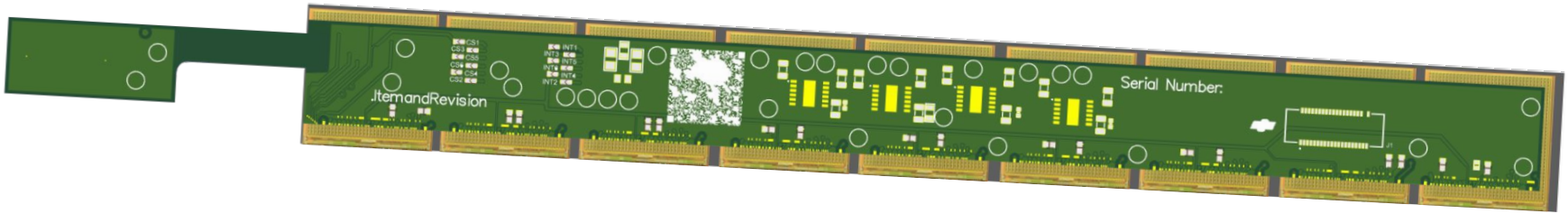
AstroLinx

- PCB design completed for AstroPix v3
- Final minor mechanical fixes undergoing
- PCB thickness ~1.66 mm
- Bulkier design than expected in order to keep a single flavor for all modules
- First fabricated parts are expected this summer
- Another iteration is anticipated for final design (v5)
- Plan to build ~6 modules with extruded Al module base, AstroPix v3, and AstroLinx this summer/fall
- The bridge card to test modules with AStep hardware is designed

Current Stackup



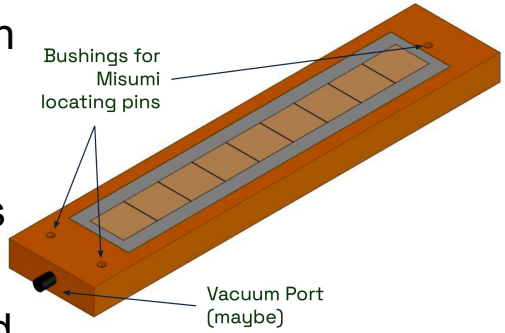


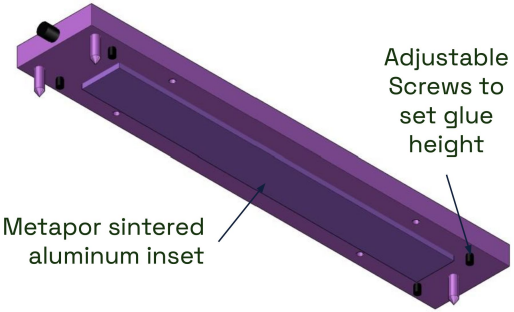


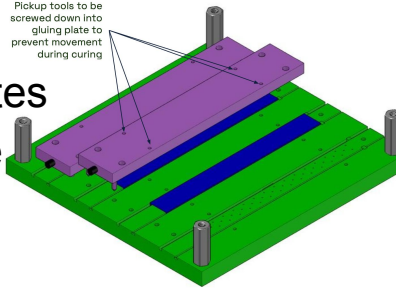
Modules

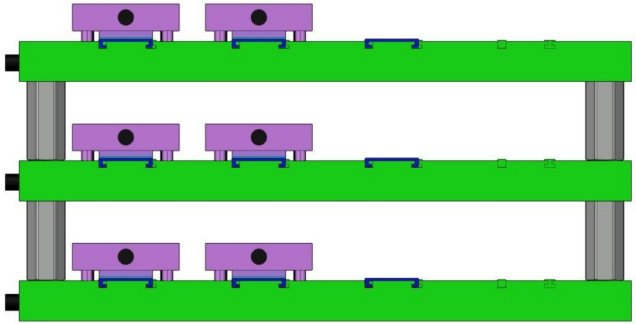
Toolings for assembly

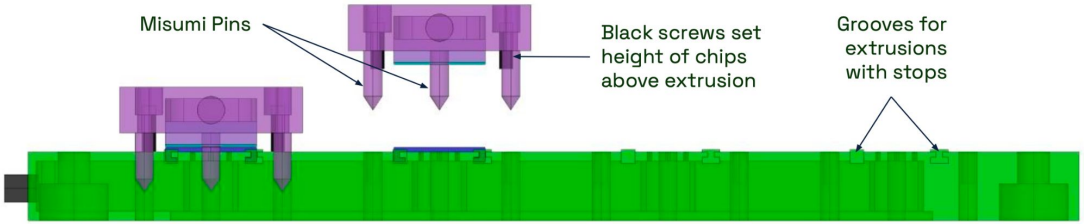
- Align the chips on Al base plate with chip-to-chip gap of 100 um
- Aligns AstroLinx with chips
- Allow glue amount control and fixes glue height during cure time
- Multiple modules can be assembled parallelly
- Glass dummies are distributed to sites
- Chip dummies with pad layer will be fabricated







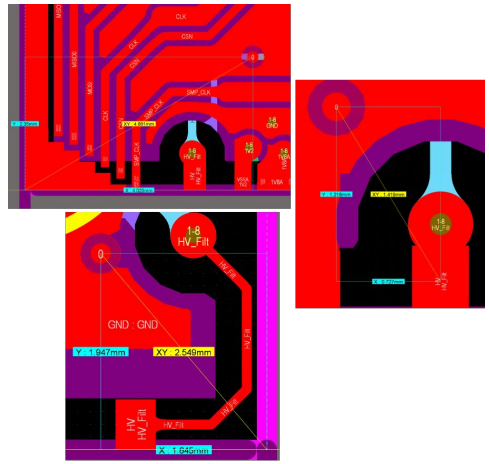


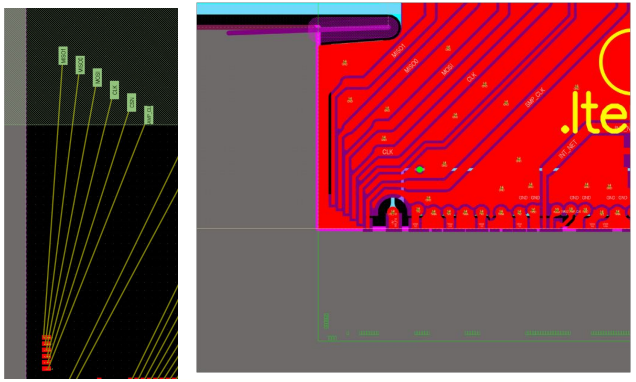


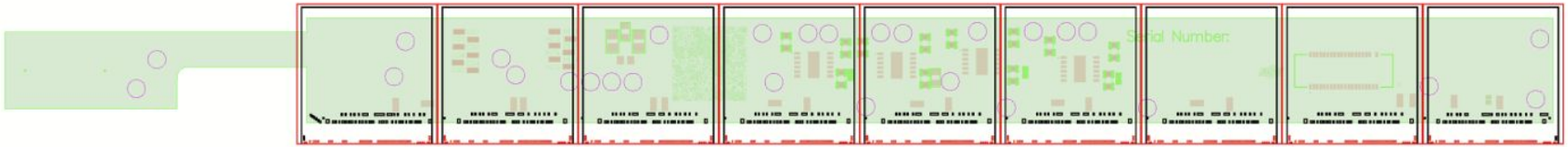
Modules

Wire Bonding

- Chip alignment study ongoing
- Added fiducials for wirebond program
- Pickup area on hybrid PCB for toolings
- AstroLinx provide some room for alignment
- Staircase pad structure provided for SPI pads on first chip
- AstroLinx aligns with left-bottom edge of first chip (two more option are under consideration)
- To avoid shorts on SPI pads - option to go for thinner wires (17 µm instead of 25 µm)







Modules

9-chip PCB prototype

- Mockup the AstroLinx electronics
- Power distribution stability
- Daisy chain read-out
- Testing DAQ development

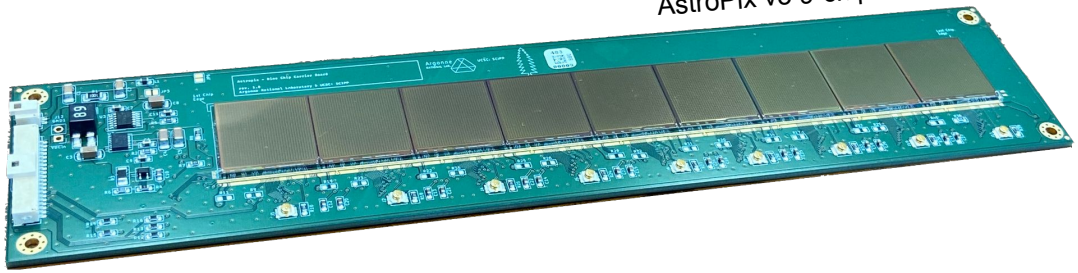
Testing with AStep card with CMOD FPGA

- Can test up to 3 modules with single card
- Started with Injection scan with individual pixel/chip
- Issue with fluctuating baseline
- borderline pixels fail to respond

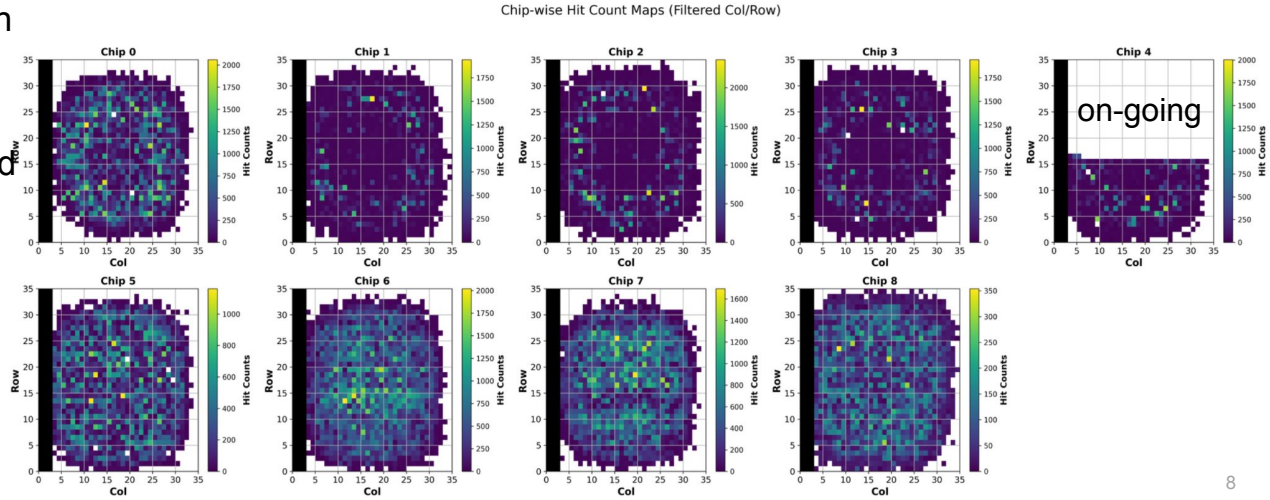
Two more PCB ready for testing

- one with single chip
- one ready with full assembly

AstroPix v3 9-chip board



Daisy chain readout through 9 chips



Summary

- Biweekly follow up meetings for Astropix wafer QC and Module/Staves
- Test articles for Module/Stave support delivered to Argonne
- Glass dummies were distributed to all 3 sites
- 9-chip PCB board tested with injected signal - show daisy chained functionality
- Chip level QC test system under production
- AstroLinx, a rigid+flex PCB design completed and under review
- Bridge card design is almost completed

Thank you!

BACKUP