Chip test system readiness

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Outline

1. Introduction
2. Chip test machine
3. AstroPix_v3 probe card
   a. Approach
   b. Status
4. v3 chip test w/ astep-fw + sw

Introduction Automated chip test system

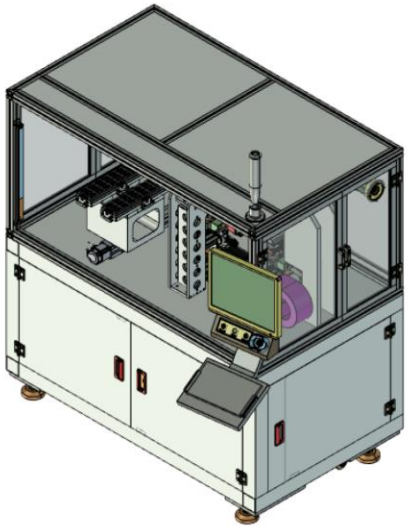
- **Developing an automated chip test system**
  - Composition:
    a. Test machine (under development by C-ON Tech):
       Chip handling + Optical alignment and vision inspection
    b. Probe card for the AstroPix_v3
  - Major design goals of the test machine
    a. Capable of scalable, efficient, and precise tests for each individual chip
    b. Versatile and flexible design based on the modular structure
       i.e., adoptable with the current v3 and the future v5 chips, by module replacement
  - Probe card
    a. Based on the single chip carrier board for AstroPix_v3
    b. Perform the carrier board's functionality via needle contact and flexible cable,
       while keeping FPGA and Proximity boards as they're now
    c. PCB production started yesterday (Oct. 20th)

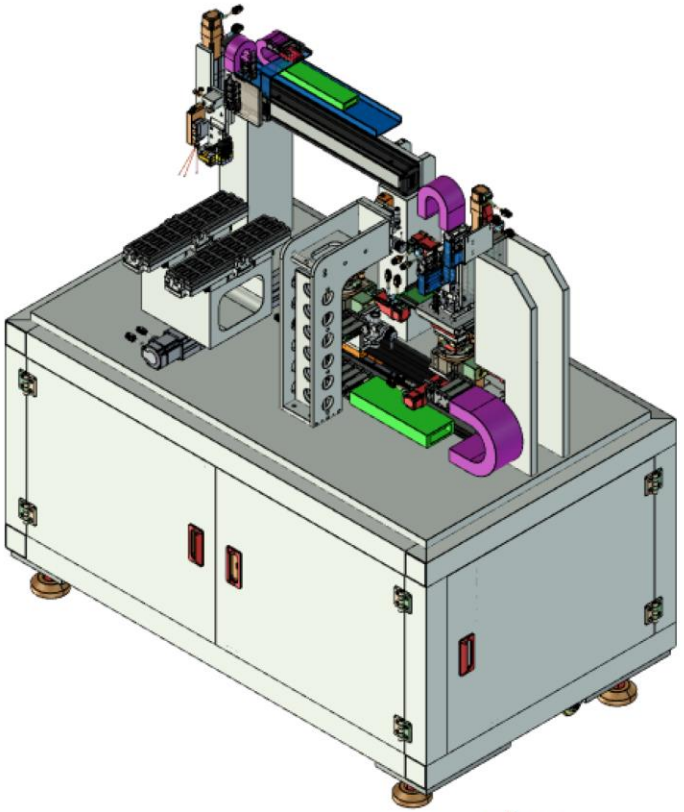
Chip test machine Overview

Introduction to Equipment

➢ Description

- Probe Test System
- Tray Loading : Manual
- Probe Test Motion : Z Axis – Servo Motor
- Chip Picker Motion : X,Z Axis - Servo Motor
- Transfer Motion : YAxis - Servo Motor
- Vision : Dispensing Align Top(1EA)/Bottom Vision(2EA)
- PC Control
- Main Equipment Size : 1,500 (W) x 950(D) x 1700(H)
- Power : 220V 1P 50/60Hz
- Inspection spec : Min 45um





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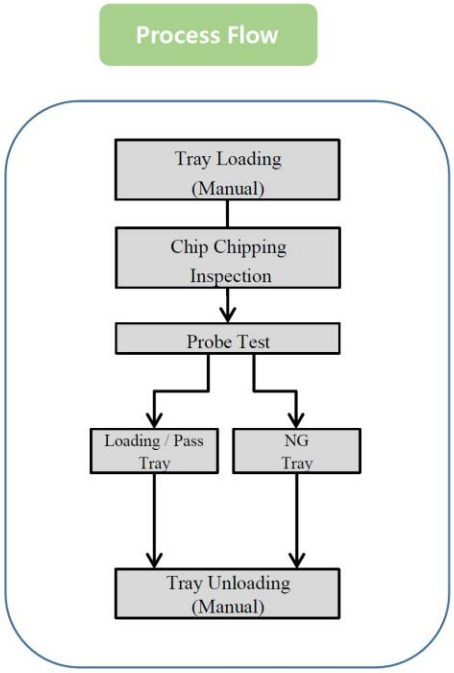
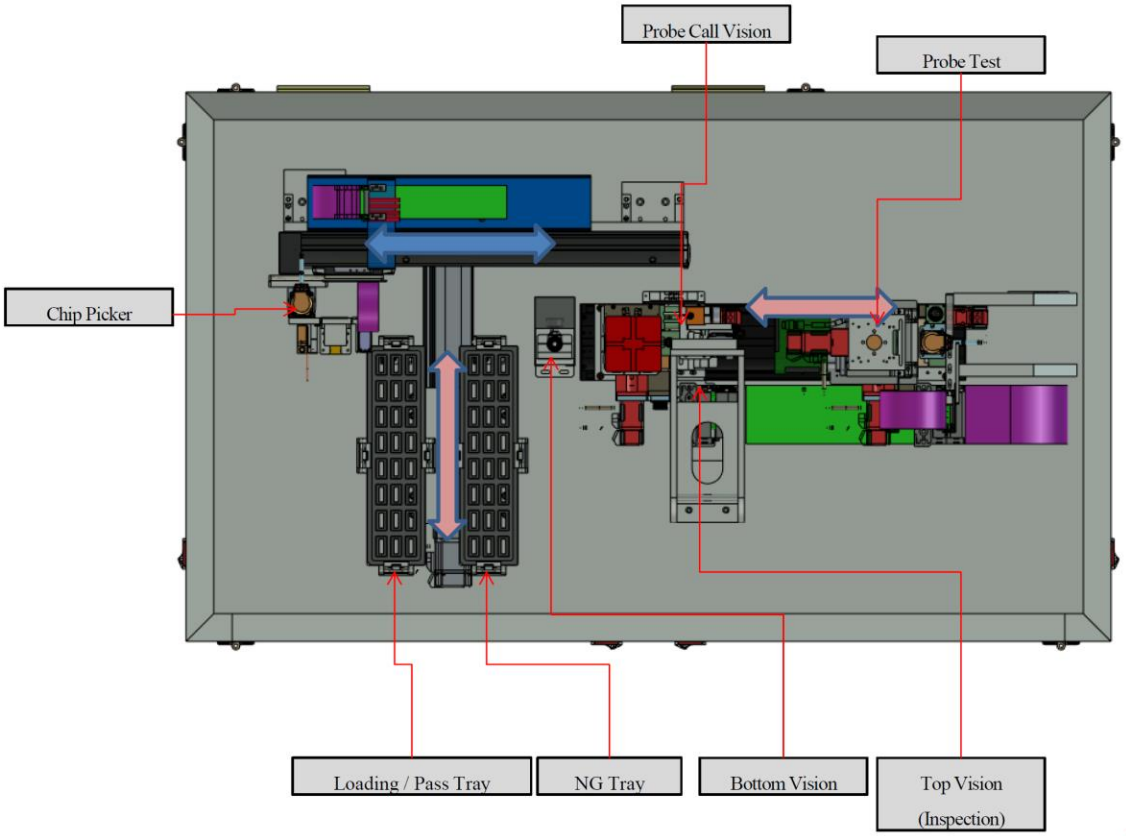
Chip test machine Workflow

Process Flow





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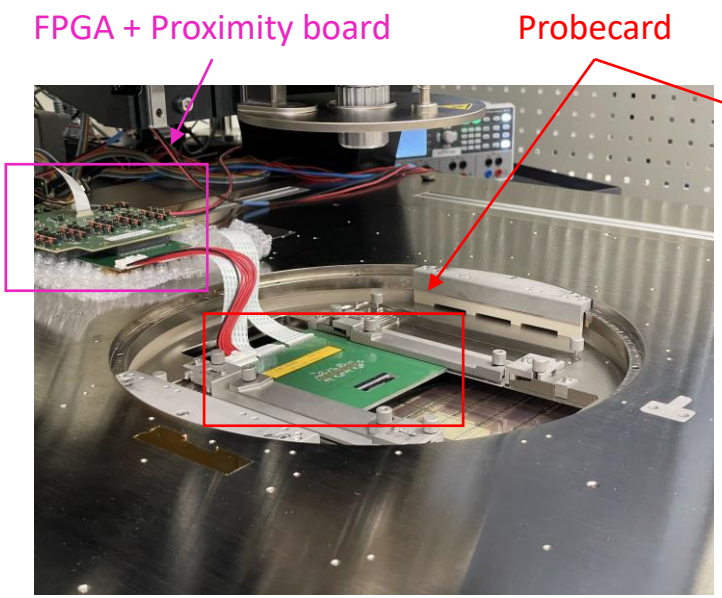
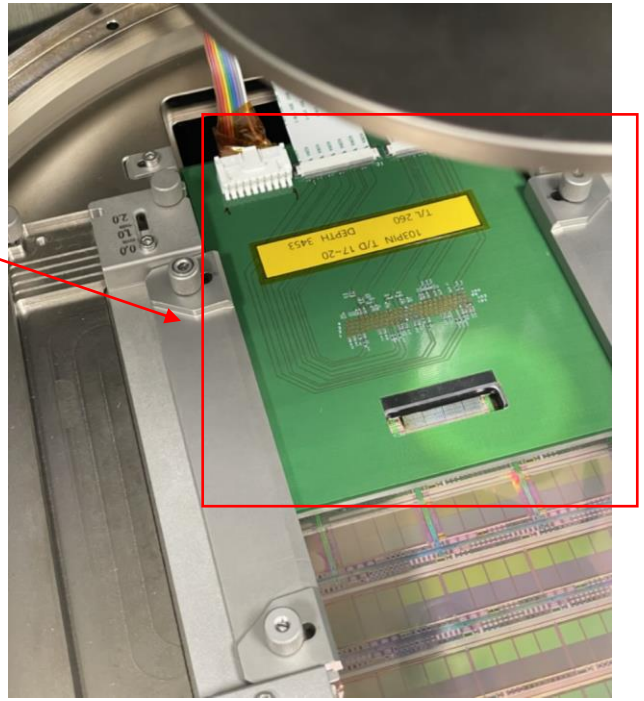
Probe Card Approach (1/2)

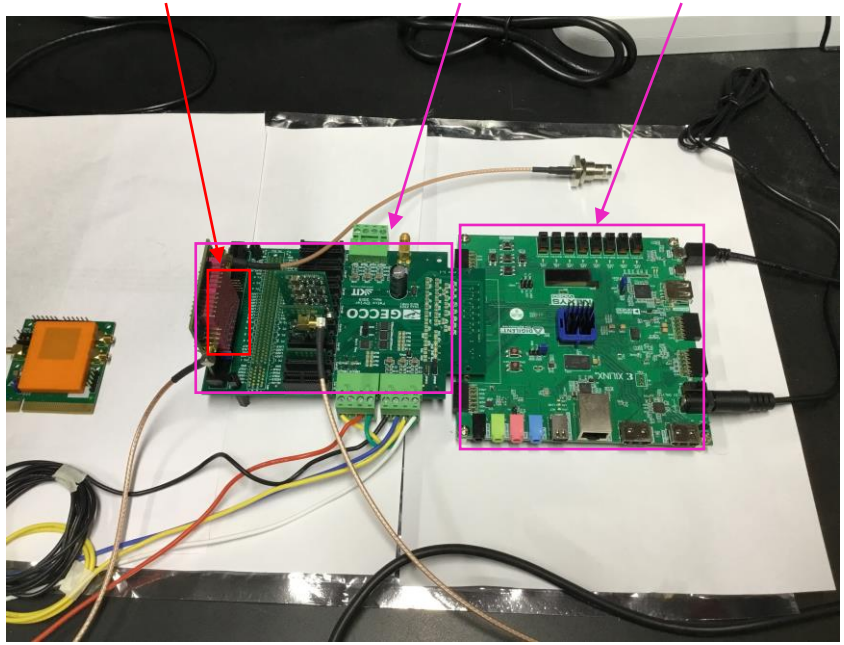
- **Benchmarking the wafer testing system for ALICE ITS3**
  - CAVEAT: this is an example!
    a. Separated to “FPGA + Proximity board” + "Probe card”
    b. PNU plans to make a similar system

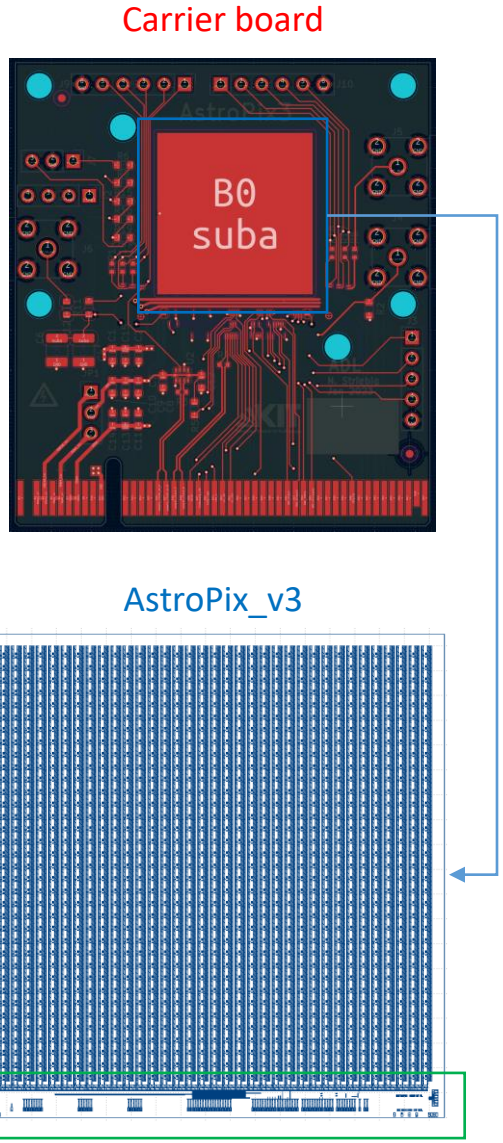




Probe Card Approach (2/2)

- **Current AstroPix_v3 operation**
  - FPGA board + Proximity board + Chip on carrier board
    a. Plan to keep the "FPGA + Proximity" parts as they are
    b. Required probe card: do current carrier board's function
    → Carrier board's circuit should be transferred to new PCB

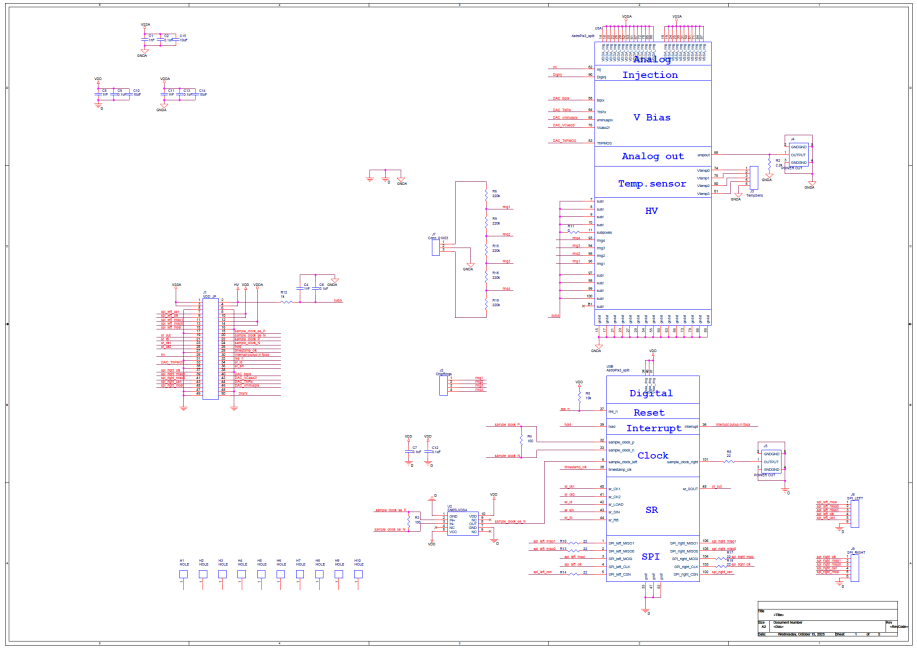


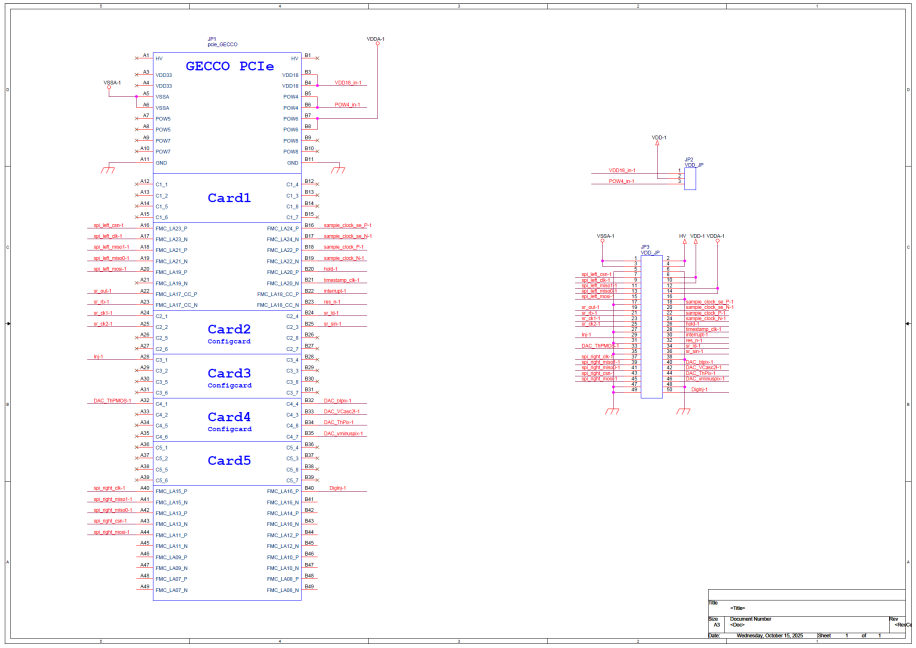


Probe Card Production status (1/3)

- **PCB schematic (ported from carrier board + updated)**
  - Provide power and bias from:

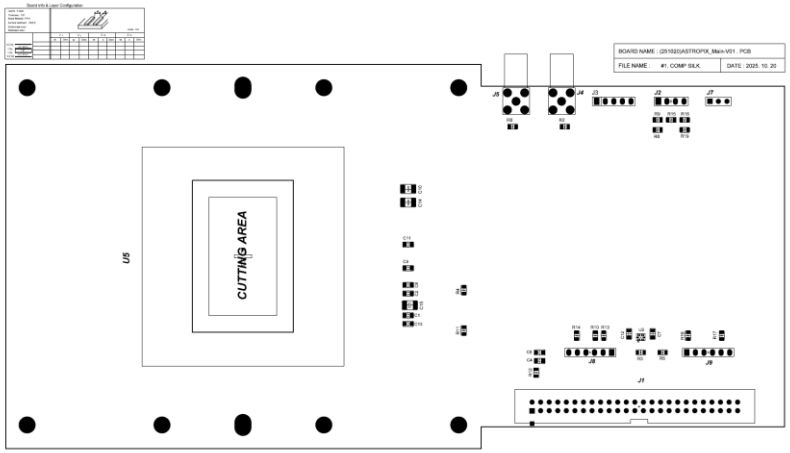
    proximity (GECCO) board → adapter card → cable → probe card

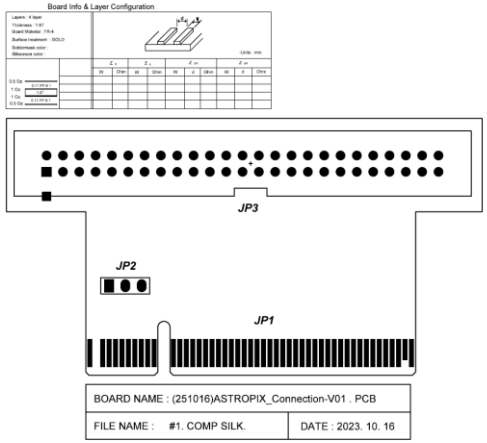


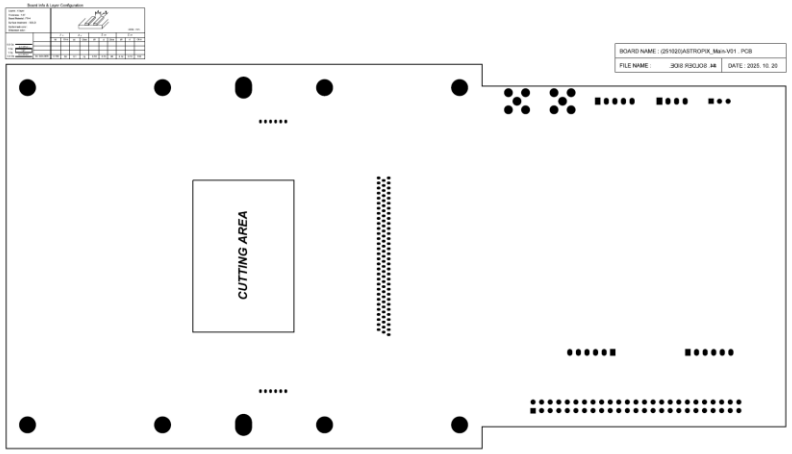


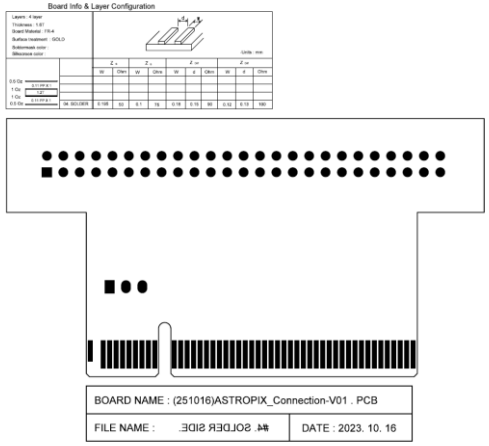
Probe Card Production status (2/3)

- **PCB with components on it**



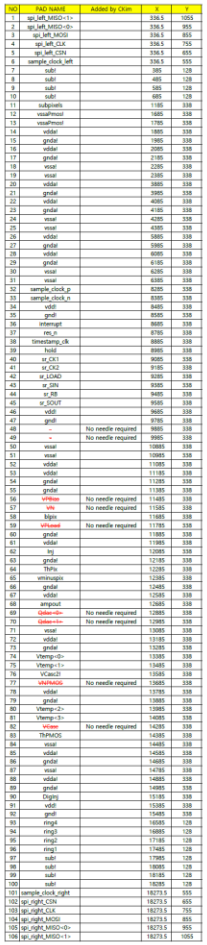


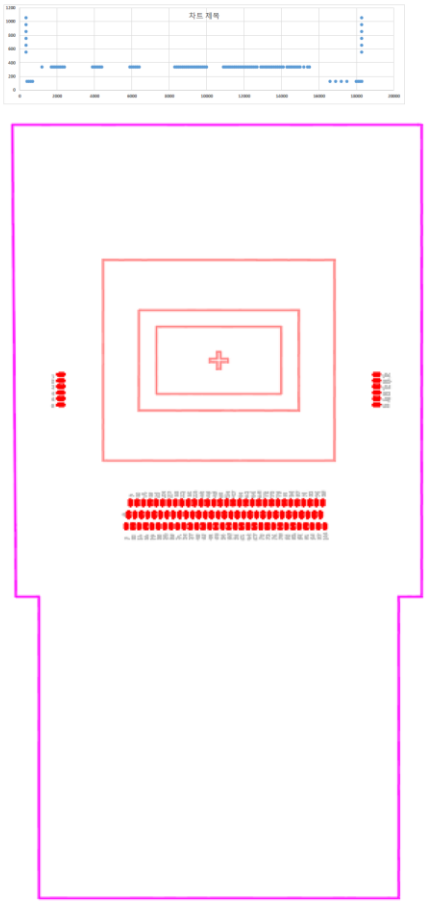




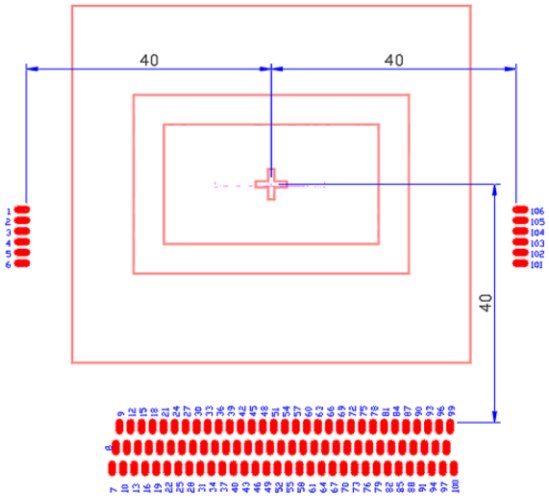
Probe Card Production status (3/3)

- **Probe needle arrangement: up-to-date pin-needle mapping (Oct. 20th)**
  - Total 97 valid pins out of 106 (which will have corresponding needle)





Pads

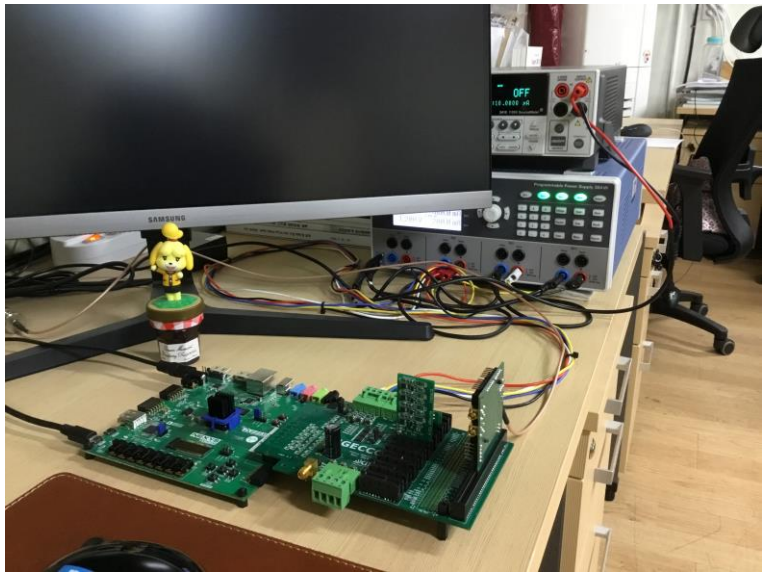


v3 chip test w/ astep-fw + sw

- **v3 chip operation via astep-fw and sw**
  - Base setup PNU have been used so far:

    FW: astropix-fw (last update: July 2024), SW: astropix-python
  - Operate v3 chip w/ astep-fw and subordinated sw
    a. Built fw by using “gecco-astropix3.tcl” setting and succeeded program it on Nexys-video
    b. Succeeded data taking w/ “astep-fw/sw/scripts/benchtest.py”
    c. Currently writing a light-weight version of the script
    d. Plan to do the source test and analysis soon
  - A script should be prepared for mass chip test:

    Plan to implement each function one by one

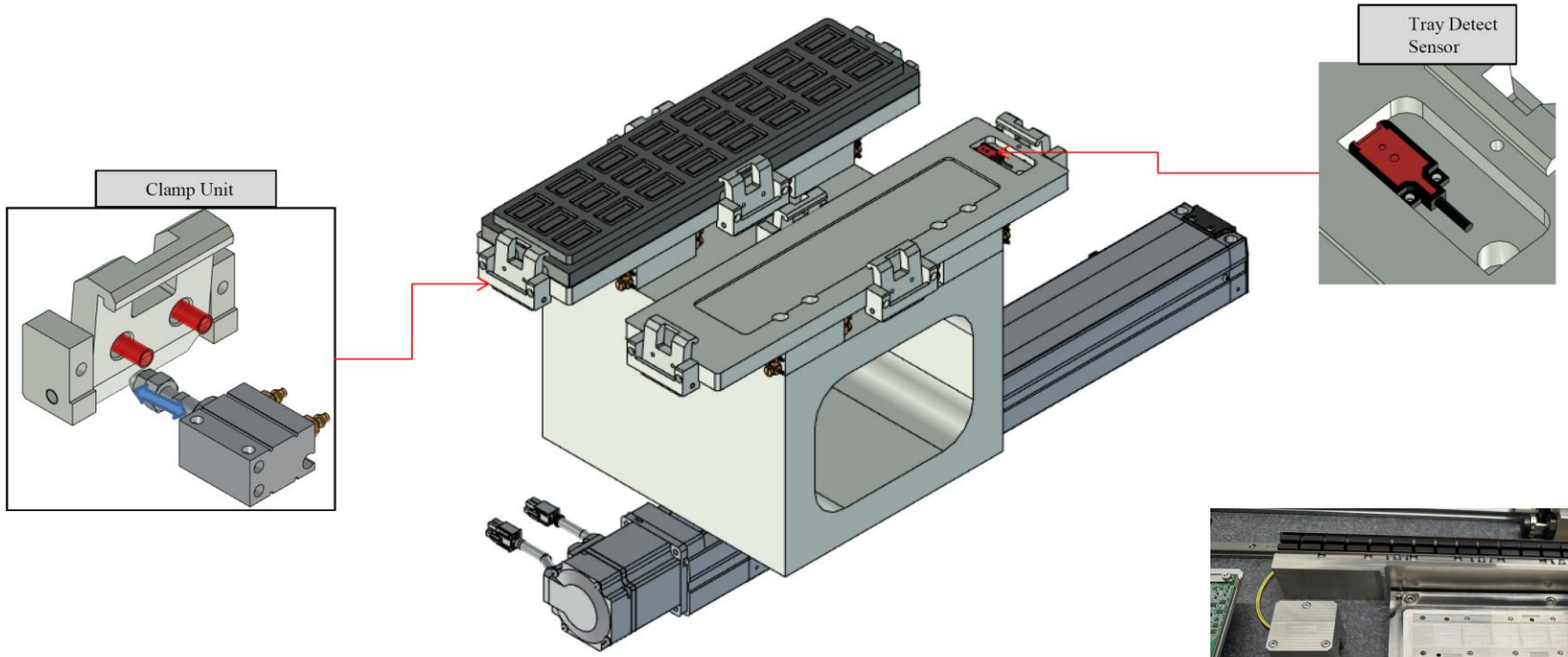


Summary and timeline

- **Chip test system readiness:**
  - Chip test machine:
    a. Production is finished: currently tune & calibration is underway
    b. Plan to use existing probe card (ALICE ALPIDE) as a dummy to test system integrity
    c. Waiting for the AstroPix_v3 probe card
  - AstroPix_v3 probe card:
    a. Design and crosscheck is finished, PCB production started at Oct. 20th (yesterday)
    b. Expected elapsed time: end of Nov. or early Dec., at the earliest
       b-1. PCB production and Component commission: ~3 weeks
       b-2. Needle assembly on the probe card: ~2 weeks
  - Data taking and analysis w/ a-step fw/sw
    a. Currently succeeded to run v3 chip with them (validity of data should be checked)
    b. Prepare a test script capable of testing at least a few functions (e.g., power, threshold scan, etc.): before probe card delivered – by end of Nov.

Backup Chip test machine: tray loader

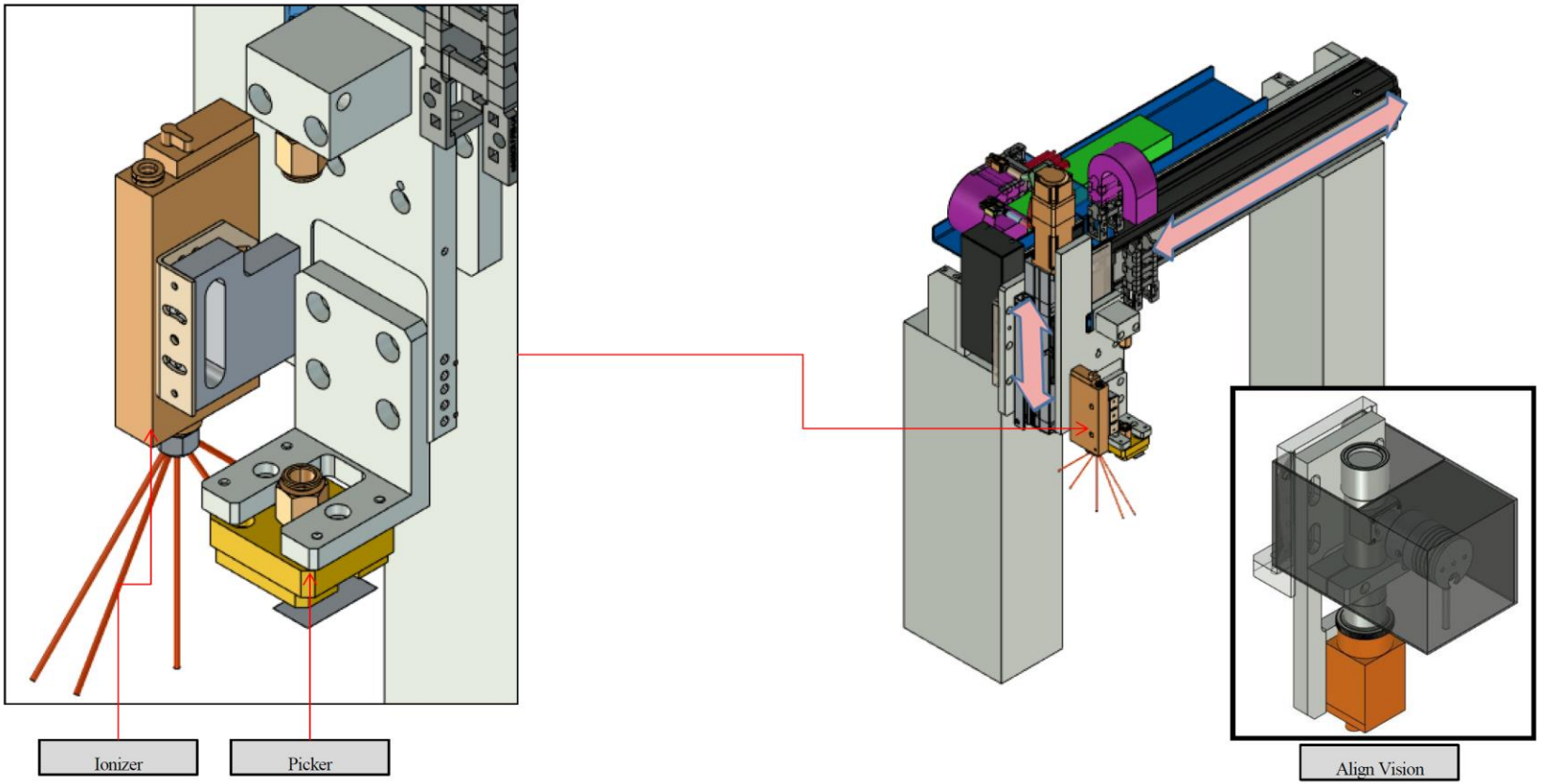
Tray Loading (Good / Reject Unit)



Example photograph of chips on the tray
(CAVEAT: this is not the device being developed!)

Backup Chip test machine: sensor picker

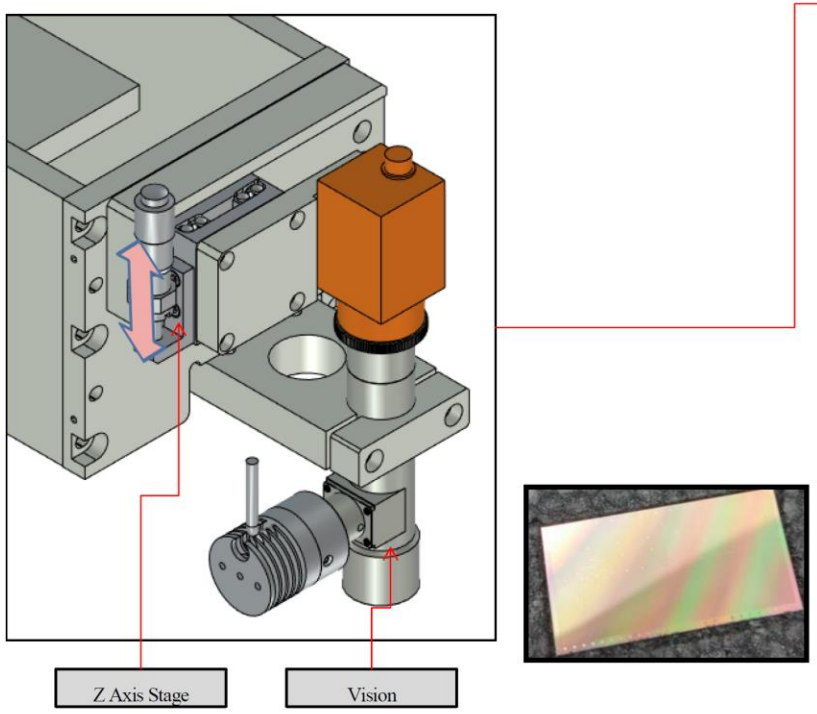
Sensor Pick up Unit

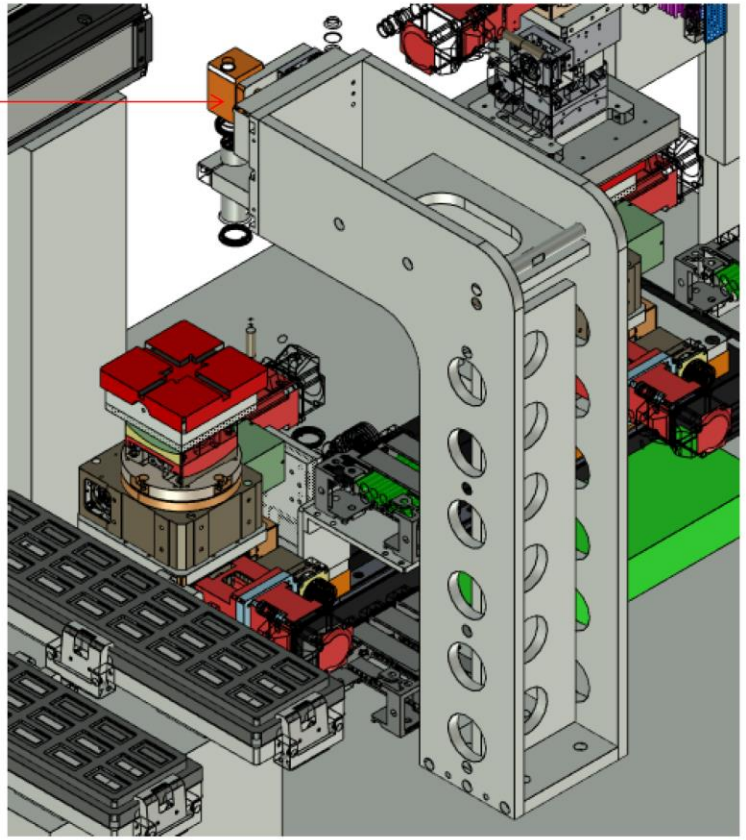


Backup

Chip test machine: chipping inspection via vision

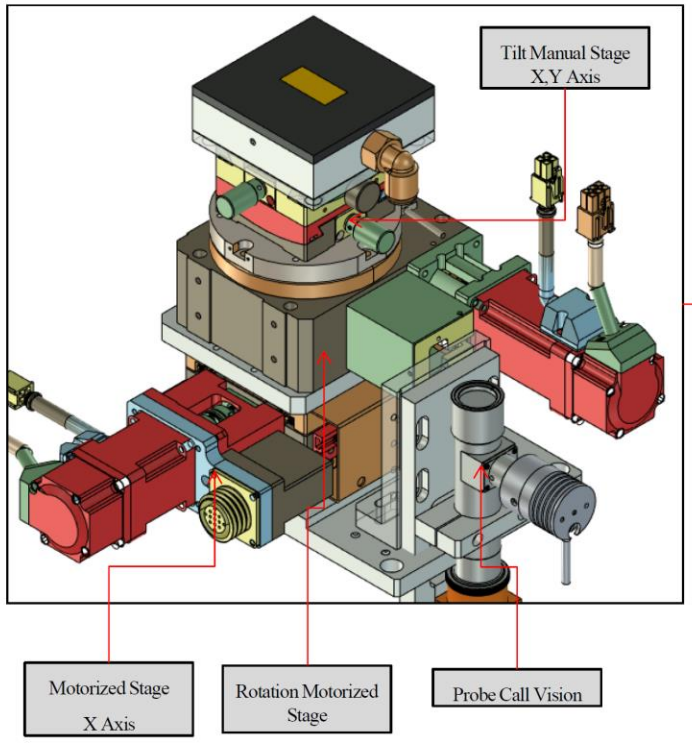
Sensor Chipping Inspection

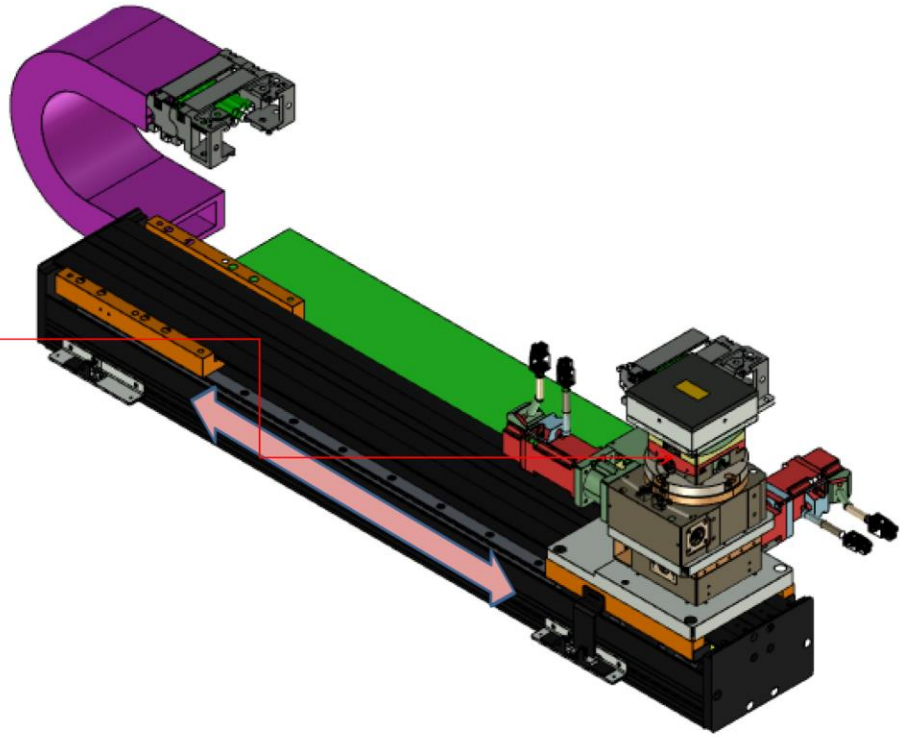




Backup Chip test machine: chuck

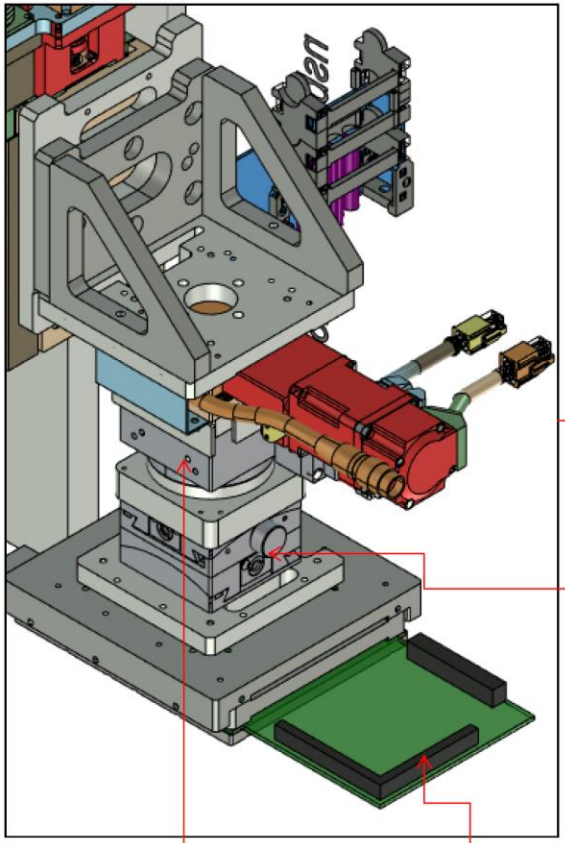
Working Stage (Motorized)

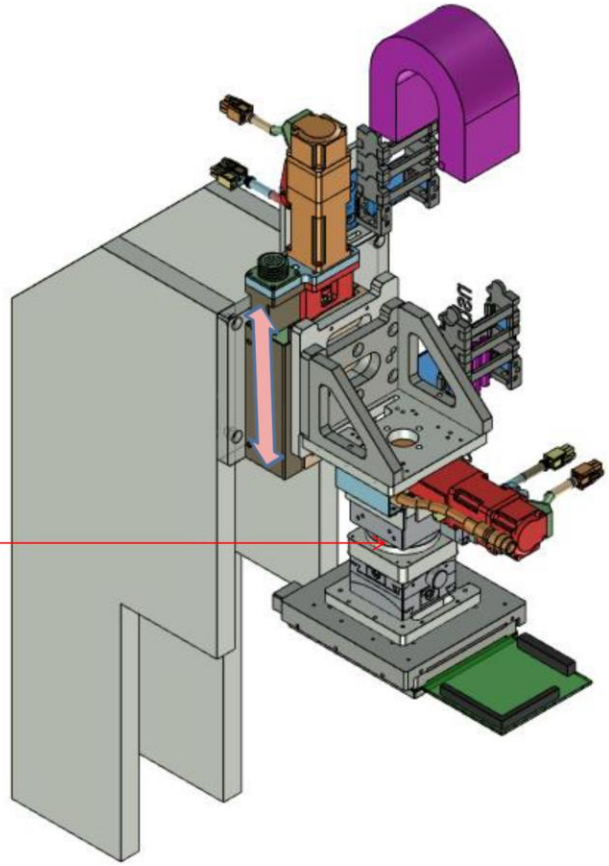




Backup Chip test machine: probing

Probe Test





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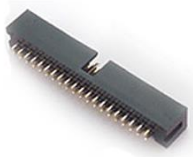
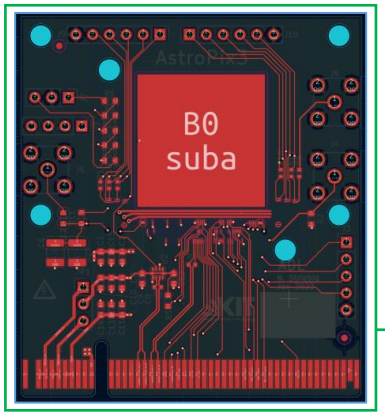
Backup Probe card operation

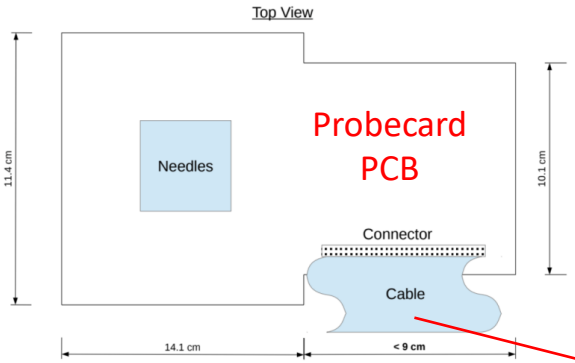
- **Operation via probe card**
  - Probe card:
    a. Contains carrier board's circuit
    b. Transfer info via 50 pins connector and cable
  - Adapter card (design is underway):
    a. To be plugged into the proximity (GECCO) board
    b. Receives info from the probe card

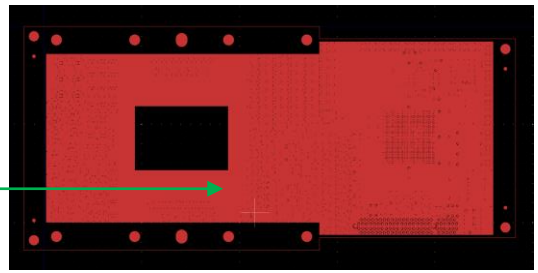
50 pins connector and cable

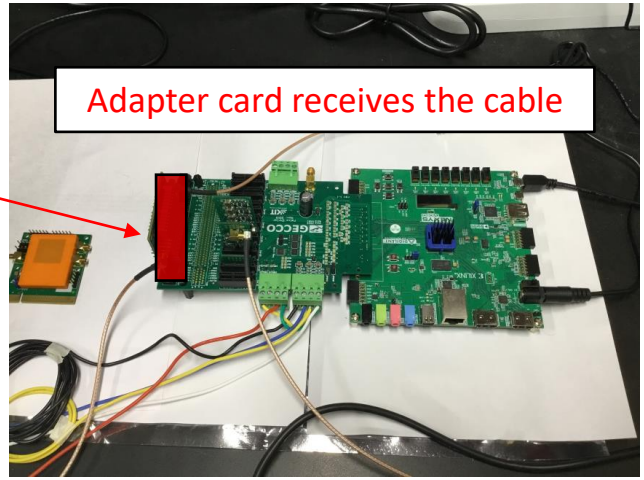


Port carrier board circuit to the probe card PCB



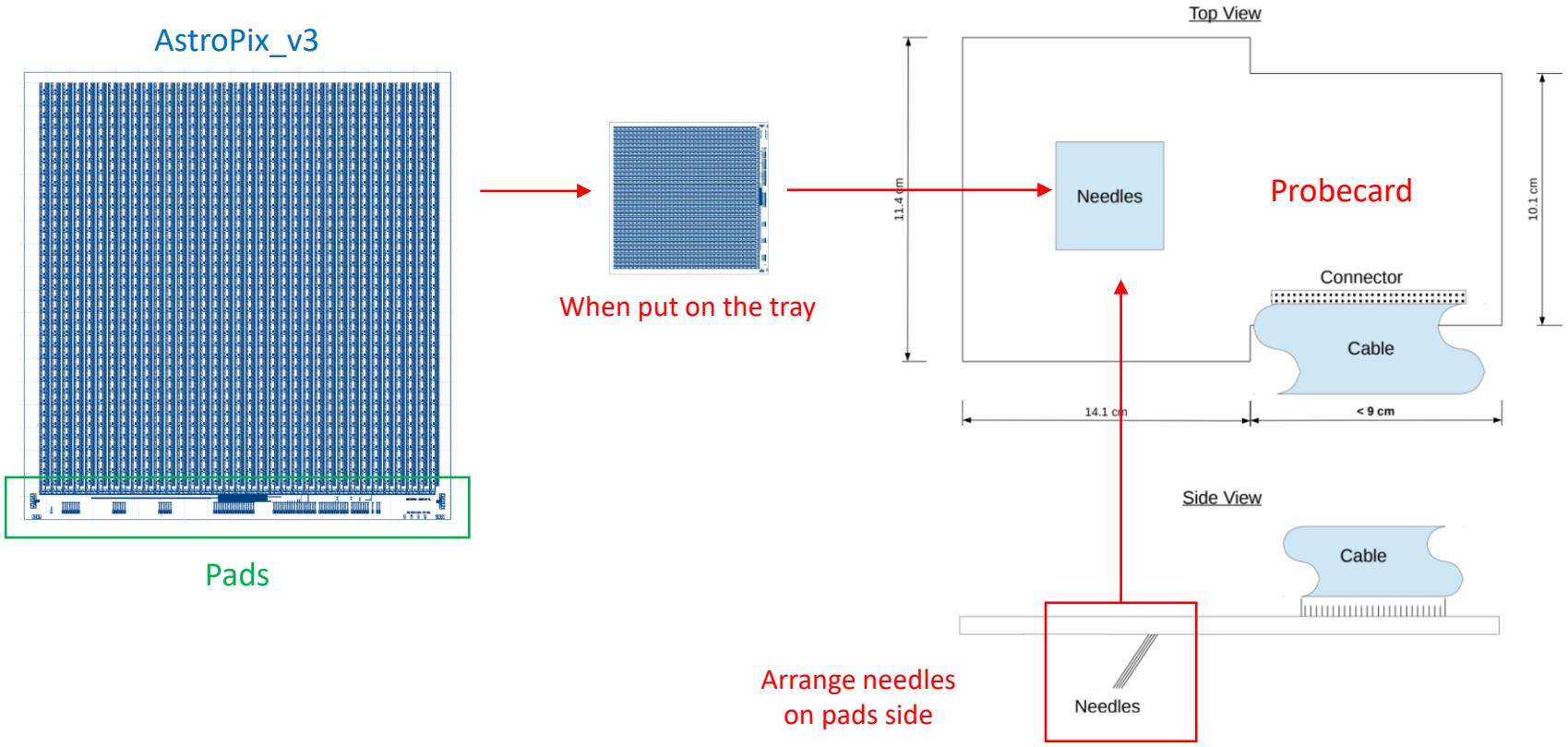






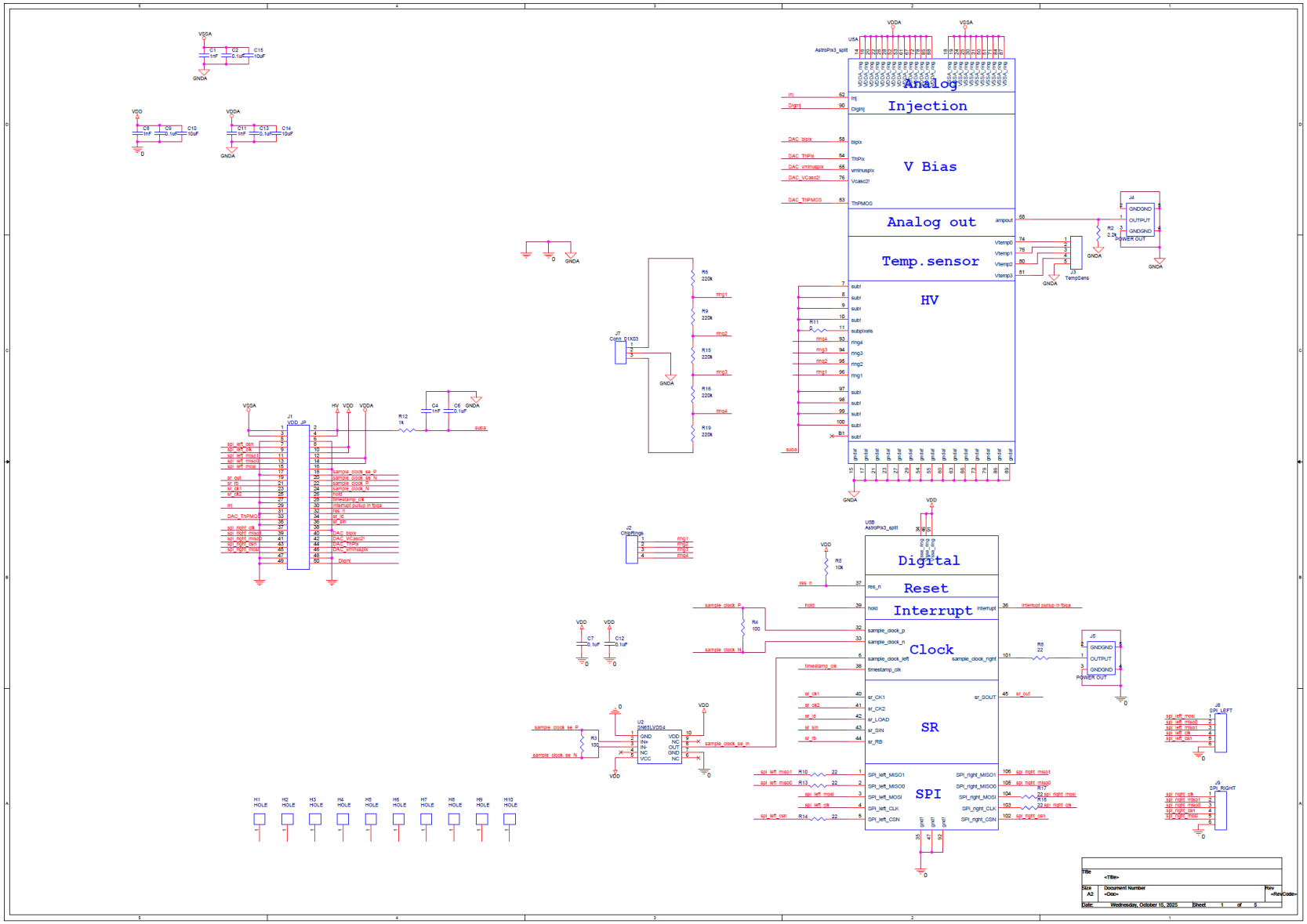
Backup Probe needle

- **Needle arrangement and contact**
  - AstroPix_v3 chip has bonding pads only at the the bottom edge: for the test,



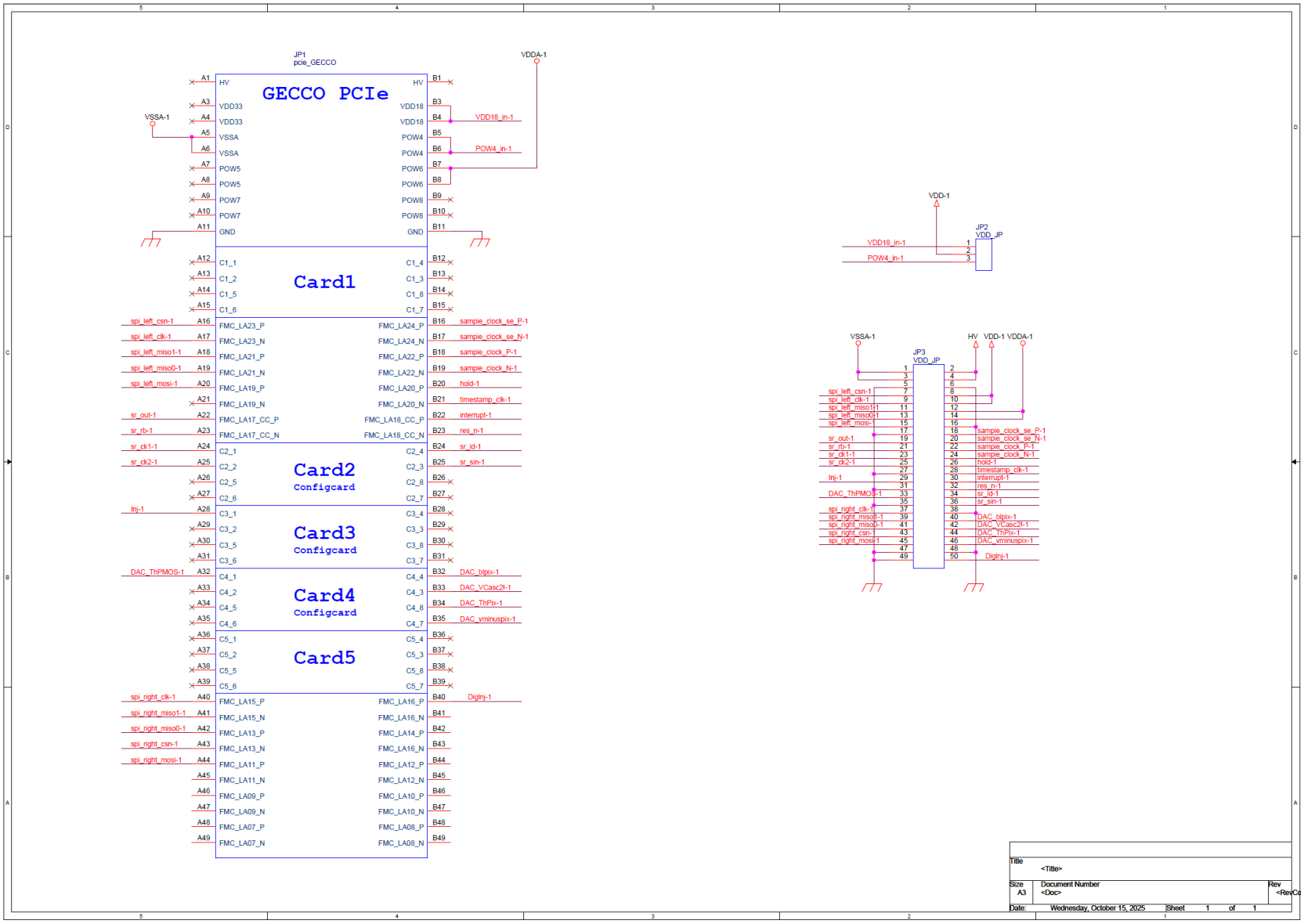
Backup

PCB circuit (probe side)



Backup

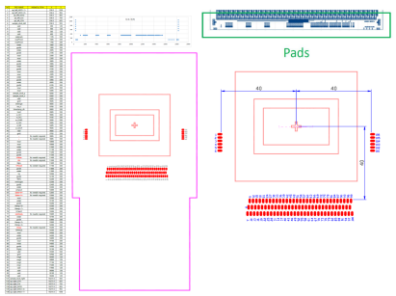
PCB circuit (GECCO side)



Backup

Pin mapping for probe needles (red marked items will be ignored)

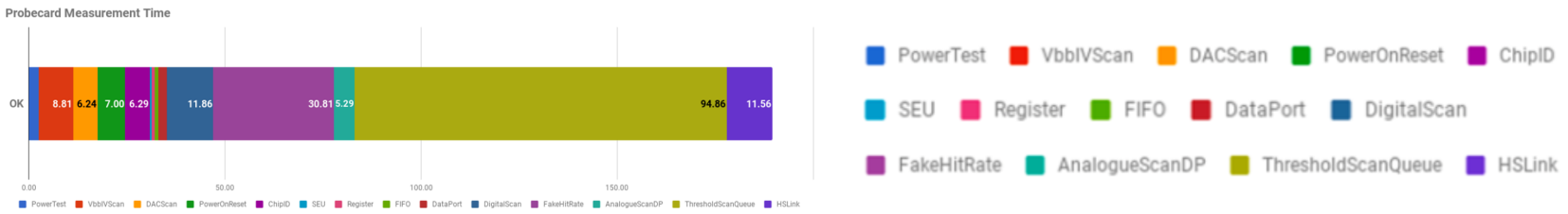
NO	PAD NAME	Added by CKim	X	Y
1	spi_left_MISO<1>		336.5	1055
2	spi_left_MISO<0>		336.5	955
3	spi_left_MOSI		336.5	855
4	spi_left_CLK		336.5	755
5	spi_left_CSN		336.5	655
6	sample_clock_left		336.5	555
7	sub!		385	128
8	sub!		485	128
9	sub!		585	128
10	sub!		685	128
11	subpixels		1185	338
12	vssaPmos!		1685	338
13	vssaPmos!		1785	338
14	vdda!		1885	338
15	gnda!		1985	338
16	vdda!		2085	338
17	gnda!		2185	338
18	vssa!		2285	338
19	vssa!		2385	338
20	vdda!		3885	338
21	gnda!		3985	338
22	vdda!		4085	338
23	gnda!		4185	338
24	vssa!		4285	338
25	vssa!		4385	338
26	vdda!		5885	338
27	gnda!		5985	338
28	vdda!		6085	338
29	gnda!		6185	338
30	vssa!		6285	338
31	vssa!		6385	338
32	sample_clock_p		8285	338
33	sample_clock_n		8385	338
34	vdd!		8485	338
35	gnd!		8585	338
36	interrupt		8685	338
37	res_n		8785	338
38	timestamp_clk		8885	338
39	hold		8985	338
40	sr_CK1		9085	338
41	sr_CK2		9185	338
42	sr_LOAD		9285	338
43	sr_SIN		9385	338
44	sr_RB		9485	338
45	sr_SOUT		9585	338
46	vdd!		9685	338
47	gnd!		9785	338
48	-	No needle required	9885	338
49	-	No needle required	9985	338
50	vssa!		10885	338
51	vssa!		10985	338
52	vdda!		11085	338
53	vdda!		11185	338
54	gnda!		11285	338
55	gnda!		11385	338
56	~~VPBias~~	No needle required	11485	338
57	~~VN~~	No needle required	11585	338
58	blpix		11685	338
59	~~VPLoad~~	No needle required	11785	338
60	gnda!		11885	338
61	vdda!		11985	338
62	Inj		12085	338
63	gnda!		12185	338
64	ThPix		12285	338
65	vminuspix		12385	338
66	gnda!		12485	338
67	vdda!		12585	338
68	ampout		12685	338
69	~~Qdac<0>~~	No needle required	12885	338
70	~~Qdac<1>~~	No needle required	12985	338
71	vssa!		13085	338
72	vdda!		13185	338
73	gnda!		13285	338
74	Vtemp<0>		13385	338
75	Vtemp<1>		13485	338
76	VCasc2!		13585	338
77	~~VNPMOS~~	No needle required	13685	338
78	vdda!		13785	338
79	gnda!		13885	338
80	Vtemp<2>		13985	338
81	Vtemp<3>		14085	338
82	~~VCasc~~	No needle required	14285	338
83	ThPMOS		14385	338
84	vssa!		14485	338
85	vdda!		14585	338
86	gnda!		14685	338
87	vssa!		14785	338
88	vdda!		14885	338
89	gnda!		14985	338
90	DigInj		15185	338
91	vdd!		15385	338
92	gnd!		15485	338
93	ring4		16585	128
94	ring3		16885	128
95	ring2		17185	128
96	ring1		17485	128
97	sub!		17985	128
98	sub!		18085	128
99	sub!		18185	128
100	sub!		18285	128
101	sample_clock_right		18273.5	555
102	spi_right_CSN		18273.5	655
103	spi_right_CLK		18273.5	755
104	spi_right_MOSI		18273.5	855
105	spi_right_MISO<0>		18273.5	955
106	spi_right_MISO<1>		18273.5	1055



Backup Test items (1/2)

- **List of chip test items for ALPIDE (also applicable to AstroPix_v3)**
  1. **Powering test:** power on/off
  2. **Vbb I-V test:** apply the reverse substrate bias from 0 V down to −6 V
  3. **DAC scan:** verify that each DAC is working by scanning through all its code words
  4. **Power on reset test:** check the functionality of power on reset
  5. **SEU check:** monitor the SEU counter and the flag bits on idle operation
  6. **Register test:** check all registers by writing and reading back to find stuck bit
  7. **FIFO test:** check all the generated memory blocks
  8. **Data port test:** verify its functionality to send quasi-static patterns in case of the readout test failure
  9. **Digital scan:** inject single hits directly into the in-pixel memories and read back
  10. **Fake hit rate**: measures the number of noisy pixels and faulty front-ends
  11. **Analog scan DP**: exercise the analog front-end and the full readout chain of ALPIDE
  12. **Threshold scan**: test all analog front-ends/pixels by using analog pulse injection
  13. ~~**High speed link check:** check its functionality~~ (N/A to AstroPix_v3)

      → **Daisy chain SPI interface:** test the interface is working (only to AstroPix_v3)



Backup Test items (2/2)

- **Expected elapsed test time per chip:**
  - CAVEAT: this is an assumption based on ALPIDE (ALICE ITS2)
    a. Elapsed time for test via probe card: ~190 sec
    b. Total elapsed test time per chip: ~~≈500 sec~~ → ~370 sec (edge inspection check dropped later)