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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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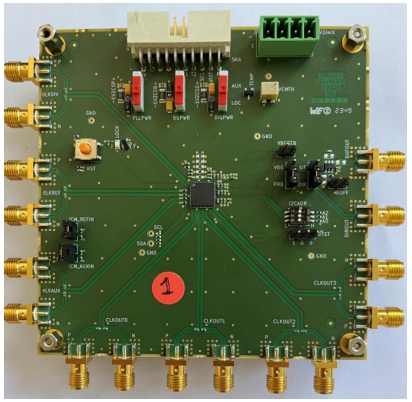
STATUS OF THE PROTOTYPES

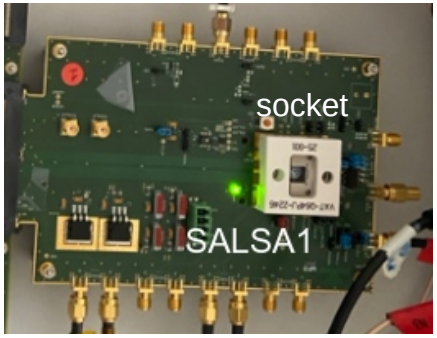
PRISMEv1 prototype (PLL test chip)

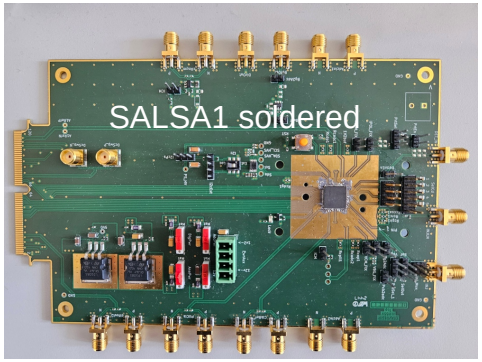
- Updates done on the PLL block: deterministic jitter noise, radiation hardness, lower internal frequency, inclusion of CDR for unified input interface, compatibility with lpGBT input frequency
- Test cards being cabled, should arrive end of this week



SALSA1 prototype

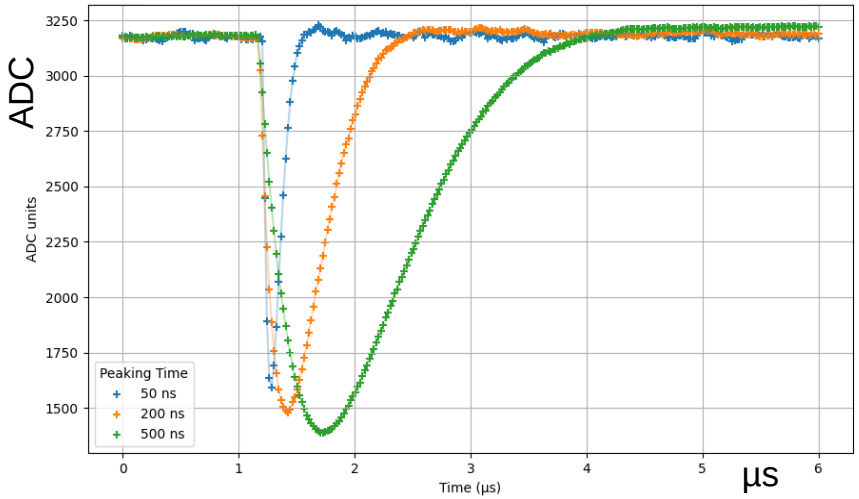
- New test-cards with SALSA1 soldered on them, instead of socket
- Systematic measurements ongoing on several ASICs
- Some results already available, cf next slides
- Studies on ADC performance started, Sao Paulo ADC working up to 55 MS/s, IRFU ADC up to 70 MS/s, further studies needed
- Still to be done: systematic studies with large input capacitance, large counting rates, saturation recovery, ADC performance and power consumption, tests at larger temperature, radiation tests, etc...



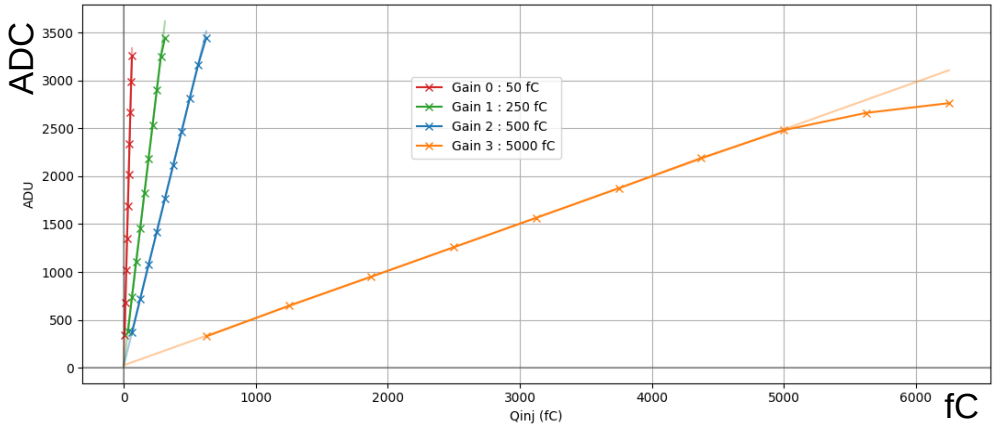


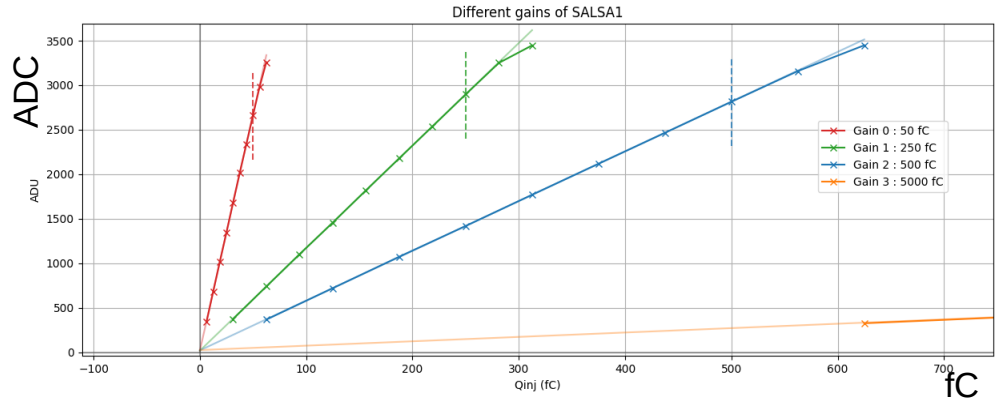
RESULTS ON SALSA1

Response with different peaking times

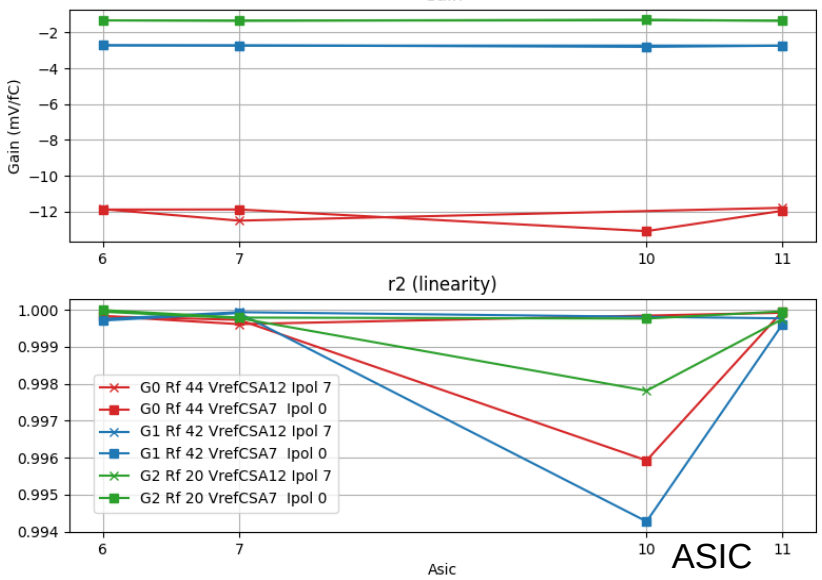


Response vs injected charges for different gains





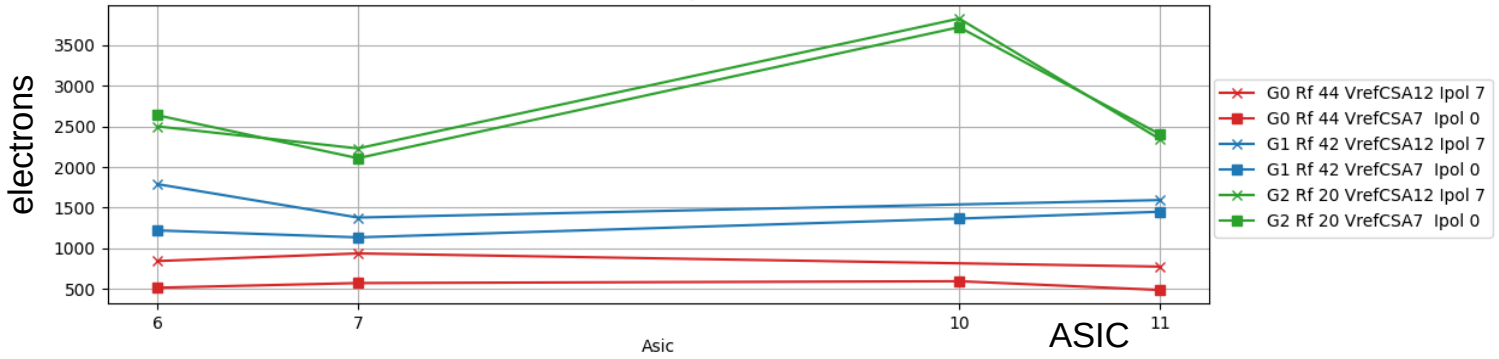
Gain and linearity vs ASIC number



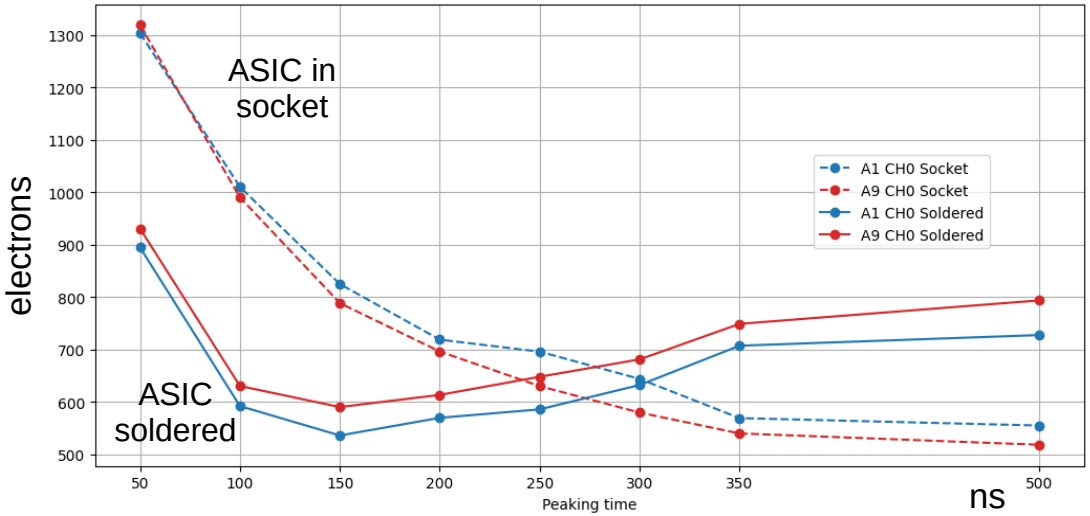
- Good linearity within nominal range for all gains
- 1 ASIC looks slightly worse than others

RESULTS ON SALSA1

Average noise vs ASIC for different gains (50-500 fC)



Average noise vs peaking times for 2 ASICs in socket or soldered



- Reproducible noise from one chip to the other, with an exception
- Noise decreases significantly at low peaking time when ASIC soldered instead of mounted in socket
- Larger noise at high peaking times to be understood (current leak ?)

CURRENT STATUS: SALSA2

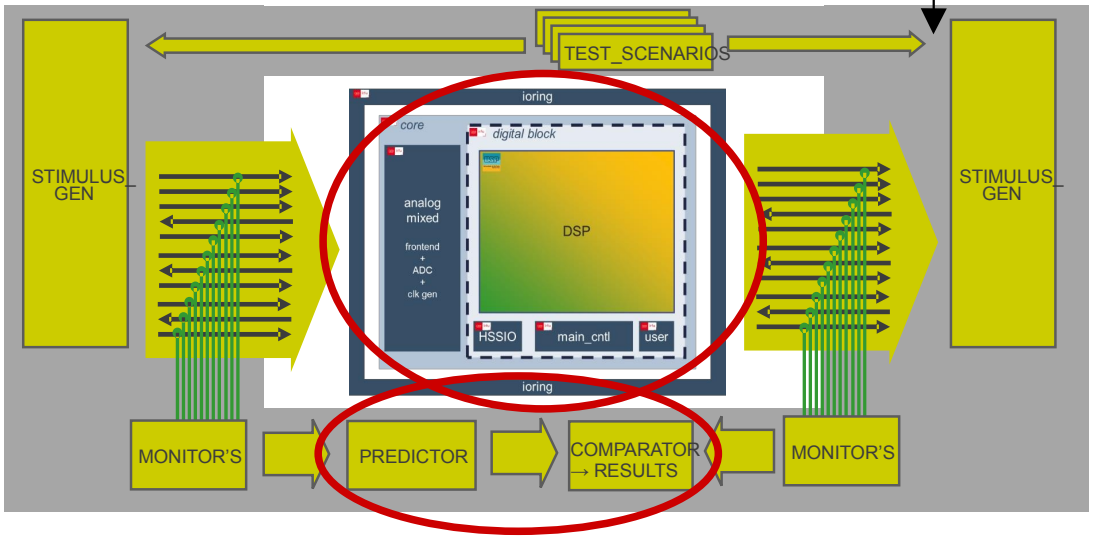
SALSA2 development status

- Work ongoing on HDL code of DSP modules, code of most modules completed, still some work on packetizer and multiplexer
- Integration of digital processing modules with other blocks started, first step to reach is integration of multiplexer into the general SALSA2 digital architecture
- Tests ongoing on synchronization and communication with rest of DAQ chain
- Floor plan under study
- UVM environment under development, 1st version of predictor DSP model done, to be adapted to low-level C language
- Packaging under study, contacts ongoing with packaging companies

Timeline

- Still a lot of works ahead:
  - code verification and validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen beginning of 2026
- Tests in 2026
- Distribution to users before end 26 or beginning 2027

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done
- Test card production → done
- Performance evaluation → ongoing

Generic R&D program for EIC project (new 65nm PLL block)

- Fully done, follow-up with PRISMEv1 new prototype (not financed by this program)

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming beginning of 2026
- Beginning of SALSA2 tests → 2nd semester 2026

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming December 2025
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

Very next steps

- SALSA1 tests → ongoing
- New PRISMEv1 chip → test-cards coming very soon
- SALSA2 development → in progress