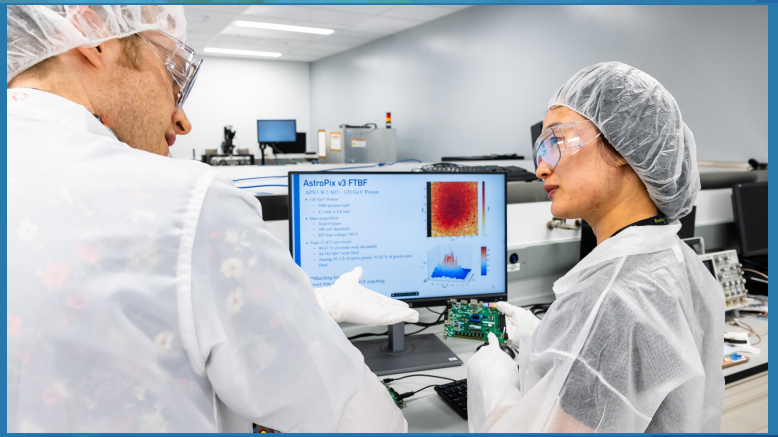
The ePIC Barrel Imaging Calorimeter

System Testing and Simulation



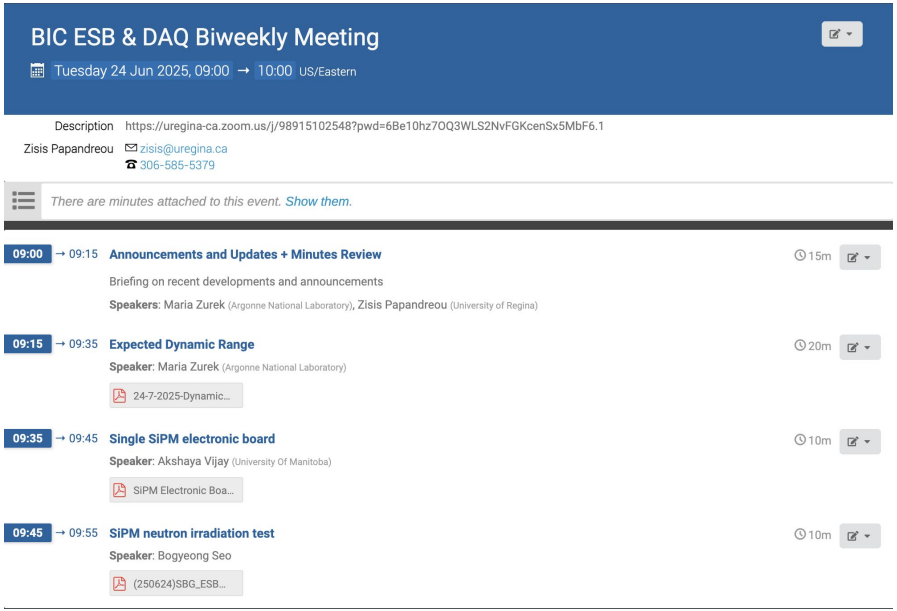
Maria Żurek for the System Testing and Simulation Team
Argonne National Laboratory

BIC General Meeting
July 24, 2025

System Testing

Joined System Testing and ESB Meetings: 8 AM CT https://indico.bnl.gov/category/606/

- June 24: ESB Meeting
- July 1: System Testing - KEK Beam Test - first results discussion



BIC ESB & DAQ Biweekly Meeting

Tuesday 24 Jun 2025, 09:00 → 10:00 US/Eastern

Description https://uregina-ca.zoom.us/j/98915102548?pwd=6Be10hz7OQ3WLS2NvFGKcenSx5MbF6.1

Zisis Papandreou zisis@uregina.ca 306-585-5379

There are minutes attached to this event. Show them.

09:00 → 09:15 **Announcements and Updates + Minutes Review** 15m

Briefing on recent developments and announcements

Speakers: Maria Zurek (Argonne National Laboratory), Zisis Papandreou (University of Regina)

09:15 → 09:35 **Expected Dynamic Range** 20m

Speaker: Maria Zurek (Argonne National Laboratory)

24-7-2025-Dynamic...

09:35 → 09:45 **Single SiPM electronic board** 10m

Speaker: Akshaya Vijay (University Of Manitoba)

SiPM Electronic Boa...

09:45 → 09:55 **SiPM neutron irradiation test** 10m

Speaker: Bogyeong Seo

(250624)SBG_ESB...

AstroPix Testing Front

Bobae Kim

697	System Demonstration	Apr 9, 2025	Mar 27, 2026	
700	Procure items needed for the setup in B102 to run the HGCROC Board	Apr 9, 2025	May 20, 2025	2 weeks
701	Test HGCROC with S14 SiPMs on SFIL: Make it work + Tune readout parameters for our SiPMs	May 21, 2025	July 1, 2025	15 days
702	REQD: Prototyping Box with new BabyBCAL SiPM Board that can connect to HGCROC readout and JLAB Coda	Jun 30, 2025	Jun 30, 2025	
704	**Milestone**: BabyBCAL with new SIPMs and HGCROC tested and benchmarked	Aug 26, 2025	Aug 26, 2025	
705	REQD: 9-chip board available (4-chip would be ok)	July 28, 2025	July 28, 2025	
706	Sync AstroPix multi-chip board with HGCROC readout	Jul 29, 2025	Aug 25, 2025	3 weeks
707	REQD: 3 9-chip boards available (4-chip would be ok)	Aug 25, 2025	Aug 25, 2025	
708	Sync AstroPix 9-chip boards with HGCROC readout	Aug 26, 2025	Sep 8, 2025	
709	**Milestone**: AstroPix 9-chip board can be read in sync with SciFi HGCROC readout	Sep 8, 2025	Sep 8, 2025	
710	Full electrical test of 3 AstroPix 9chip pcb read out by the ASTEP board: data transfer, calibration,noise, etc.	Sep 9, 2025	Oct 20, 2025	
711	**Milestone**: 3 AstroPix 9-chip boards can be read in sync with SciFi HGCROC readout	Oct 20, 2025	Oct 20, 2025	
712	Development of the Calibration Procedure for chips based on v4 single chip	Oct 21, 2025	Dec 1, 2025	

705 REQD: **9-chip board**

- 🚧 Noise/Injection scan
- Observed two issues: debugging is on-going

707 REQD: 3 9-chip board **(4-chip)**

- Observed the coincident event matched three layers!

708 Sync with HGCROC

- first trial for synchronization using single chip and GECCO board: debugging is on-going
- Adapt the FPGA firmware for the Cmod A7 board and generate the appropriate bitstream file: on-going

705 REQD: 9-chip board

Bobae Kim

✅ Initial functionality confirmed – power stable and DAQ communication OK.

🚧 Noise/Injection scan (10s for each pixel) with 9 chips on 9-chip PCB

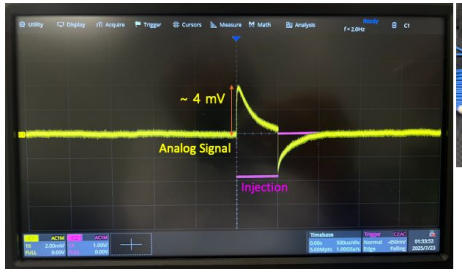
- Observed unexpected maximum buffer values — ideally, only 0/22 or 44 bytes were expected.
  - Max.buffer = 4,677 pixels/total 10,080 pixels @threshold=200mV
  - Max.buffer = 283 pixels/total 10,080 pixels @threshold=300mV
- Analog signal height is lower compared to single- or quad-chip setups

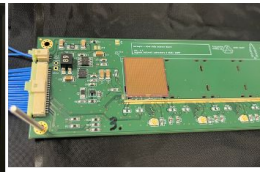
🚧 Analog signal check using injection with 1 chips on 9-chip PCB

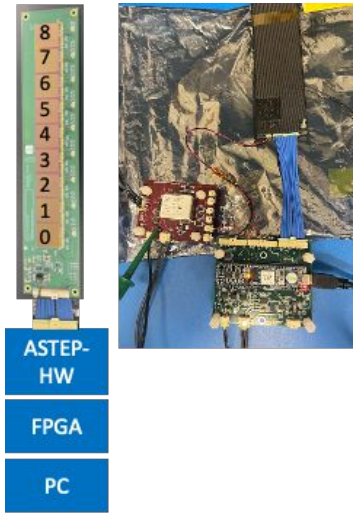
- Only ~4 mV analog signals were observed on a 9-chip PCB with a single mounted chip.
- The same chip showed ~200–300 mV signals when mounted on a single carrier board.

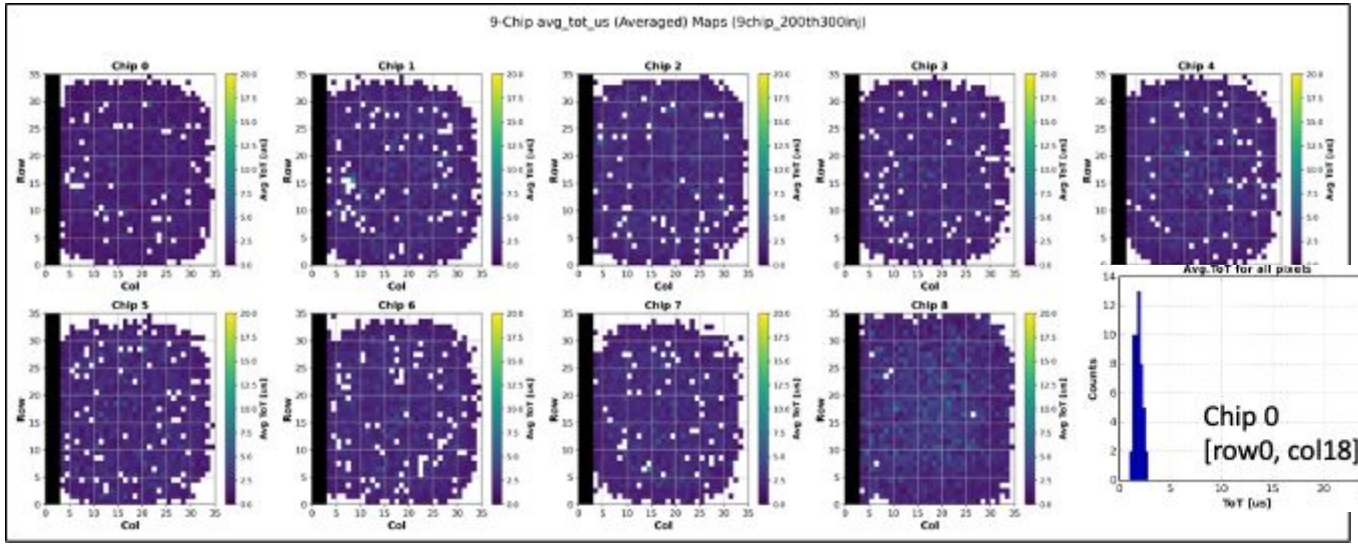
→ Based on these observations, this issue might be due to an undepleted sensor.

→ Improving the metal contact for HV GND under each chip on the 9-chip PCB could help establish a sufficient depletion region.









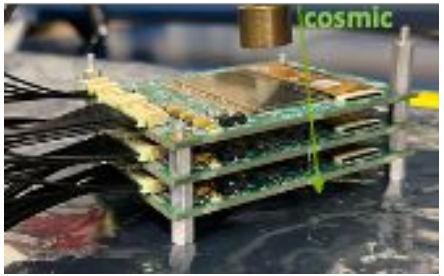
707 REQD: 3 9-chip board (4-chip)

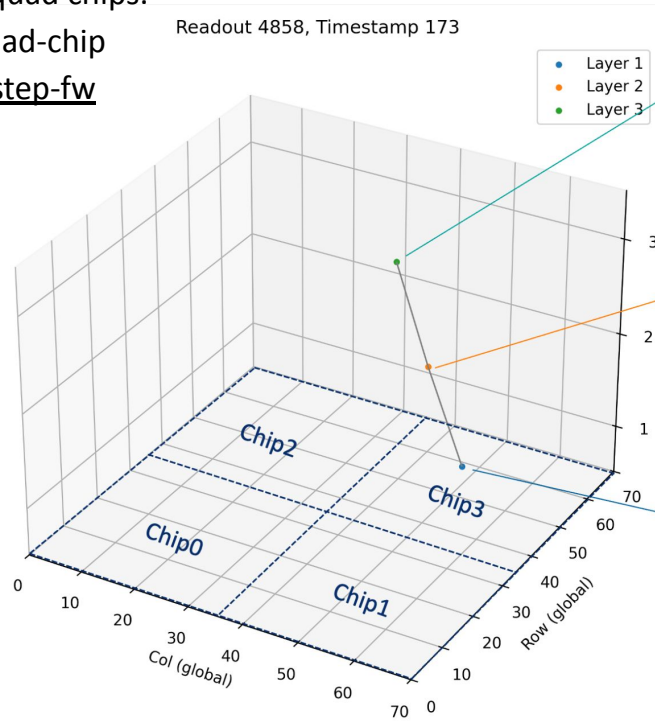
Bobae Kim

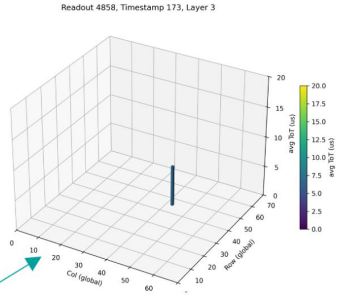
- To verify that the software and firmware under development operate properly
- Display of a representative event where all three layers share the same timestamp
- 1 TimeStamp = 400 ns

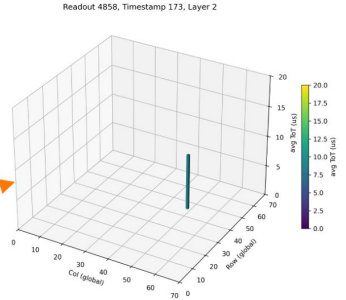
→ Validated the capability to read data from all quad chips.

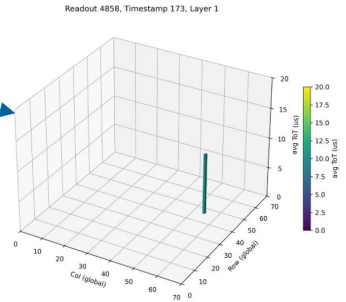
→ Successfully merged the feature branch for quad-chip testing into main: https://github.com/AstroPix/astep-fw









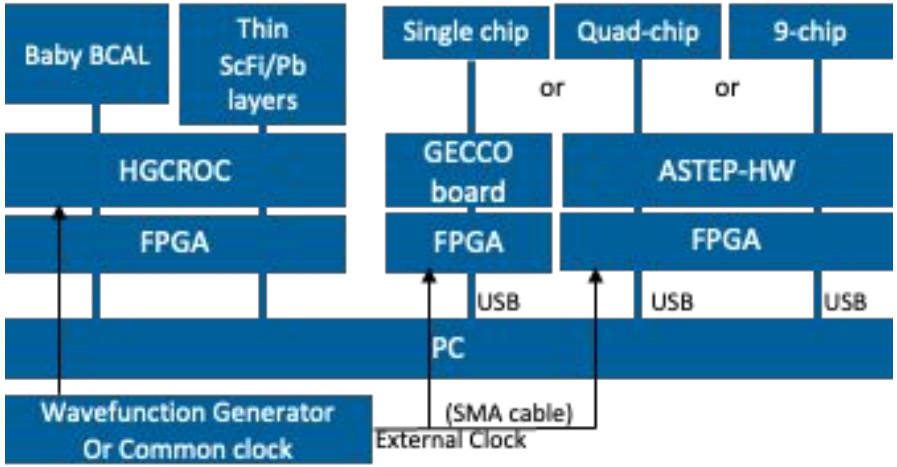


708 Sync with HGCROC (1)

Bobae Kim

Synchronization Plan between AstroPix DAQ and HGCROC for Pb/SciFi

🚧 Provide 40 MHz external clock to HGCROCs and AstroPix DAQ



AstroPix single chip+

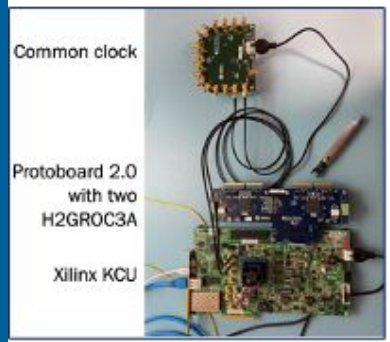
GECCO board + Nexys + ASTEP sw/fw

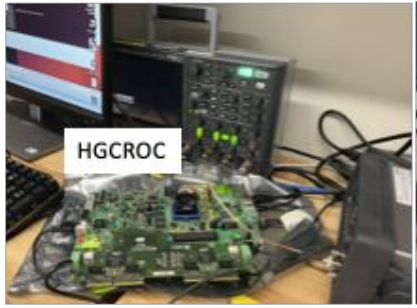
- LVDS external clock used
- 10MHz both AstroPix Timestamp and the FPGA timestamp external
- Bit file exists but needs debugging;

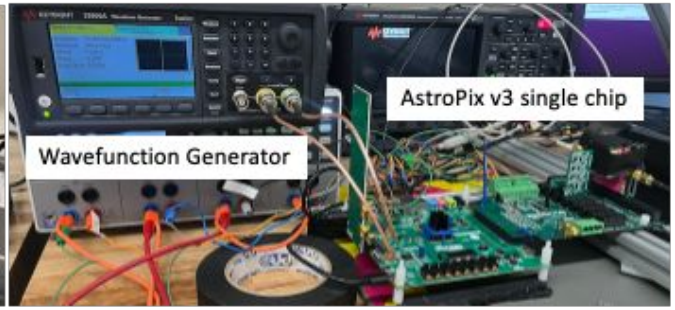
AstroPix quad-chip / 9-chip module +

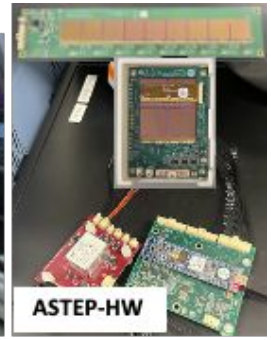
ASTEP HW board + CMOD + ASTEP sw/fw

- Single-ended clock required
- 40 MHz FPGA Timestamp and 10 MHz AstroPix Timestamp





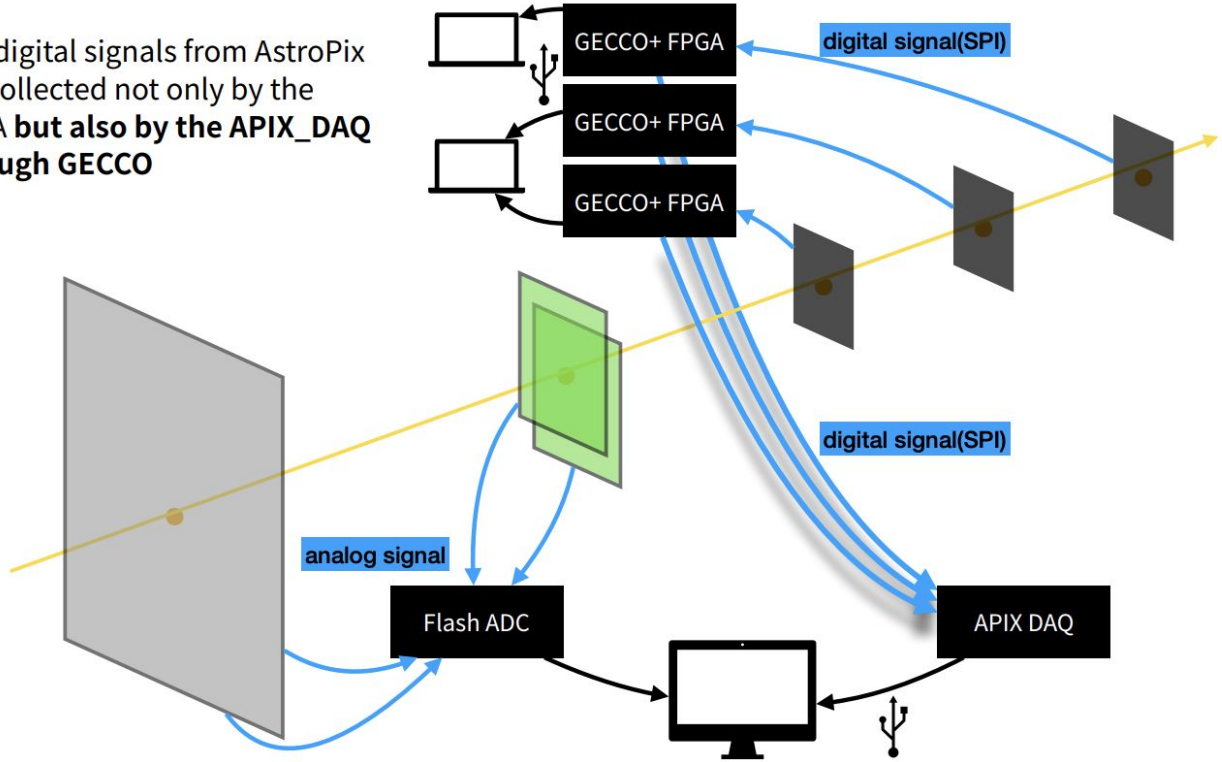




AstroPix3 Beam Test at KEK using Integrated DAQ System

Yoonha Hong

The digital signals from AstroPix are collected not only by the FPGA **but also by the APIX_DAQ through GECCO**



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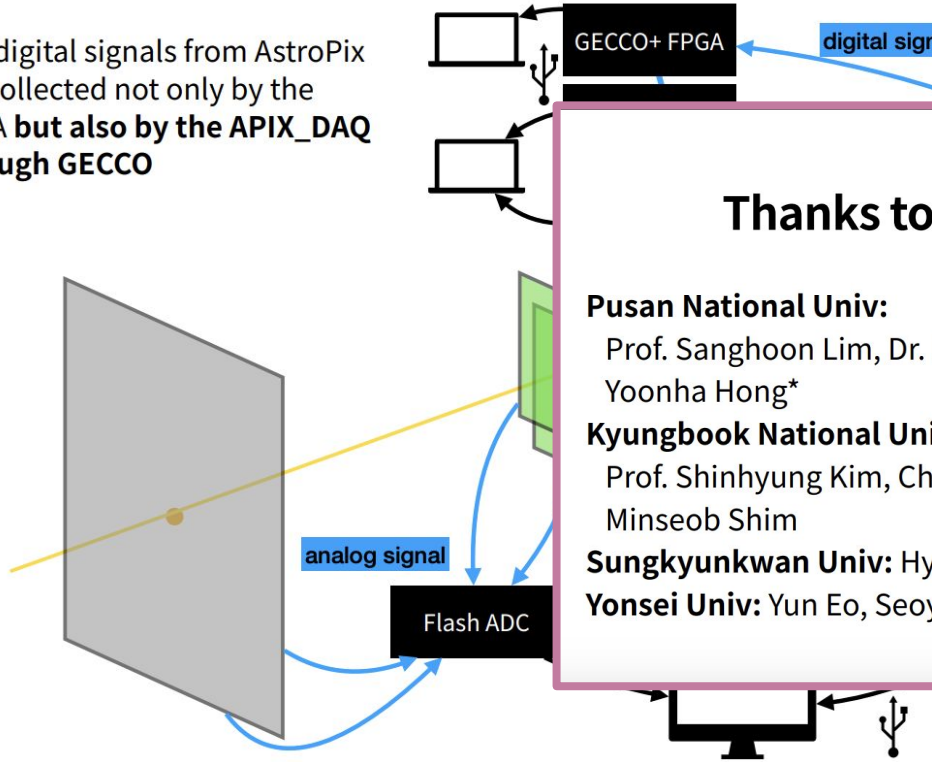


Thanks to Test beam participants!

Pusan National Univ:
Prof. Sanghoon Lim, Dr. Jeongsu Bok, Dr. Jongwon Lee, Jaehyeok Ryu, Yoonha Hong*

Kyungbook National Univ:
Prof. Shinhyung Kim, Changhui Lee, Bogyeong Seo, Wonjun Ko, Minseob Shim

Sungkyunkwan Univ: Hyungjun Lee

Yonsei Univ: Yun Eo, Seoyun Jang

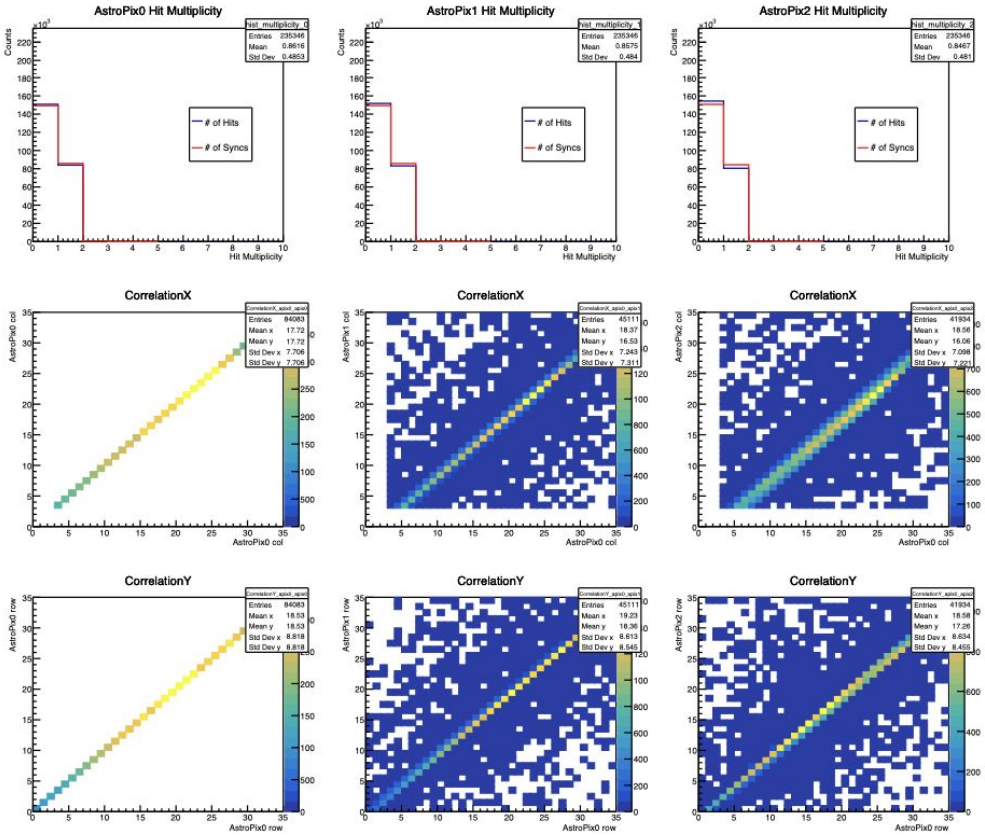
AstroPix3 Beam Test at KEK

Yoonha Hong

Position correlation

AstroPixs only, 4.5 GeV/c

- correlation drawn only if each chip has single hit

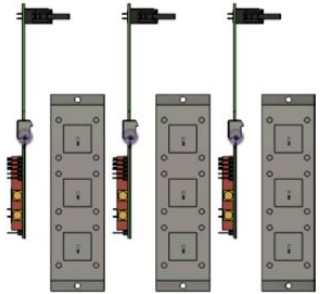


AstroPix3 Beam Test at KEK

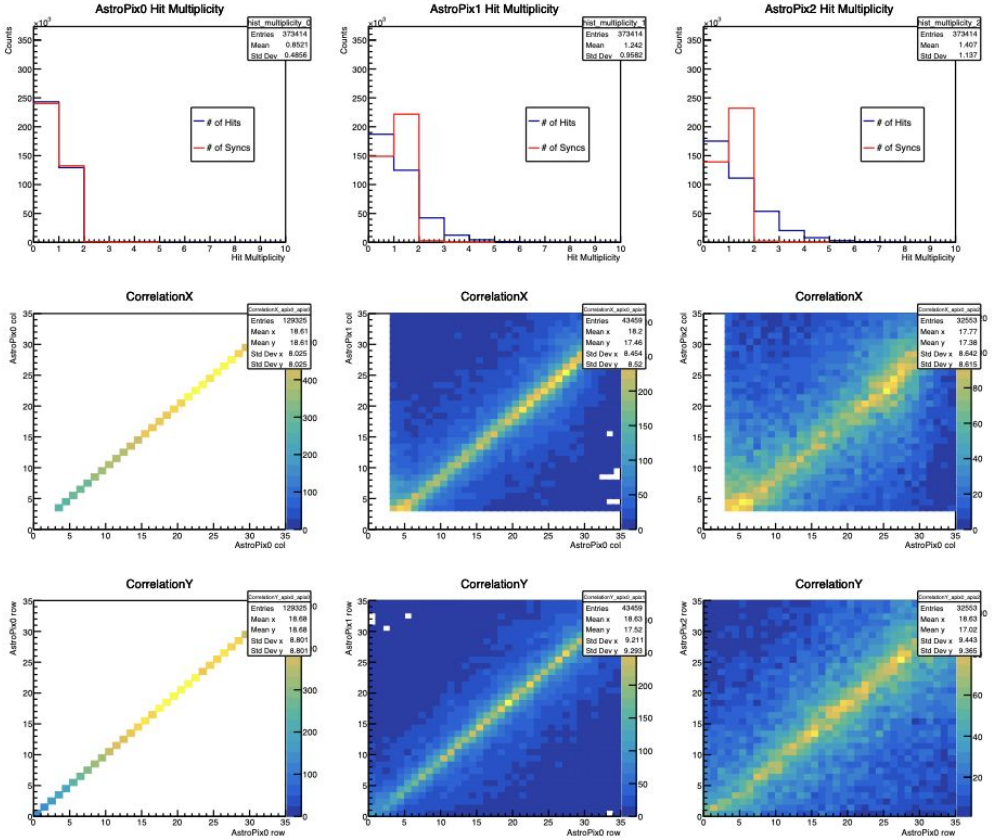
Yoonha Hong

Position correlation

AstroPixs+3 Calorimeter, 4.5 GeV/c



- correlation drawn only if each chip has single hit

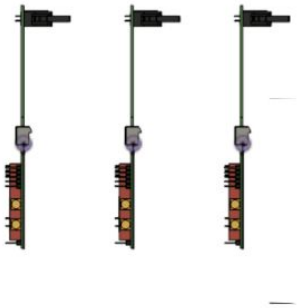


AstroPix3 Beam Test at KEK

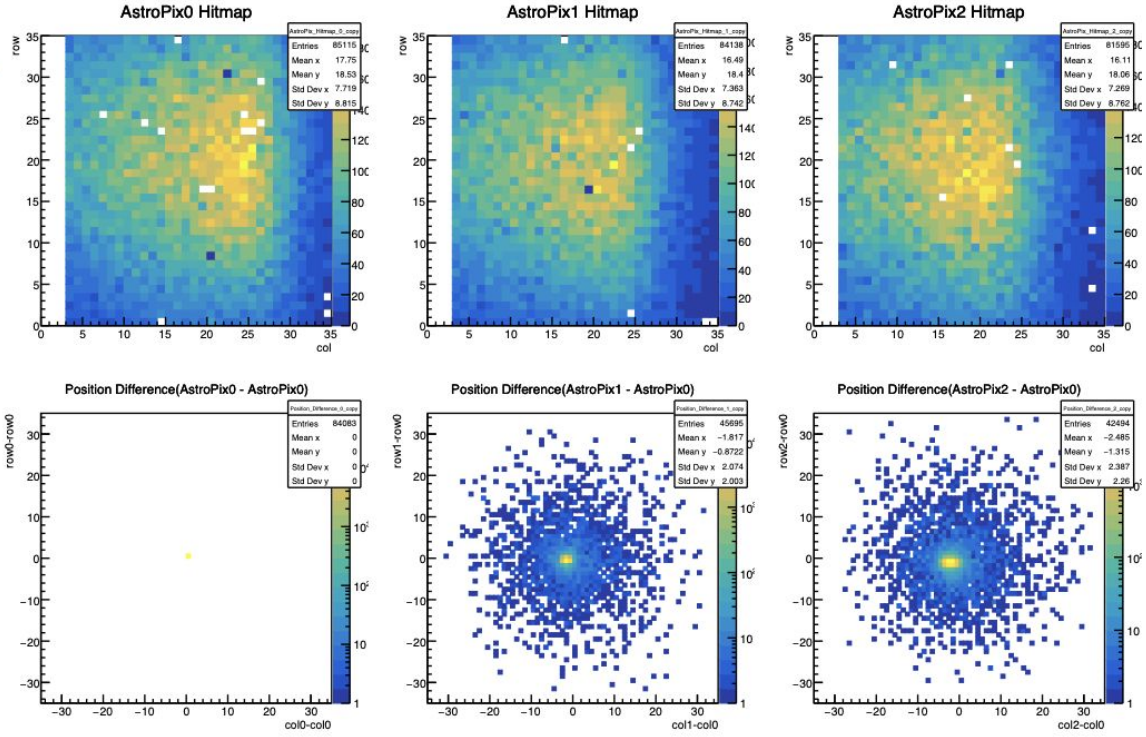
Yoonha Hong

Hitmaps

AstroPixs only, 4.5 GeV/c



- position difference drawn if chip0 has a single hit

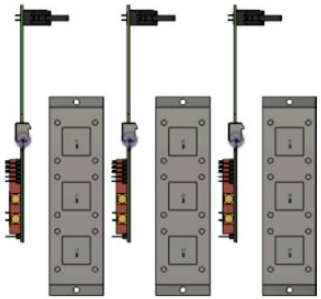


AstroPix3 Beam Test at KEK

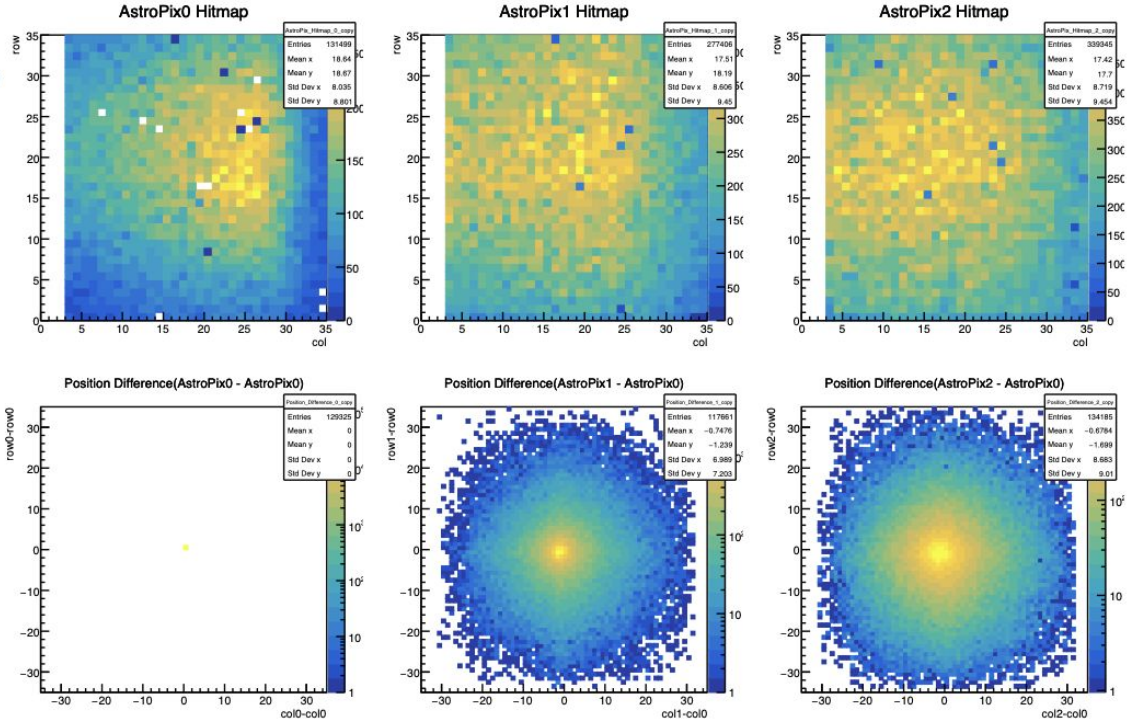
Yoonha Hong

Hitmaps with Calorimeter modules

AstroPixs+3 Calorimeter, 4.5 GeV/c



- position difference drawn if chip0 has a single hit



Simulations

Simulation Meetings, 2 PM CT https://indico.bnl.gov/category/551/

Akshaya Vijay - Topological Clustering for SciFi and AstroPix
https://indico.bnl.gov/event/29018/

Tomas Sosa Giraldo - e/pi Analysis

Jared Richards - Sampling fraction Simulations for Baby BCAL

https://indico.bnl.gov/event/28901/

Minho Kim - Signal Pulses building in eicRecon

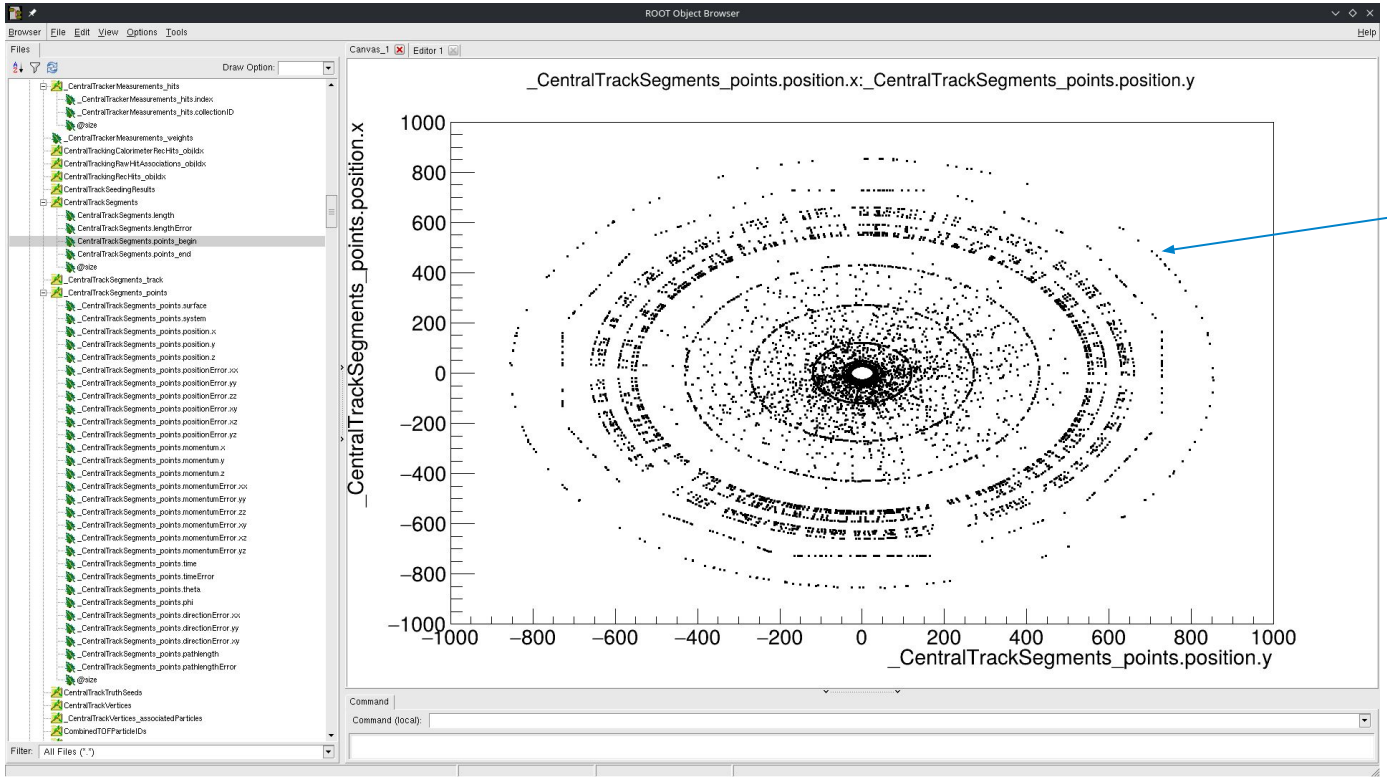
https://indico.bnl.gov/event/28815/

Wouter Deconinck - AstroPix in Tracking

https://indico.bnl.gov/event/28646/

Simulations

Wouter Deconinck



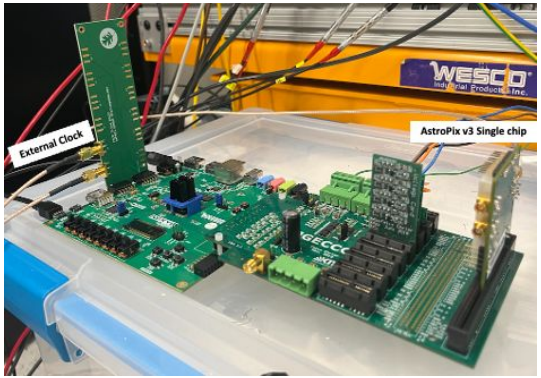
1st AstroPix Layer

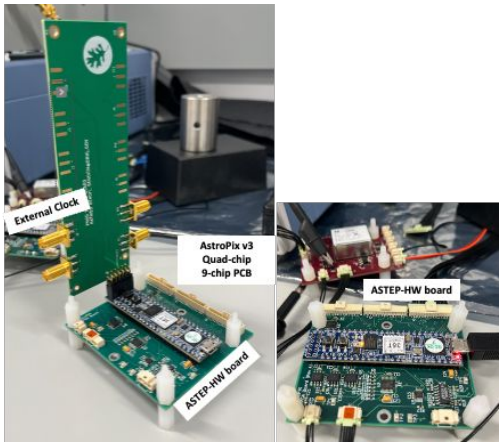
Thank you!

708 Sync with HGCROC (2)

Bobae Kim

(top) AstroPix single chip+ GECCO board + Nexys + ASTEP sw/fw
(bottom) AstroPix quad-chip / 9-chip module +ASTEP HW board + FPGA CMOD a7 + ASTEP sw/fw





The first trial for synchronization was conducted during Bobae's ORNL visit in **November 2024**, using:

- A 10 MHz **external clock**
- A **GECCO board** and a **v3 single chip**
- The AstroPix DAQ system

The clock signal was fed into:

- FPGA timestamp counter (32-bit: 0–2^{32})
- AstroPix timestamp (8-bit: 0–255)

1st main goals of this trial were to verify:

- The **FPGA timestamp increases linearly over time**
- The **AstroPix timestamp rolls over** correctly while the FPGA timestamp continues to count

ASTEP FW+SW status

- In the November 2024 trial, only the firmware (FW) was updated to support synchronization.: https://github.com/AstroPix/astep-fw/tree/beam_bobae_2411
- In the recent version of the astep firmware and software (main branch), the synchronization functionality is now also implemented on the software (SW) side.: https://github.com/AstroPix/astep-fw/tree/main
  - Current task: adapt the FPGA firmware for the Cmod A7 board and generate the appropriate bitstream file.