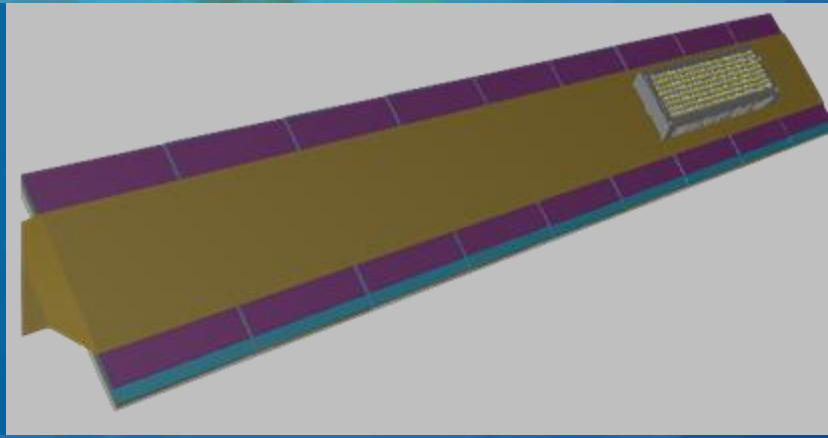
The ePIC Barrel Imaging Calorimeter

AstroPix Wafer QC, Modules and Staves



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Argonne National Laboratory

Sanghoon Lim
Pusan National University

BIC General Meeting
July 25, 2025

for the Wafers, Modules, and Stave Green Team

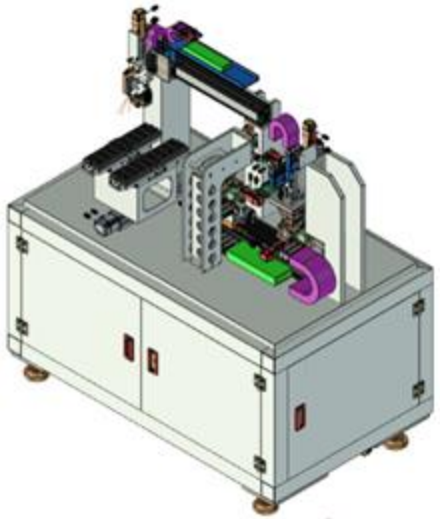
News

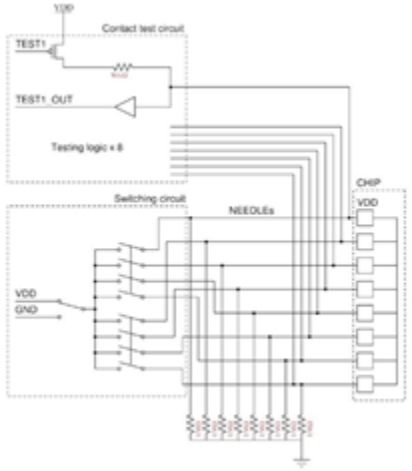
- Wafer QC and Module/Stave meetings
  - wafer QC meeting - 5 pm CT (Indico webpage)
  - Module/Stave meeting - 4:30 pm CT (Indico webpage)
  - Alternative weeks on **Mondays**

- Work in progress
  - AstroPix Chip QC test stands under production
    - AstroPix v3 chip probe card design ongoing
    - Dummy chip production discussion ongoing (2 cm x 2 cm, scaled v5)
  - Module and Stave support test articles delivered to Argonne
    - We have received two half stave railings and 20 module base plates
  - AstroLinx (Module PCB) design is uploaded to Box
    - AstroLinx internal review completed (Monday, Jul 21st)
  - Module carriers and handling tools design in progress
  - Wire-bonding procedure under discussion

Wafer/Chip Probing

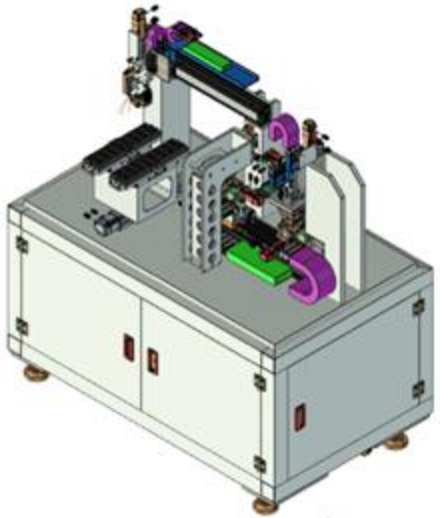
- Wafer/chip level testing prior to module assembly
- Quality Control Testing
  - IV measurements, power on, SEU check, Register check, FIFO test, analog and digital scan, threshold tuning, calibration checks
- Test stand production started
  - Delivery expected in September 2025
- **V3 probe card design ongoing**
  - Design work on probe contact confirmation



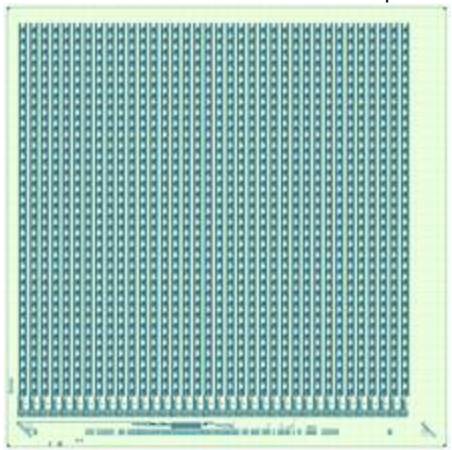


Wafer/Chip Probing

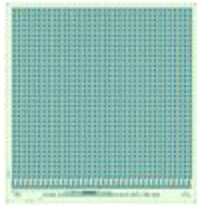
- Wafer/chip level testing prior to module assembly
- Quality Control Testing
  - IV measurements, power on, SEU check, Register check, FIFO test, analog and digital scan, threshold tuning, calibration checks
- Test stand production started
  - Delivery expected in September 2025
- **V3 probe card design ongoing**
  - Design work on probe contact confirmation
- **Scaled v5 dummy chip fabrication**
  - Scaled v5 chip to 2 cm x 2 cm size
  - Discussion with company to fabricate the dummy chips in progress



AstroPix v5 scaled to 2 cm x 2 cm footprint



AstroPix v5

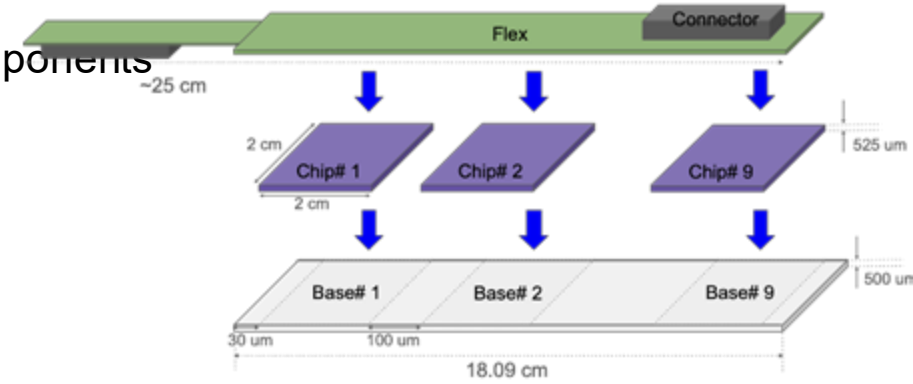


Modules

Design

- AstroPix Module comprises of 3 layers/components
  - **Base Plate (Aluminum)**
  - **Nine AstroPix Chips**
  - **Flex PCB**
- **Failsafe design** - easy to rework on Stave

AstroLinx: Module PCB



Not Scaled

1.7 mm - Connector

1.7 mm - AstroLinx

0.1 mm - Glue

0.525 mm - AstroPix

0.1 mm - Glue

1 mm - Module Baseplate

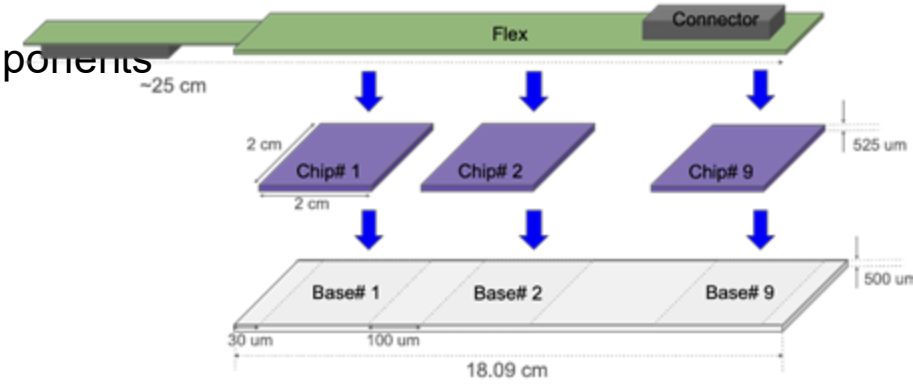
Iterated stackup with AstroLinx design and mechanics module baseplate/stave/tray design to fit within envelope

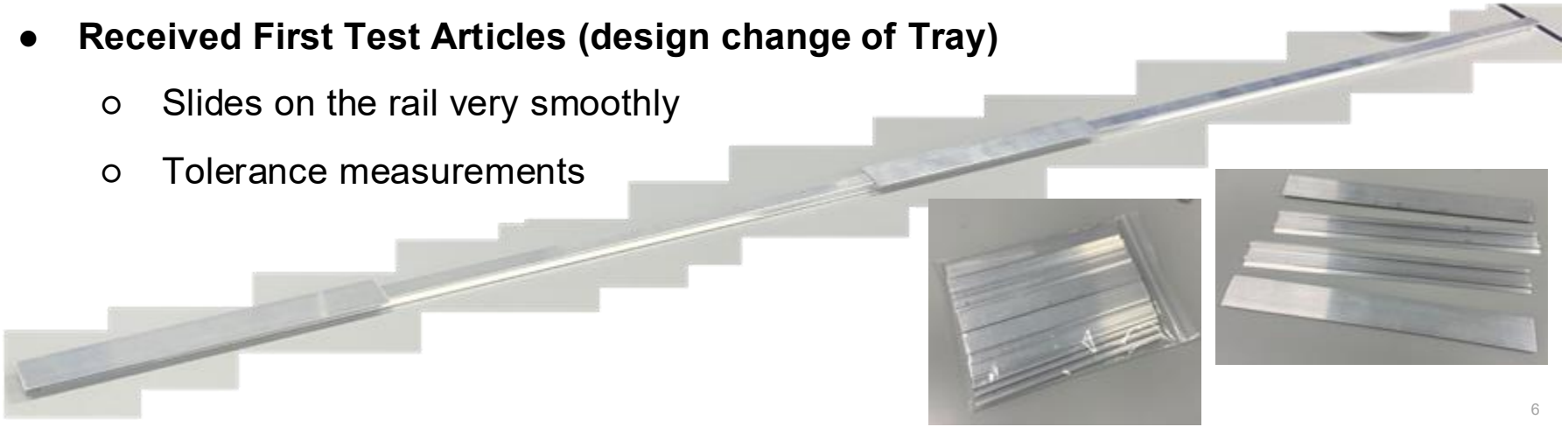
Modules

Design

- AstroPix Module comprises of 3 layers/components
  - **Base Plate (Aluminum)**
  - **Nine AstroPix Chips**
  - **Flex PCB**
- **Failsafe design** - easy to rework on Stave
- **Received First Test Articles (design change of Tray)**
  - Slides on the rail very smoothly
  - Tolerance measurements

AstroLinx: Module PCB

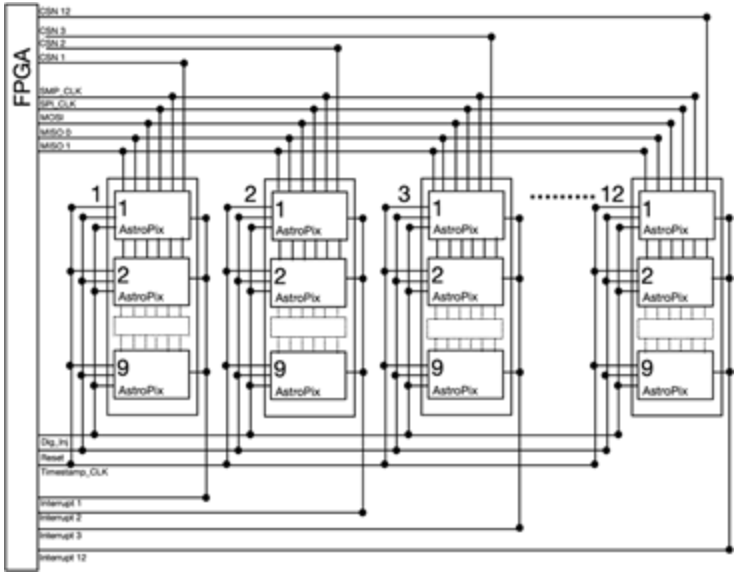


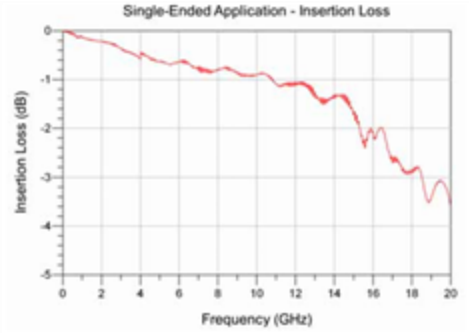


Modules

AstroLinx

- PCB design completed for AstroPix v3
- **Reveiw happened this Monday, Jul 21st**
- Few minor tweaks soon to be implemented
- Full Stave (12 boards) signal loss due to material is 3.32 dB. In addition, some signal loss due to connector (0.5 dB/connector).

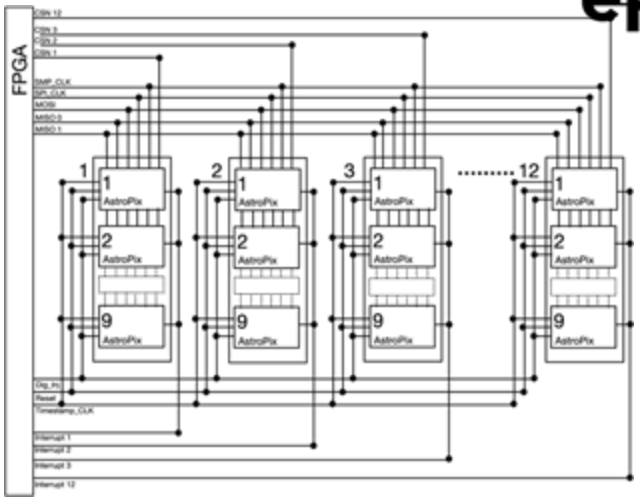


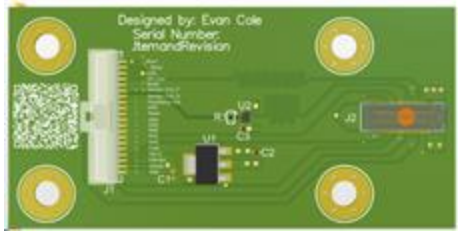


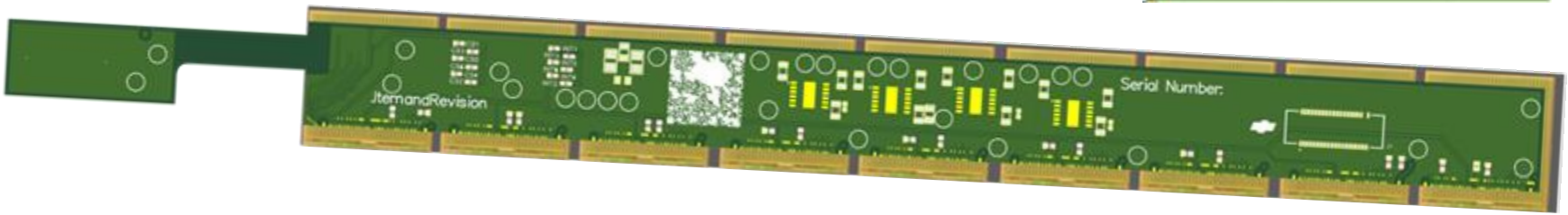
Modules

AstroLinx and Readout

- PCB design completed for AstroPix v3
- Reveiw happened this Monday, Jul 21st
- Few minor tweaks soon to be implemented
- **Next week - planned signoff on design and layout**
- QC test procedure is a next step
- **Design/Layout ready for bridge card to readout the Module using AStep FPGA boards**







Modules

9-chip PCB prototype

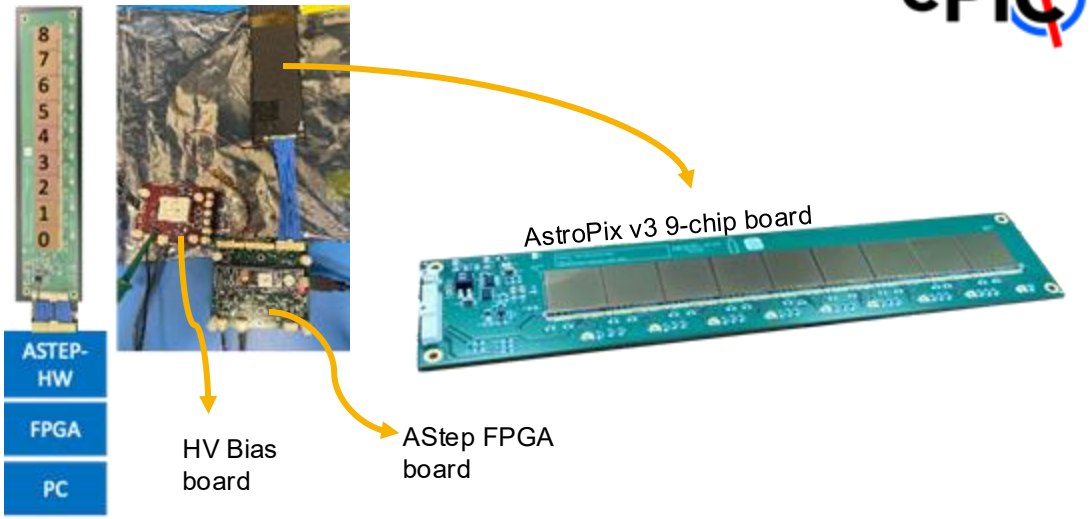
- Mockup the AstroLinx electronics
- Power distribution stability
- Daisy chain read-out
- Testing DAQ development

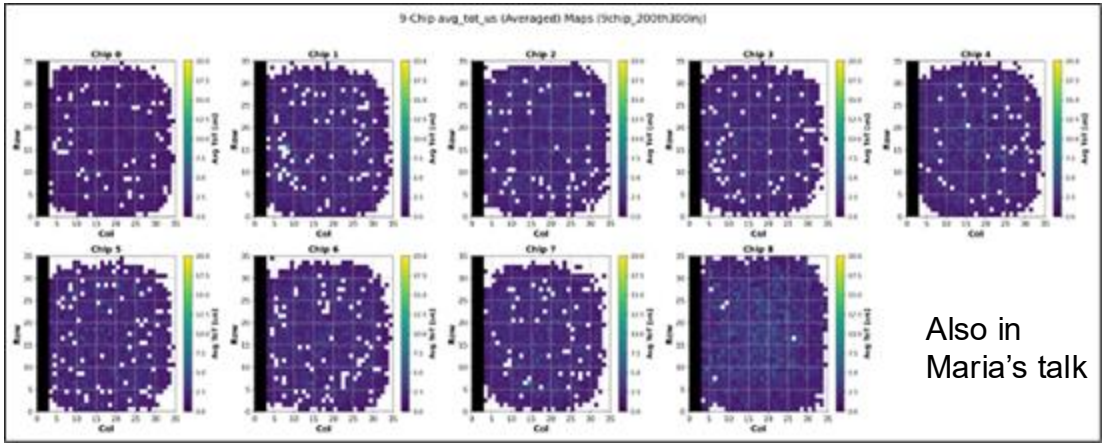
Testing with AStep card with CMOD FPGA

- Can test up to 3 modules with single card
- Started with Injection scan with individual pixel/chip
- **Fabrication of FPGA board submitted (Shared with NASA)**

Two more PCB ready for testing

- one with single chip (check Maria's talk)
- one ready with full assembly





Summary

- Biweekly follow up meetings for Astropix wafer QC and Module/Staves
- Test articles for Module/Stave support received
- Glass dummies available
- 9-chip PCB board tested with injected signal - show daisy chained functionality
- Chip level QC test system under production
- AstroLinx, a rigid+flex PCB design review completed
- Bridge card design is completed

Next

- Silicon dummies under discussion with company
- Probe card design for v3 chip
- Dummy hand assembly with test articles and glass dummies
- Tooling design finalization
- Source scan with 9-chip pcb board
- Submission of AstroLinx v3, discussion about QC

Thank you!

No BACKUP