Wafer probing in the UK?

James Glover
(with slides borrowed from Ivan Amos Calì)

EIC-UK WP1 (MAPS) meeting

Wed, 16th July 2025

The original plan

As assumed for the infrastructure bid:

- 2 UK sites were to help with the wafer probing.
  - Birmingham and Brunel.
- New probe stations would be needed for both sites (to handle high-speed data readout with vertical probe needles).
  - Some scope was considered to upgrade Birmingham's existing probe station, but funding base-line was to replace it.
- Assumption was to replicate the set-up being developed by the MIT-group @ CERN.

What has changed?

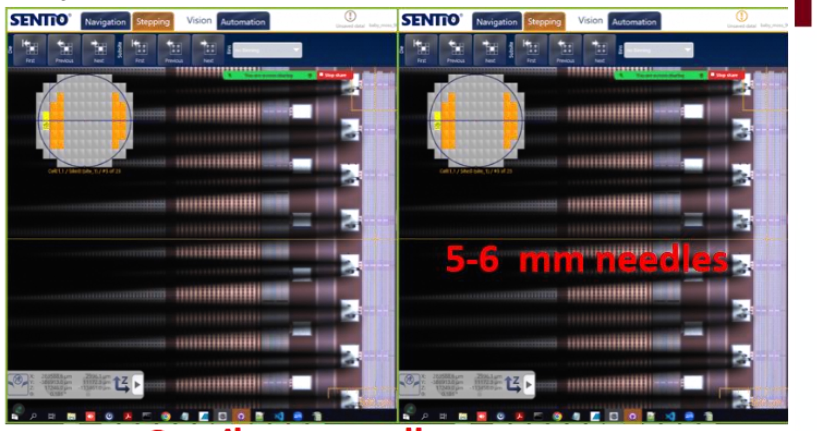
- The HS probes also increase the test time per segment.
- Fewer sites needed to do the wafer probing!

INTRODUCTION

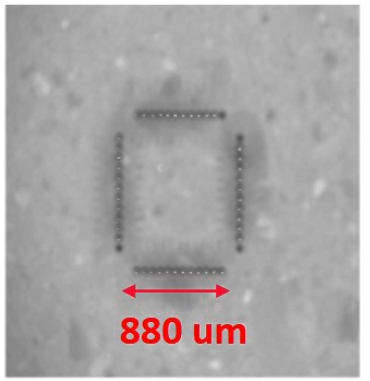
- MOSAIX and LAS will have 10.24 Gbps data links:
  - Standard cantilever probe cards **cannot** be used to **fully characterize** the sensor because limited at few hundred Mbps
  - **Vertical probing** allows operation at > 10 GHz. A prototype probe card was created to validate the technology

- SVT will need 300-400(?) wafers (considering yield and spares). Time needed for characterize 1 MOSAIX/LAS:
  - 12-24h if read out at low speed (160 Mbps)
  - 0.25-1 h if readout at high speed (10 Gbps)

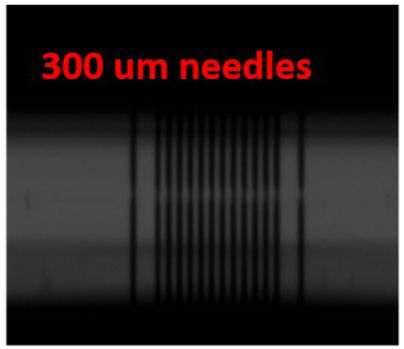
- Automatization and fast readout is critical to the project
- Collective effects studies require parallel readout of multiple MOSAIX



Cantilever needles



Chuck camera view of the needles

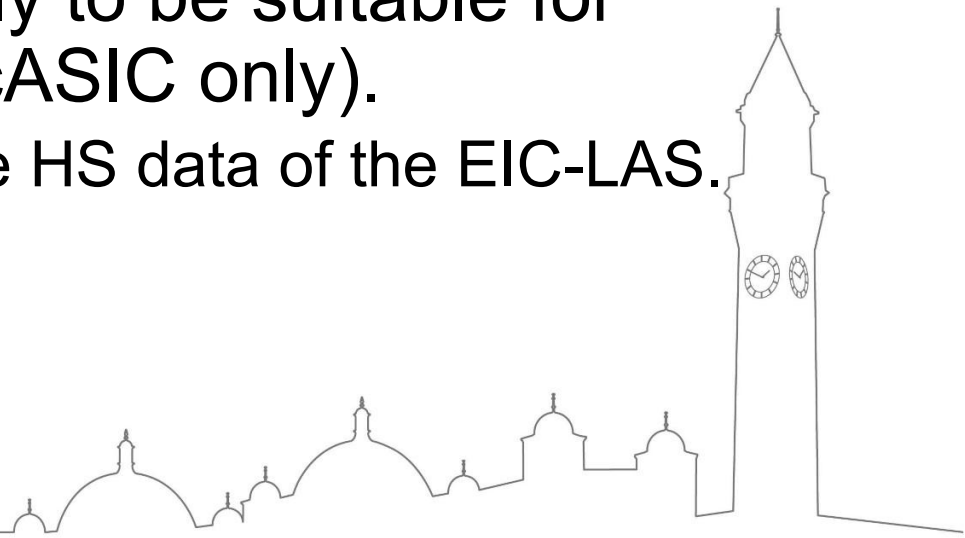


Side camera view of the needles

Cantilever needles

Where does that leave us?

- Do we relay need 2 extra probing site in the UK?
- Considerations need to made as to how many (vertical) probe stations the collaboration really needs!
  - Nevertheless, vertical probing expertise in the UK would be useful.
- Birmingham's current wafer probing is likely to be suitable for cantilever probing (so could probe the AncASIC only).
  - Vertical probe needles are only needed for the HS data of the EIC-LAS.



Probe station specifications

WAFER PROBING STATION at CERN

- MPI TS-3500 SE Automated test system
  - Installed at CERN in the DSF (Departmental Silicon Facility) lab

- Main specifications:
  - Designed to be able to load up to 300 mm (12”) wafers
    - **Micro-holes (200 um) chuck for thin wafers handling**
  - RF setup with possibility to test up to 110GHz and beyond
  - Several cameras installed: wide, **chuck, off-axis (vertical probing)**, VCE
    - Automatic Probe To Pad Alignment compensation
  - Extended probe card holder (see later)
  - Wafer wallet could be added for fully automatized process

- Goal:
  - **Commission test setup before being distributed to the institutes**
  - Test all the ITS3 ER2 wafers + (N) SVT ER2 wafers
  - Participate in the SVT production testing

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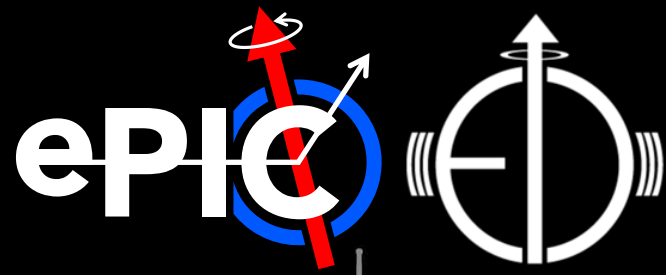
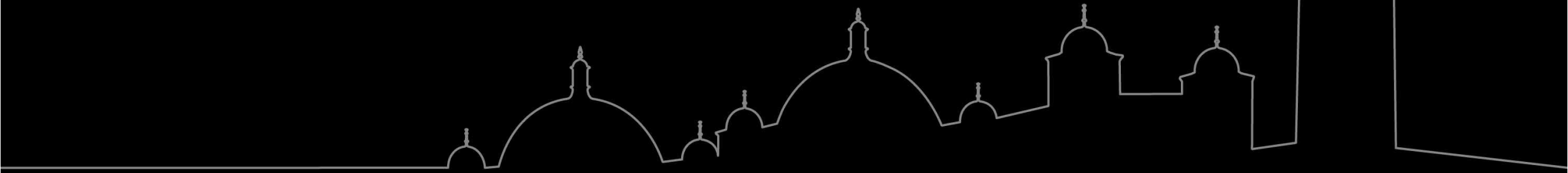


Thank you very much!

Any questions?



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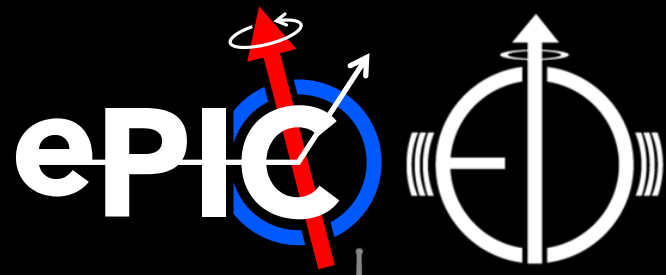
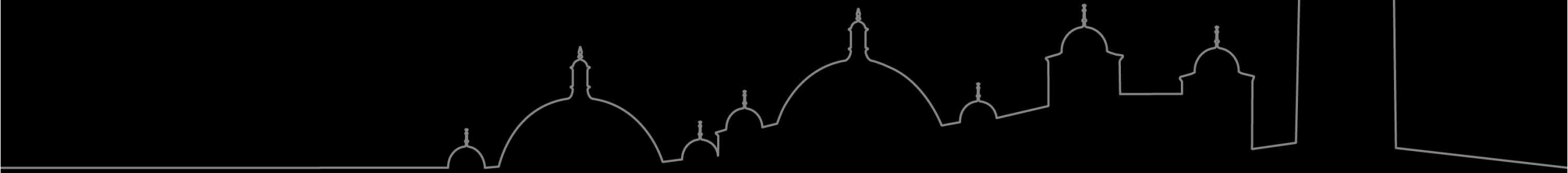


Additional (support) slides



Total probing time estimates

AncASIC (2×15 mm):

- $\mathcal{O}$(1,000) chips per 300 mm wafer.
- $\mathcal{O}$(5,000) chips needed (∴ ~5 wafers).
- Assume 10 min/chip, ~840 hrs of testing needed.
  - 35 days running 24/7 (@ 1 site).
  - ~6 mths running only working hours & days (@ 1 site).

EIC-LAS (20×160 mm):

- $\mathcal{O}$(10) chips per 300 mm wafer.
- $\mathcal{O}$(5,000) chips needed (∴ ~500 wafers).
- @ 1 hr/chip, 5,000 hrs of testing needed.
  - 209 days running 24/7 (@ 1 site).
  - ~2 yrs running only working hours & days (@ 1 site).

Approx sixes only. Assumes no parallel testing of chips and each chip only tested once.