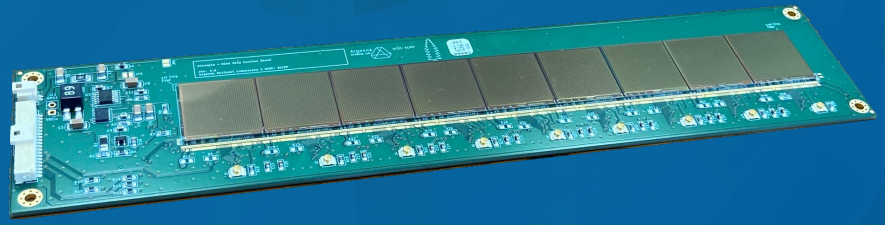
*Barrel Imaging Calorimeter Preliminary Design Review*

# System Testing: AstroPix Multichip Demonstrations



**Bobae Kim**
Argonne National Laboratory
on behalf of the BIC DSC

**BIC PDR**
September 17-18, 2025

# Charge

1. Is the progress and design maturity of the barrel electromagnetic calorimeter systems aligned with being baselined in June 2026 (>60% maturity is required)?
2. Are the technical performance requirements appropriately defined and complete for this stage of the project?
3. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
4. Are the current designs and plans for detector and electronics readout likely to achieve the performance requirements with a low risk of cost increases, schedule delays, and technical problems?
5. Are the calorimeter fabrication and assembly plans consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?
8. Have the recommendations from previous reviews been adequately addressed?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# System Testing Talks

**Together, these three talks demonstrate the validation path from module-level multichip tests, through system integration, to full system performance benchmarking.**

- **Multichip Design Demonstrations (B. Kim)**
  - 9-chip PCB test article in bench tests
  - AstroPix+Pb/SciFi system integration tests
- **AstroPix System Testing (J. Bok)**
  - AstroPix in beam tests
    - Performance validations of single chip / Three astroPix layers / AstroPix+Pb/SciFi
- **Pb/SciFi & System Testing (H. Klest)**
  - Pb/SciFi in beam tests and bench tests
    - Performance validations of Baby BCal and ANL Pb/SciFi Matrix

The testing program de-risks the design and defines system QC/QA for production; current validations confirm calorimeter energy performance and rate capability, and validate the simulation against data.

# Outline

## System Testing: AstroPix Multichip Demonstrations

- AstroPix Multichip Demonstration: 9-chip Module
  - Goal
  - Multichip Testing Setup: Setup & 9-chip Module
  - 9-chip Module Test Article: Performance Test Results (noise scan/Sr90 source test)
  - High-level Plan

- System Testing for Integration
  - Goal
  - Previous Test Result
  - Current Status & Plan
  - High-level Plan


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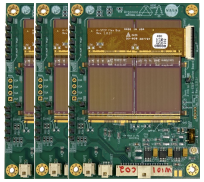
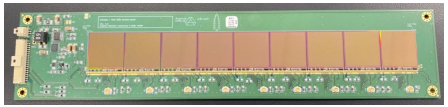
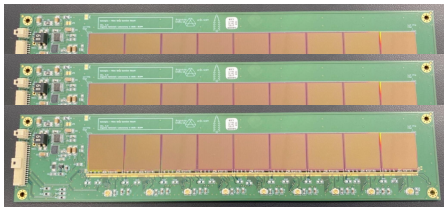
# AstroPix Multichip Demonstrations:
# 9-chip Module Test Article

# Goals of AstroPix Multichip Demonstration

**AstroPix v3**





- Basic device validation
  - Power stable and DAQ communication
- Performance validation
  - Noise scan
    - Active pixel yield
  - Source test with Sr-90
    - Hit Maps and ToT distributions
      → Consistent with v3 single-chip performance
    - Hit rates per chip
      → Compared with estimated one and current setup limits

| Configuration of AstroPix v3 | #.Chip | Status | Results |
|---|---|---|---|
| Single chip | 1x1 | ✅ | AstroPix talks (R.Caputo, S.Lim, J.Bok) |
| Quad chip | 2x2 | ✅ | backup slide p.19-21 |
| Three layers of Quad chips | 3x(2x2) | ✅ | backup slide p.22 |
| 9-chip Module (First test article) | 1x9 | ✅ | |
| Three layers of 9-chip Modules | 3x(1x9) | On-going | |

# Multichip Testing Setup

## 9-chip Module + AstroPix DAQ

### 9-chip Module Test Article

- PCB design based on single-chip/quad-chip carrier boards
- Mockup of the AstroLinx electronics
- Readout: **Daisy-chained 9 AstroPix chips** via SPI

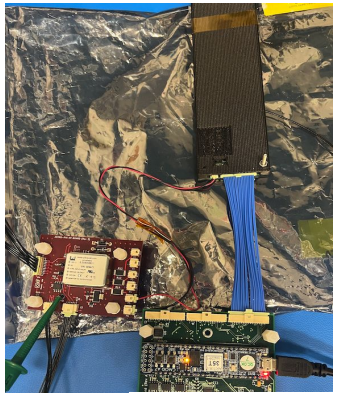
### AstroPix DAQ: A-STEP HW board + CMOD FPGA

- Developed for NASA A-STEP sounding rocket payloads (ComPair-2 prototype), now also used for current performance evaluations
- Supports up to three layers with quad-chip/9-chip modules
- Validated operation of a three-layer quad-chip configuration (up to 12 chips) by cosmic-ray tests

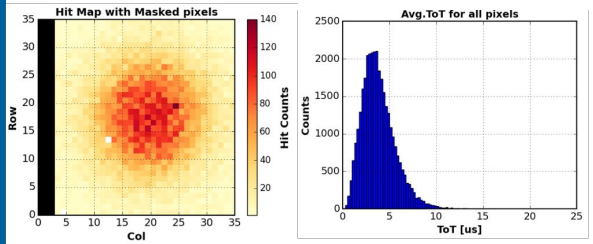

ASTEP -HW

FPGA

PC

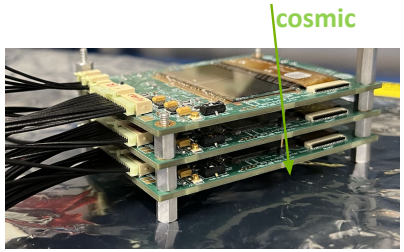


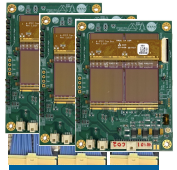
Reference: v3 single-chip Sr-90 test results







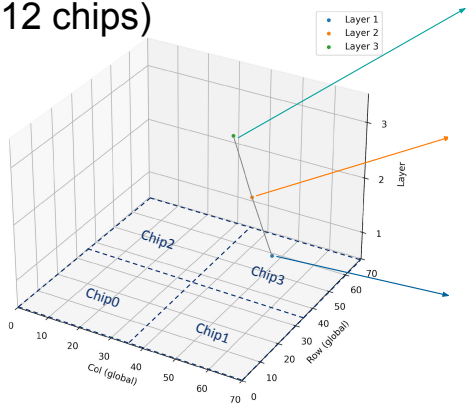


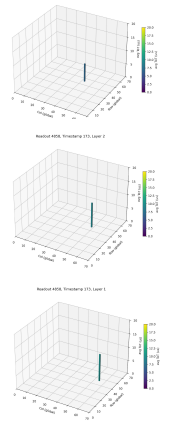



ASTEP-HW

FPGA

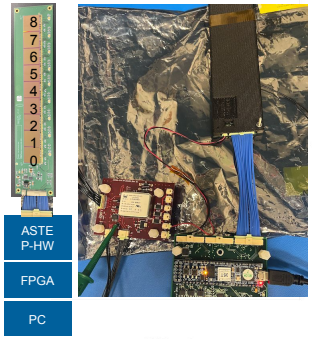
PC



# 9-chip Module: Noise Scan Results

- First three columns disabled during the performance test due to a different comparator.
- Pixels with noise rate ≥ 1 Hz were masked, and 99% active pixel yield for all chips (except chip 8: 91.9%)







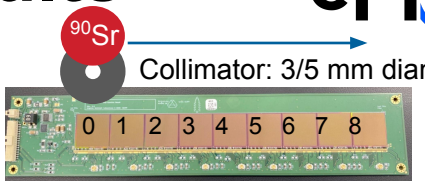
| Chip # | Disabled Pixels | Active Pixel |
|---|---|---|
| 0 | 4 | 99.6% |
| 1 | 1 | 99.9% |
| 2 | 4 | 99.6% |
| 3 | 10 | 99.1% |
| 4 | 5 | 99.6% |
| 5 | 4 | 99.6% |
| 6 | 4 | 99.6% |
| 7 | 5 | 99.6% |
| 8 | 91 | 91.9% |

→ **Achieved 99% active pixel yield** in the current test article (except the last noisy chip)

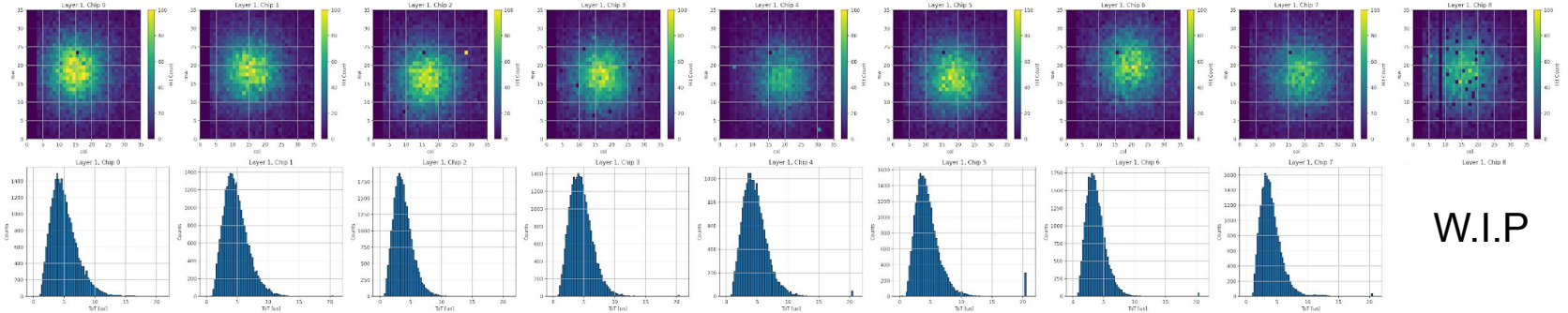
→ **Pre-production will follow the full production strategy: only chips with >99% good pixels accepted**

# 9-chip Module: Sr-90 Source Test Results

- 10 uCi Sr-90 Source moved to the next chip every 1 minute by manual placement
- Results consistent with v3 single-chip performance, confirming proper operation

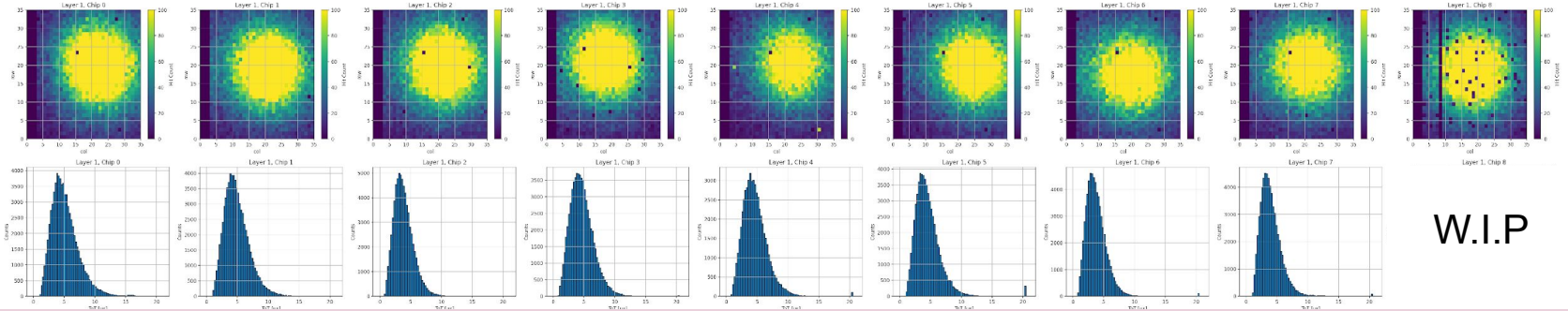



- 3-mm-diameter collimator



W.I.P

- 5-mm-diameter collimator

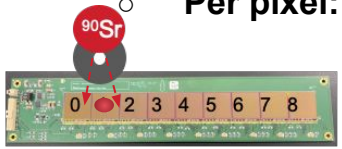


W.I.P

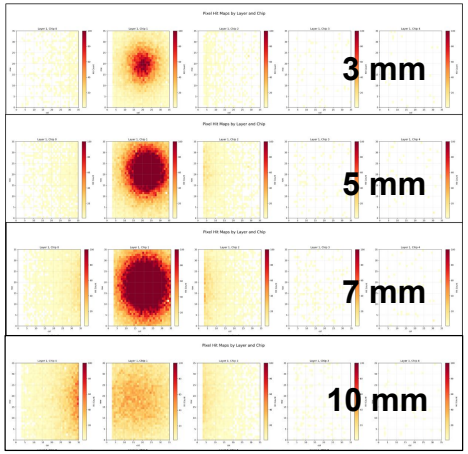
→ **The 9-chip module test article works well as intended with the current setup (powering, Daisy-chained readout)**

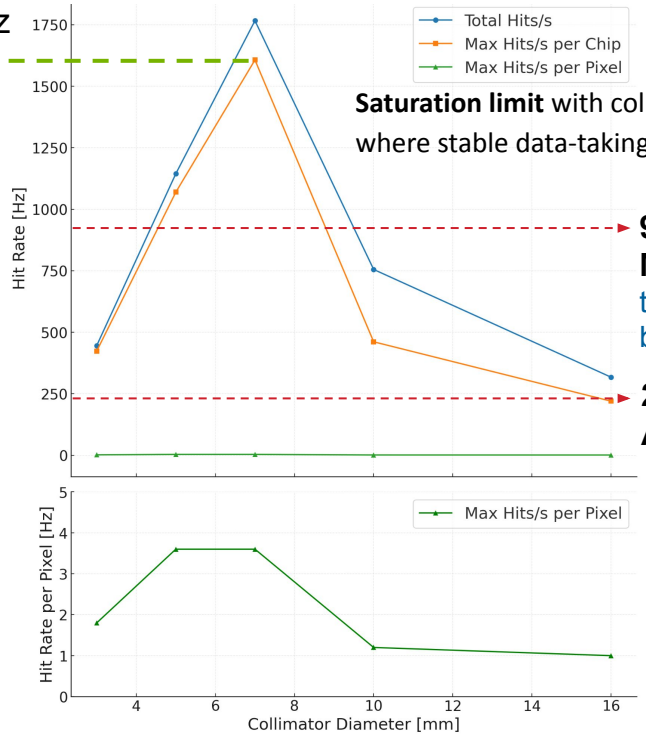
# 9-chip Module: Data Rate Results

- Goal: Validate the capability to read out data from the 9-chip module with the current setup
- Maximum hit rate with the current setup:
  - **Per 9 chips:** 1,766.5 Hz
  - **Per chip:** 1,606.9 Hz
  - **Per pixel:** 3.6 Hz

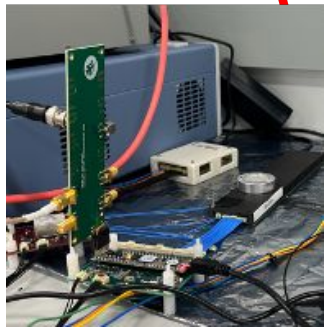



Collimator: 3/5/7/10/16 mm diameters




**Saturation limit** with collimators > 7 mm, where stable data-taking is no longer possible.



**924.8 Hz per chip**:
**Max**. expected data rates for imaging layers, taking into account DIS, electron, and proton beam backgrounds

**224.5 Hz per chip**:
**Avg**. expected data rates for imaging layers,

3.6 Hz **per pixel**
→ v3 design limitation
⇒ Improved in v4 sensor design

→ **The first per-chip measurement on the 9-chip module**, under the current setup, **meets imaging-layer data-rate.**
→ **Operation in realistic beam conditions is promising:** 924.8 Hz per chip is **expected on ~2–3 chips.**

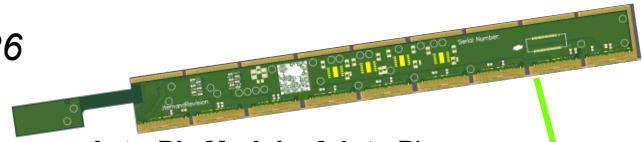
# High-level Plan Toward Final Design

## AstroPix Imaging Layer

**AstroPix 9-chip module test article** operates as intended and meets imaging-layer data-rate requirements.

**AstroPix 9-chip Module Testing:**

- Six AstroPix v3 9-chip modules built for testing - *FY26 Q2*
- Repeat testing with AstroPix v5 after fabrication is complete. - *FY26*



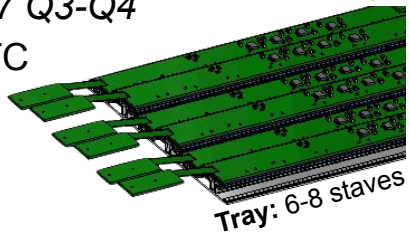
**AstroPix Module: 9** AstroPix sensors
- A **stave** consists of **12 modules.**

**AstroPix Stave Testing:**

- Half-stave testing with AstroPix ETC - *FY26 Q4*

**AstroPix Tray Testing:**

- Test Box design included in preproduction (planned to be also the shipment carrier) - *FY26 Q4*
- Full electrical QC and source calibration with ETC (for first v5 and v6 tray) - *FY27 Q3-Q4*
  - Verification of connection and communication between all modules and ETC
  - Electrical Stress Test
  - Synchronization and system timing validation
  - Energy calibration
- These results will inform the full tray QC procedures performed at the assembly sides, as well as reception and installation procedures at BNL



**Tray:** 6-8 staves

# System Testing for Integration

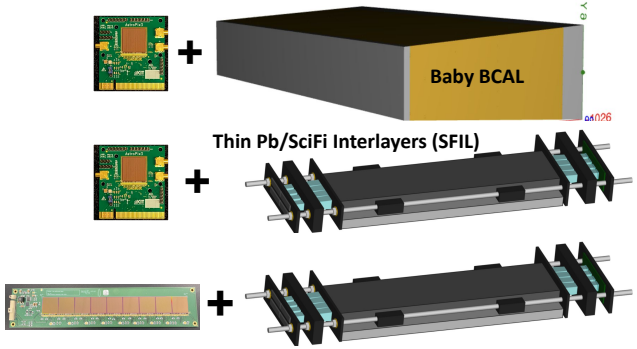
# System Testing for Integration

**Goal:** Establish **procedures** and **experimental setup** for **system-level performance validation and QC** for integrated AstroPix + Pb/SciFi test articles. Integrated tests requested in the comments from DAC reviews.

- To perform integrated system tests, we need **synchronization.**
  - A **common time base** is essential for **multi-detector event building**.
  - Bench pre-validation de-risks the EIC-wide **39.4 MHz common-clock** scheme
- How to synchronize at the system level (ultimate goal)
  - Distribute a **common external clock** to ASTEP/ETC and HGCROC/CALOROC
    - Synchronized event building by comparing FPGA timestamp differences across DAQs.

**Validated system-integration options:**

AstroPix v3 + Pb/SciFi calorimeter

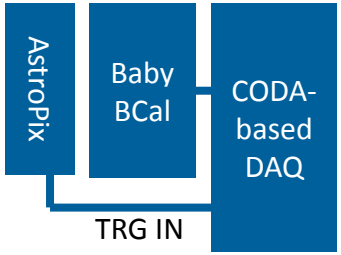


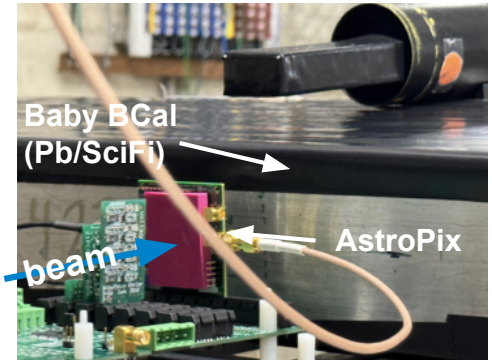

| How to integrate/**sync**. | AstroPix DAQ | Pb/SciFi DAQ | Status |
|---|---|---|---|
| Analog signal of AstroPix as TriggerIN | Single chip+ GECCO+Nexys | Jlab CODA-based DAQ | ✅ |
| MISO signal of AstroPix as TriggerIN | Single chip+ GECCO+Nexys | Jlab CODA-based DAQ | ✅ |
| External clock for FPGA TimeStamp | 9-chip Module+ ASTEP+CMOD a7 | HGCROC | On-going |

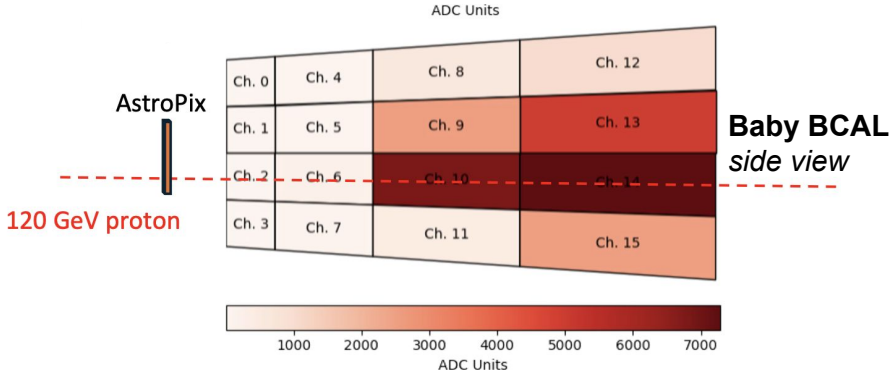
# System Integration: First Test Results

## AstroPix+BabyBCAL in Beam test (June 2024)

- Baby BCAL triggered by analog signal from one pixel of AstroPix



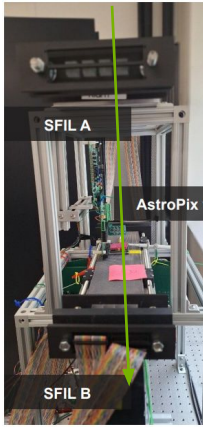



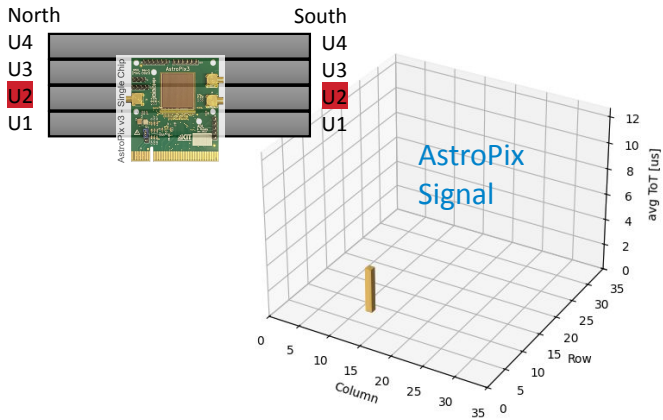



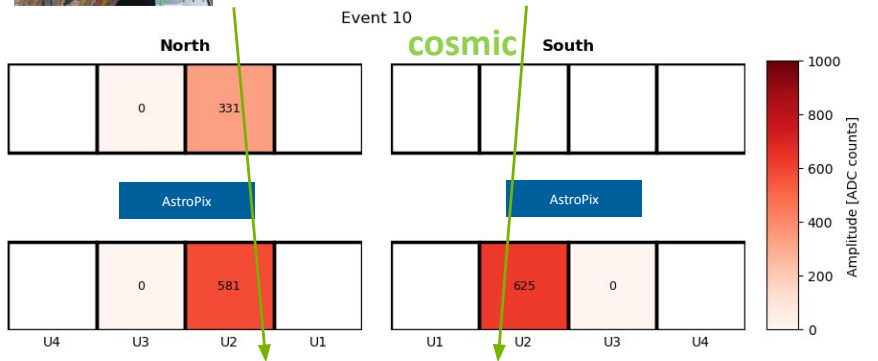

120 GeV proton event display from the integrated system

## AstroPix+SFILs in Bench test (April 2025)

- LVDS MISO signals that generated from AstroPix used as trigger IN for SFIL's DAQ



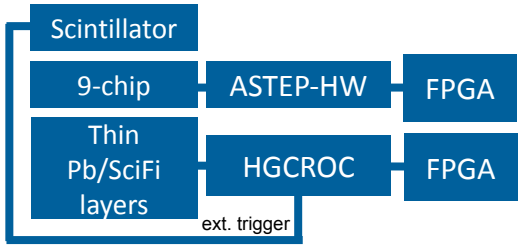



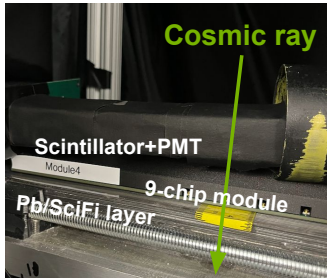



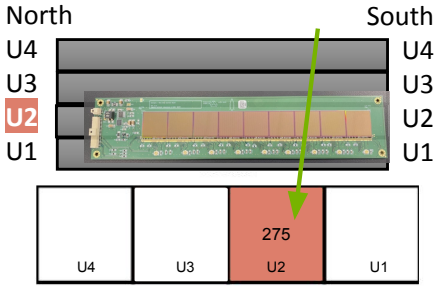
# System Integration: Current Status & Plan

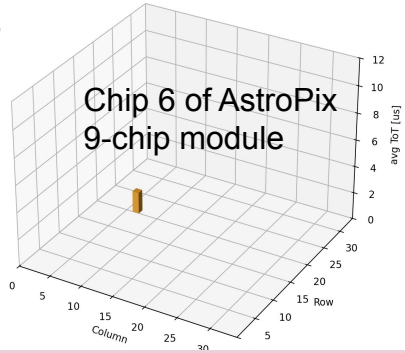
**AstroPix 9-chip module+Pb/SciFi SFIL in bench test** (Sep. 2025)

- Scintillator signals used as trigger IN for Pb/SciFi SFIL's DAQ and streaming readout for AstroPix DAQ
- Example cosmic-ray event display from the integrated system with internal clocks

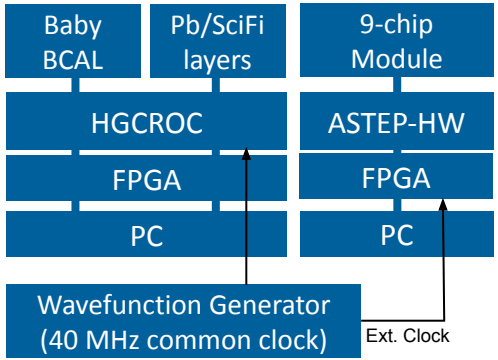


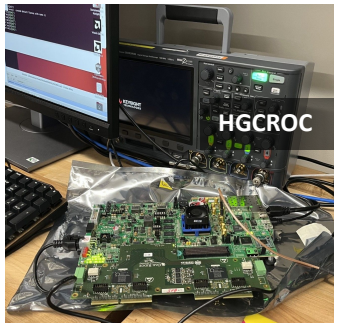



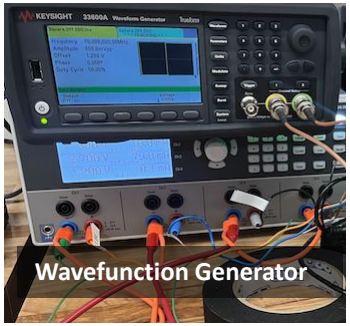



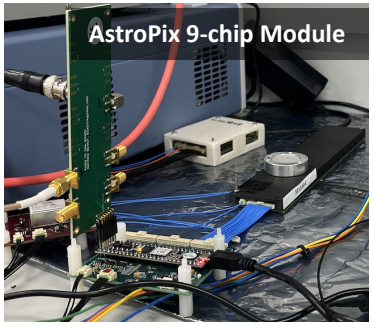




→ **Proof-of-principle integration of AstroPix 9-chip+A-STEP and SFIL+HGCROC with internal DAQ clocks**




→ In progress: **40 MHz common external clock tests** using the current AstroPix + Pb/SciFi test articles.

# High-level Plan Toward Final Design

## System Integration & Synchronization

**Prepare the system integration of AstroPix+Pb/SciFi for testing**

**Thin Pb/SciFi layer with integrated AstroPix 9-chip module test article**

- Test with 40 MHz external common clock to both ASTEP and HGCROC/CALOROC for synchronization *- in progress*

**Pb/SciFi layer with integrated AstroPix Stave**

- Half-stave testing with AstroPix ETC - *FY26 Q4*
- Test with 40 MHz common clock to both AstroPix ETC and HGCROC/CALOROC

**Pb/SciFi sector with integrated AstroPix trays** performance validation and testing - *FY27 Q4*

- Verification of full system response with MIPs. Read out both systems in sync, cross calibration for energy and position between SciFi and AstroPix. Thermal performance in the full system (trays + sector + ESB)

# Thank you

# Environment, Safety, & Health

- Each lab follows their internal work planning and controls processes
  - Identify hazards, implement mitigations, document procedures
- Main hazards
  - Low electrical hazard
  - Radioactive sources

# v3 Quad chip: Performance Test Results (1)

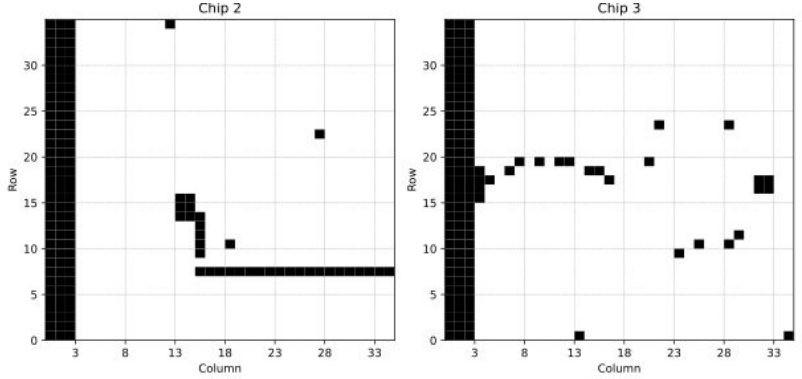
| chip 2 | chip 3 |
|---|---|
| chip 0 | chip 1 |

## Bench Test: Noise scan

- Goal: Quantify the fraction of pixels responsive within the dynamic range and exhibiting intrinsic noise rates below the threshold.
- Pixels with noise rates ≥ 1 Hz are masked, resulting in an active pixel yield of ≥ 97%.

*Chip 2 and Chip 3 have lower active pixel yield due to the special quad-chip structure (bus bar).

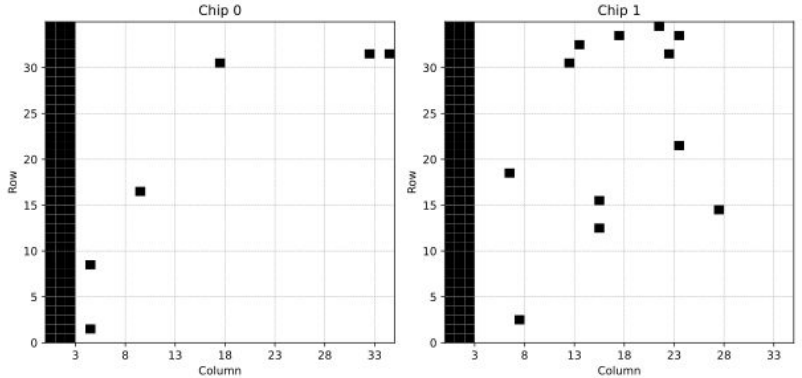
Active pixels: 97.0%
34/1,120 pixels disabled




Active pixels: 97.7%
26/1,120 pixels disabled




Active pixels: 99.5%
6/1,120 pixels disabled

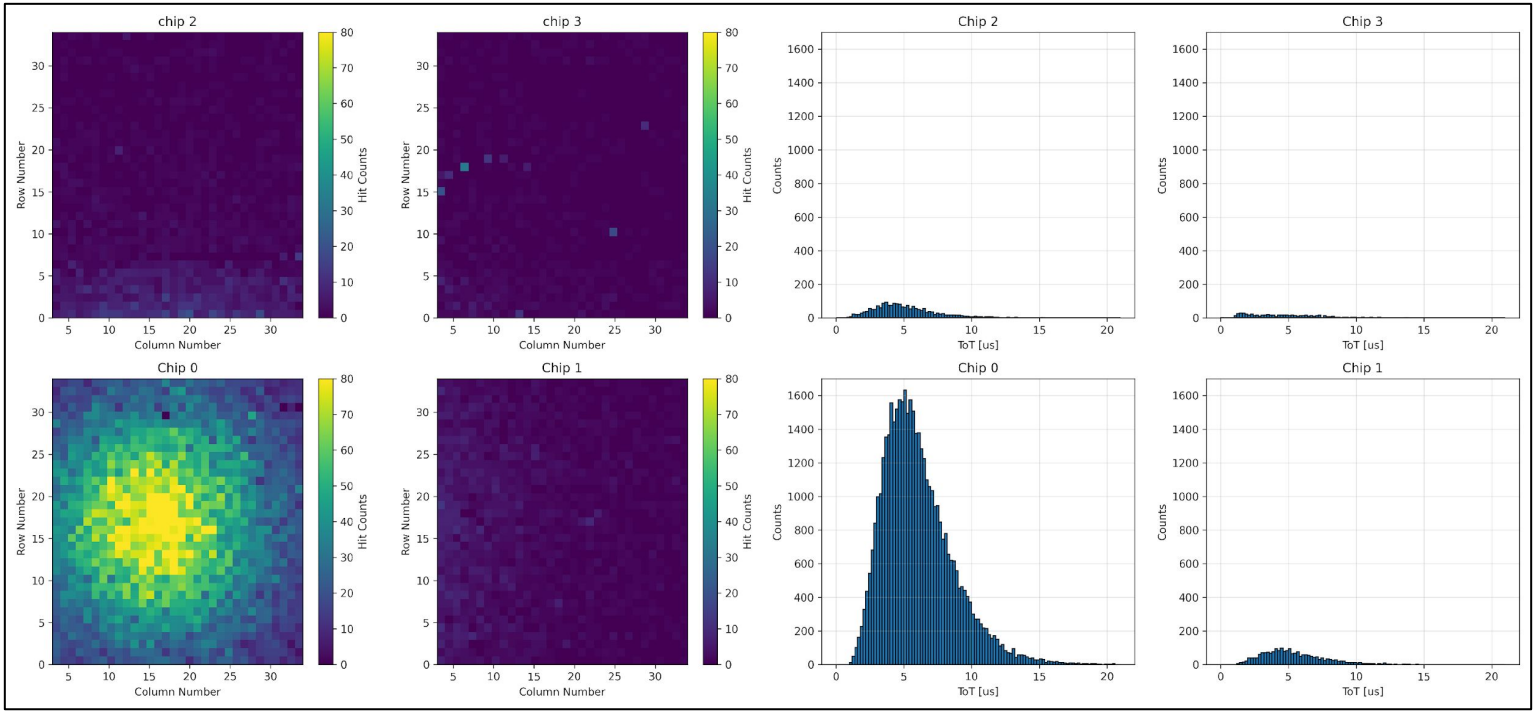



Active pixels: 98.9%
12/1,120 pixels disabled

# v3 Quad chip: Performance Test Results (2)


## Bench Test: Source test with Sr90 for Performance vadliation

- Radiation source tests show hit maps aligned with the source positions (Chip 2, 3, 0, 1).
- ToT distributions are well-described by a Landau convoluted with a Gaussian function.
- Results are consistent with v3 single-chip performance, confirming proper operation.



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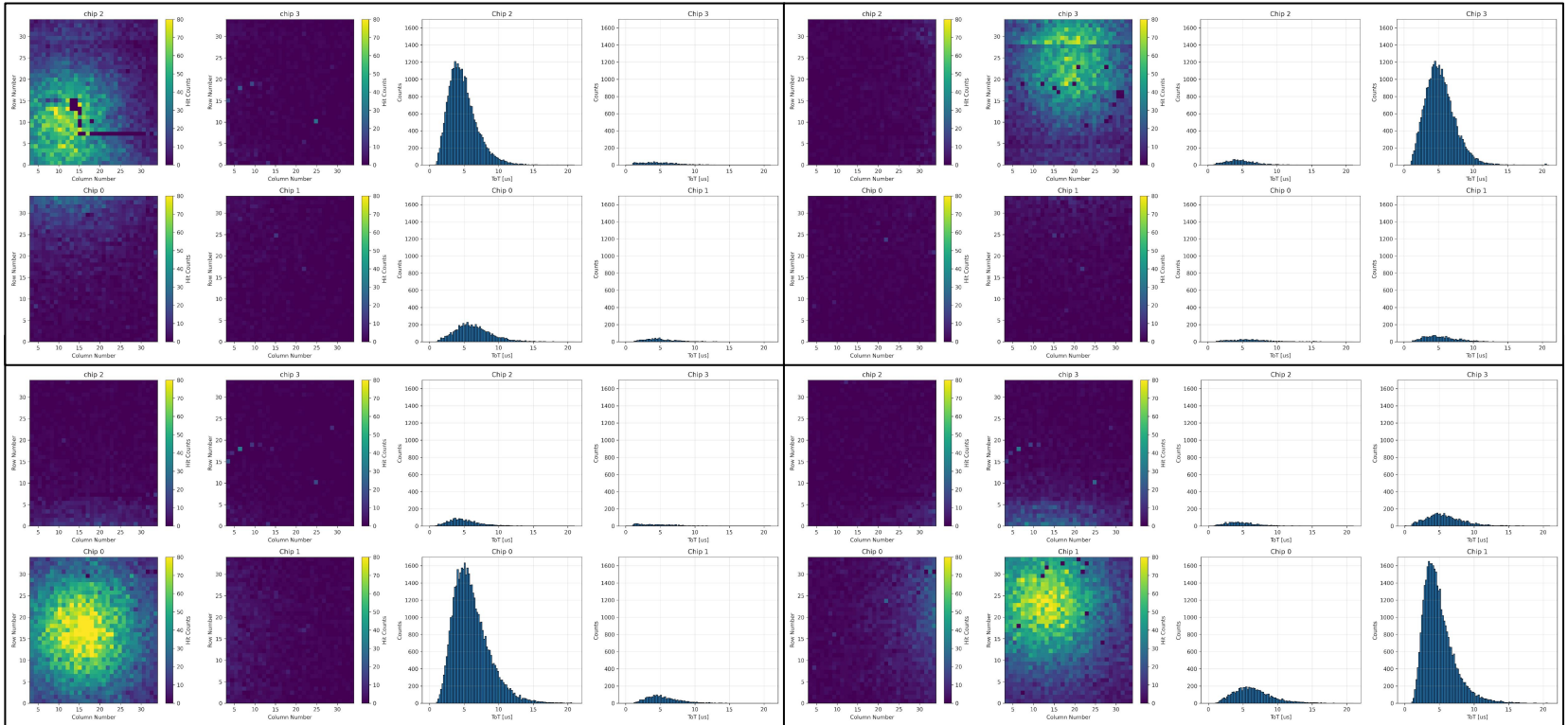
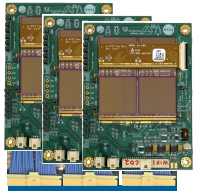


# Three v3 Quad chips: Performance Test Results (1)

## Bench Test: Cosmic test using three layers of quad-chips

- Goal: To verify that the software and firmware under development operate properly
  - Designed to share same AstroPix timestamp for three layers
- Representative event: all three layers share the same timestamp
  - 1 TimeStamp = 400 ns

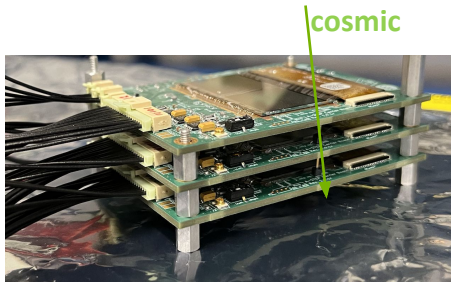
→ Validated capability to read data from all quad chips (up to 3x(2x2))

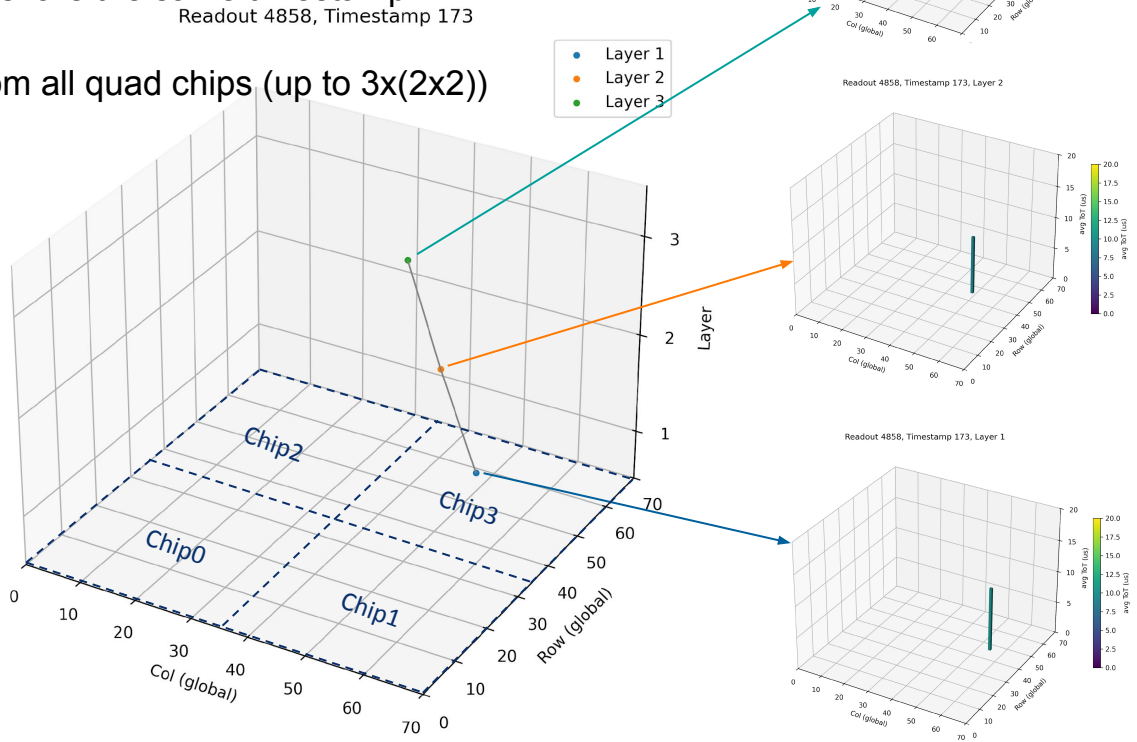


ASTEP-HW

FPGA

PC



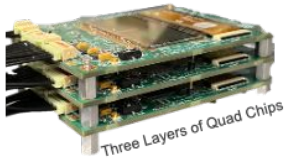



# Test Setup

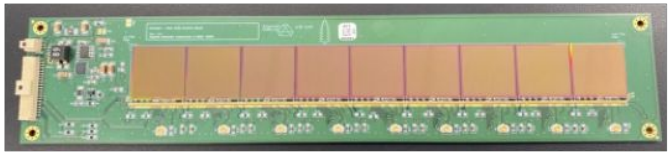
- 1x1


- 2x2


- (2x2)x3

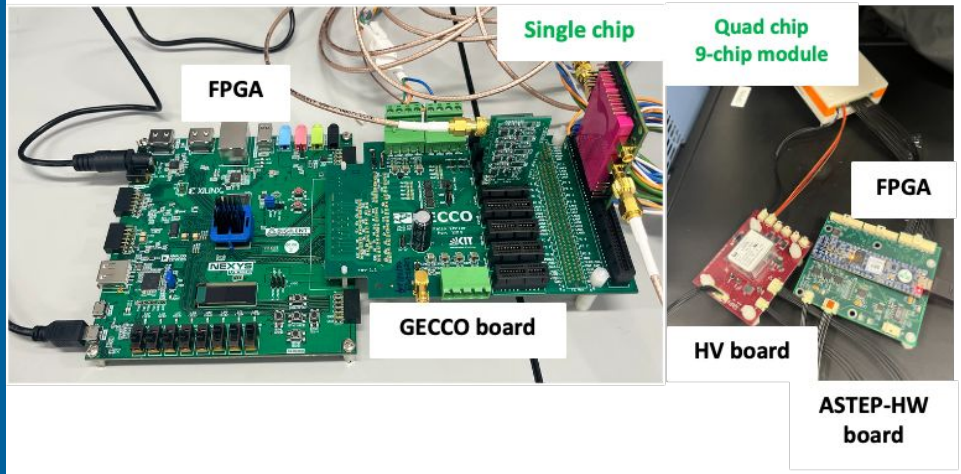



- 1x9





## Two testing setups for AstroPix



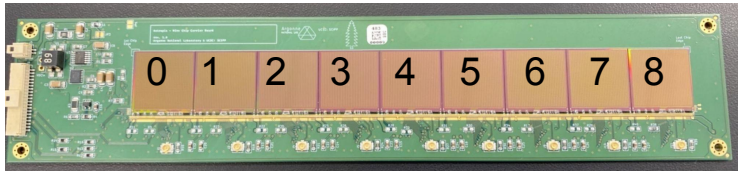

## Bench test

- Noise scan (w.r.t thresholds)
  - → Masking noisy pixels
- Injection test (w.r.t different injection voltages)
  - → ToT response vs injection voltages
- Radiation source test
  - → Calibration curve each pixel
  - → w. Sr90: Validation of configuration

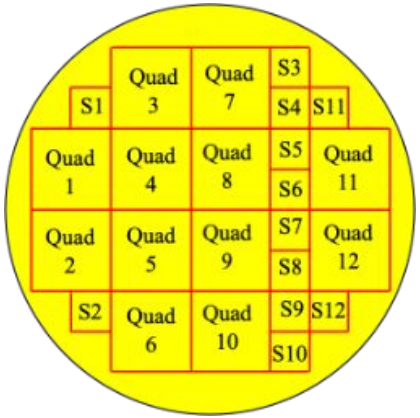
## Beam test

- 120 GeV Proton beam @FNAL (June.2024)
  - → MIP response
  - → Depletion depth

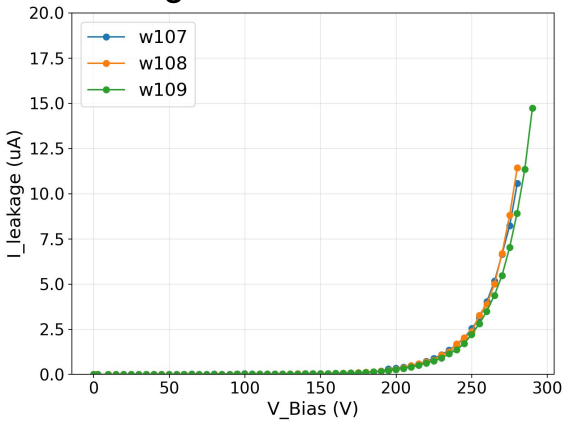
# IV measurement




w106s03/04/05/06/07/08/09/10/11 mounted on 9-chip prototype module

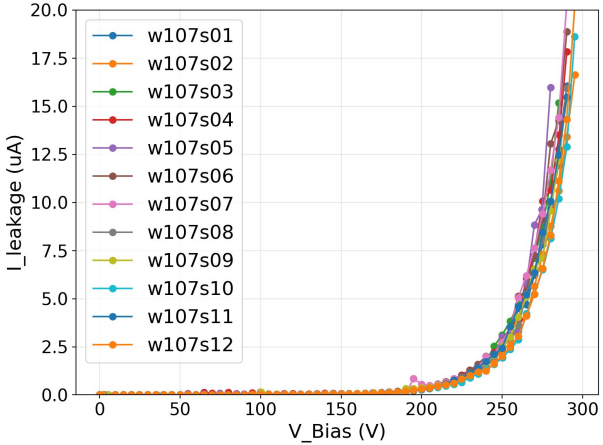



avg.IV w.r.t wafers

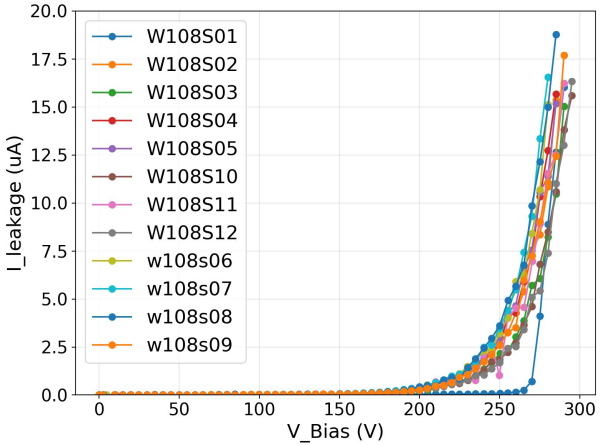



Move to Sanghoon's Talk (QC)

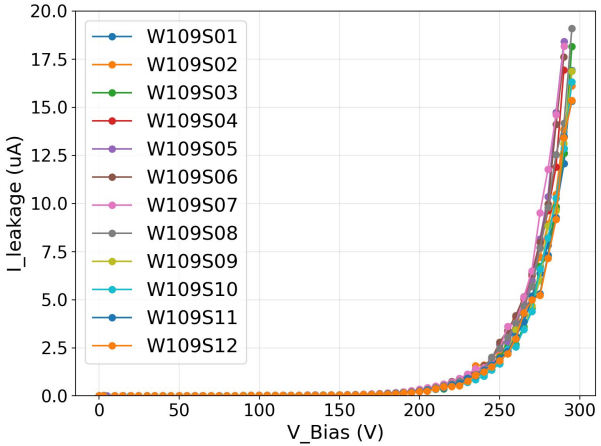
- W107




- W108



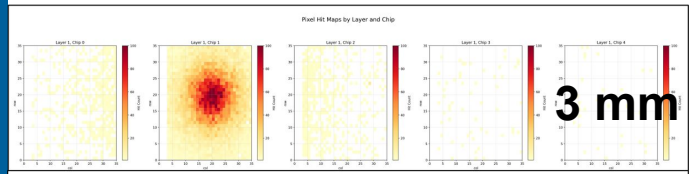

- W109

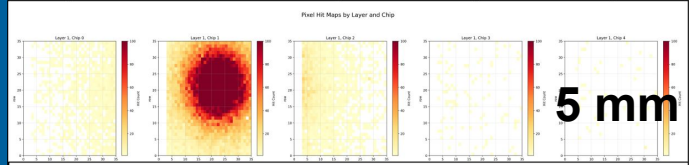


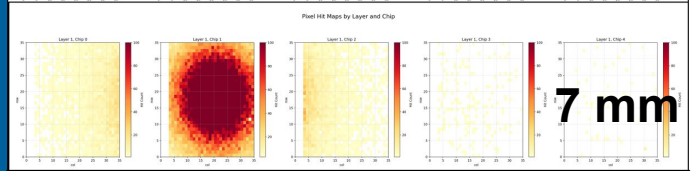
# System Testing for Integration: External Clock Testing

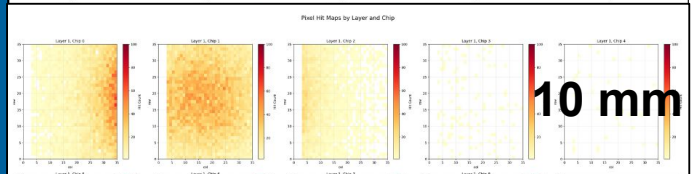
- ✅ External-clock source test with 10 µCi Sr-90 and various collimators
- The maximum readout rate provided by the current SW/FW is about **13 readouts/s**.
  - When the source covers one chip (chip 1), it also affects the neighboring chips.
    - The maximum number of hits is **1,766.5 Hz** (total).
    - The maximum number of hits per chip is **1,606.9 Hz**.
    - The maximum hit rate per pixel was measured to be about **3.6 Hz**.

Collimator: 3/5/7/10/16 mm diameters




- With 10 mm and 16 mm collimators, AstroPix reaches the **saturation limit**, where stable data-taking is no longer possible.

| Collimator | readout/s | Total Hits/s | Total Hits/s/chip | Hits/s/pixel |
|---|---|---|---|---|
| 3 mm | 2.7 | 445.8 | 423.5 | 1.8 |
| 5 mm | 7.0 | 1144.6 | 1069.5 | 3.6 |
| 7 mm | 12.7 | 1766.5 | 1606.9 | 3.6 |
| 10 mm | 13.0 | 755.3 | 461.2 | 1.2 |
| 16 mm | 13.2 | 317.4 | 219.9 | 1.0 |

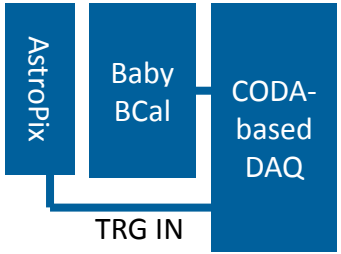
*chip with source on top

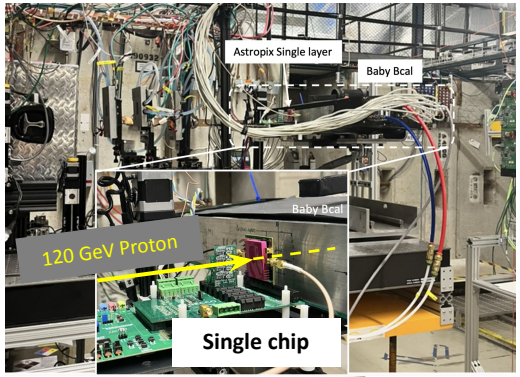
→ Max per-chip rate observed with the current setup (consistent with TDR: Max rate per chip of 924.8 Hz)

# Previous Test Result

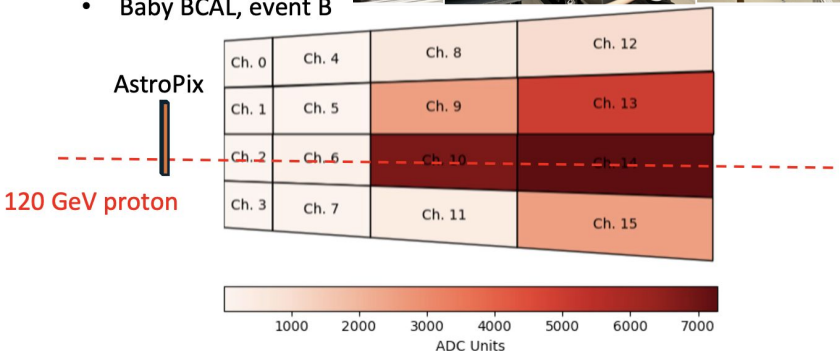
## AstroPix+BabyBCAL @Beam test (June 2024)

- Baby BCAL triggered by analog signal from one pixel of AstroPix



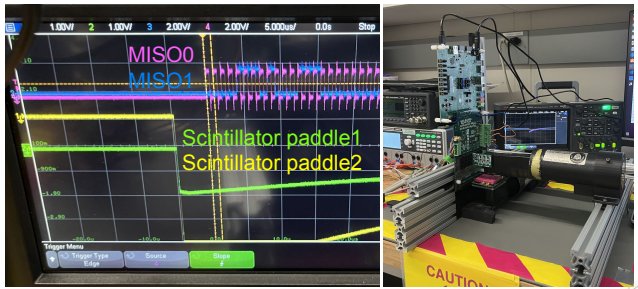

- Baby BCAL, event B

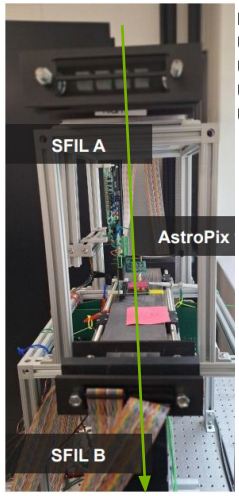


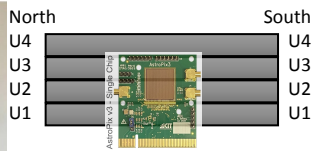

Example plot of 120 GeV proton event display from an integrated system of Baby BCAL and a single-layer AstroPix v3

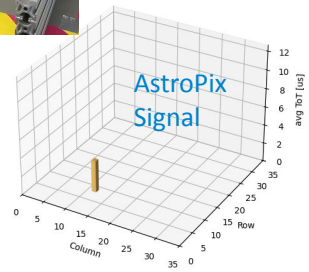
## AstroPix+SFILs @Bench test (April 2025)

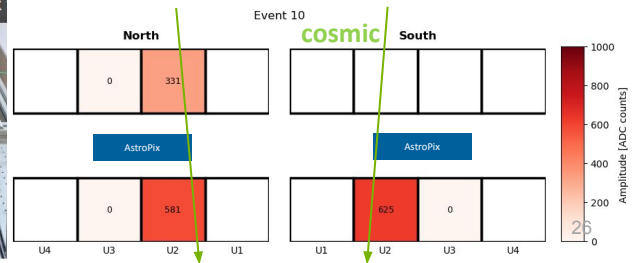
- LVDS MISO signals that generated from AstroPix used as trigger IN for DAQ



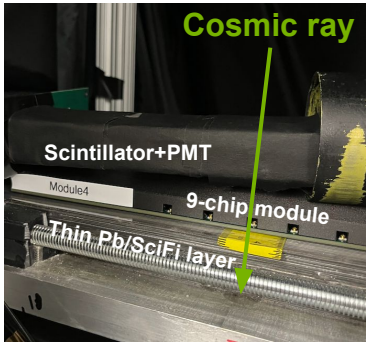



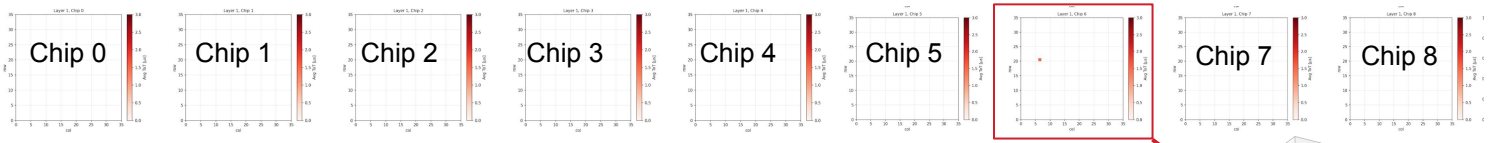



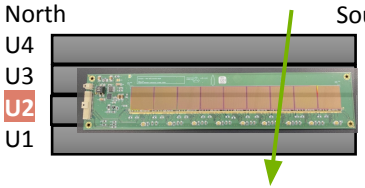
# First Trial: System Test with Internal Clock

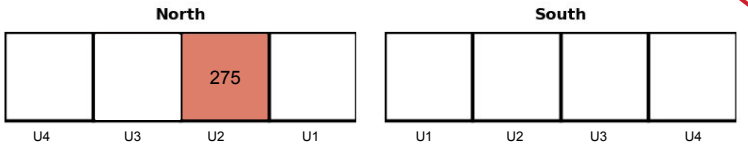
## AstroPix 9-chip module + SFIL as test articles @Bench test (Sep. 2025)

- Example cosmic-ray event display from the integrated system (AstroPix 9-chip + A-STEP, SFIL + H2GCROC)
- Event by comparing FPGA timestamp differences with each DAQ's internal clock

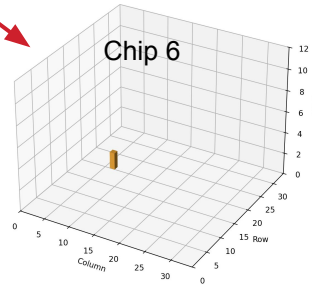


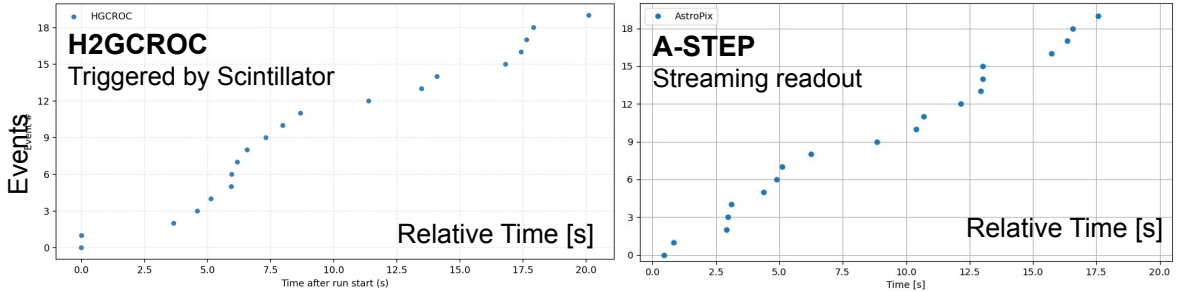



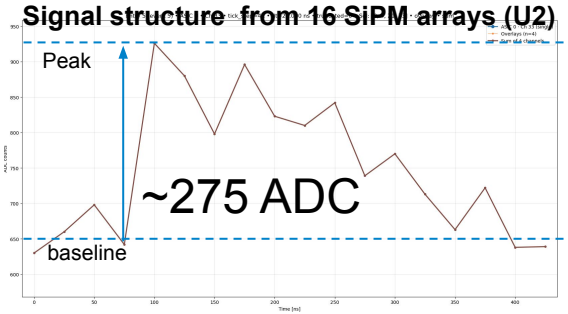




*More details on MIP response with a thin Pb/SciFi layer + H2GCROC in SciFi & System Demonstration (by H. Klest)




- FPGA timestamp converted into relative time (HGCROC/A-STEP)



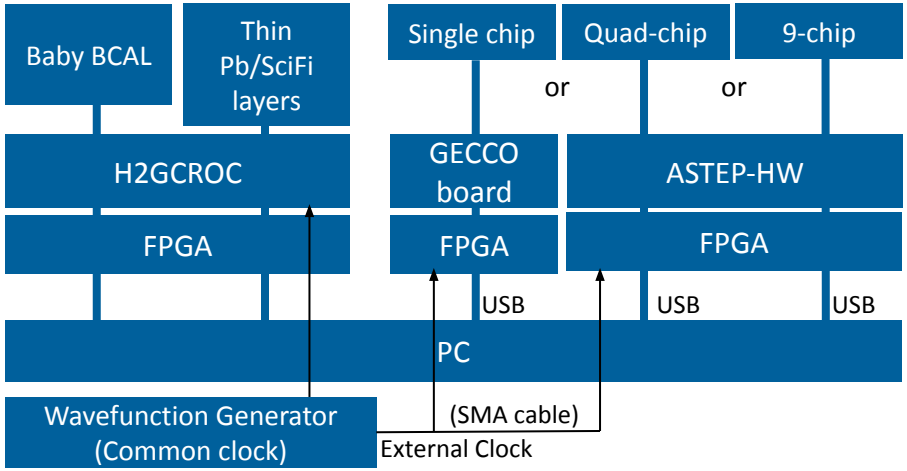




→ **Proof-of-principle integration of AstroPix 9-chip+A-STEP and SFIL+HGCROC at the bench.**

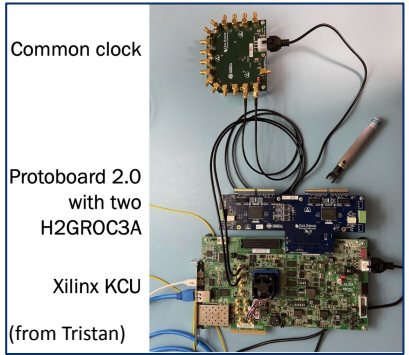
# System Testing for Synchronization

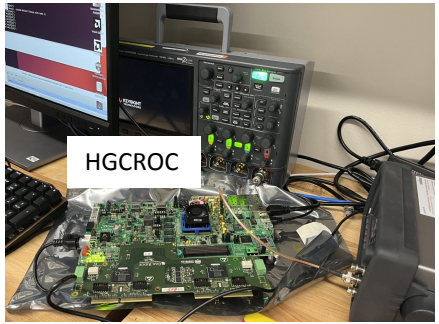
## Synchronization Plan between AstroPix DAQ and H2GCROC for Pb/SciFi

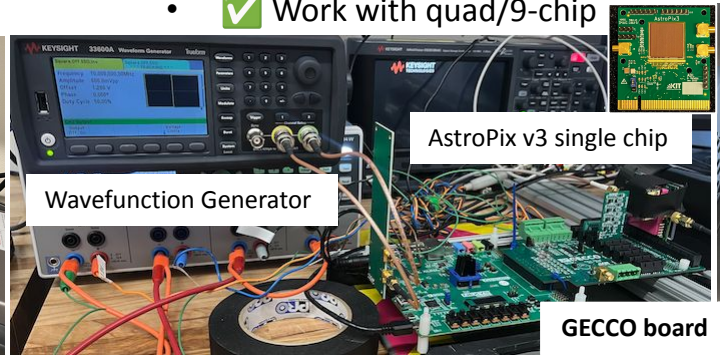
- Provide 40 MHz external clock to H2GCROCs and AstroPix DAQ by comparing with FPGA timestamp difference

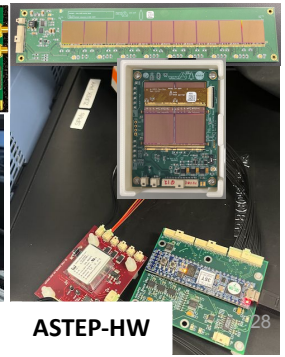



- **AstroPix single chip+ GECCO board + Nexys + ASTEP sw/fw**
  - 10 MHz LVDS external clock
  - Both Timestamp and the FPGA timestamp external
  - 🚧 Debugging: fixed FPGA TS and broad ToT distribution
- **AstroPix quad-chip / 9-chip prototype module + ASTEP HW board + CMOD + ASTEP sw/fw**
  - 10 MHz single-ended external clock
  - Both Timestamp and the FPGA timestamp external
  - ✅ Work with quad/9-chip



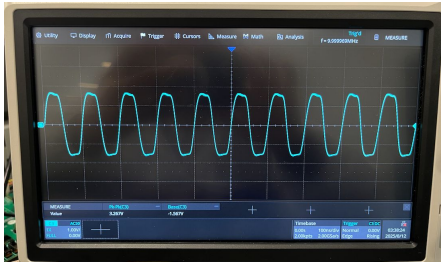



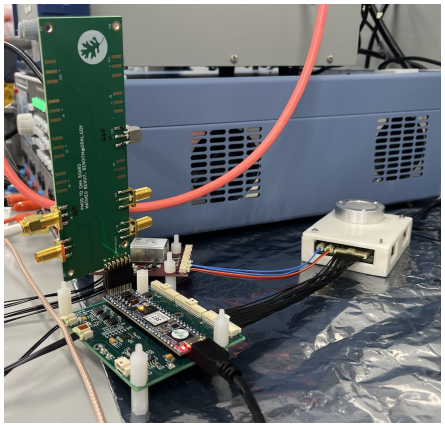



# System Testing for Integration: External Clock Testing (1)

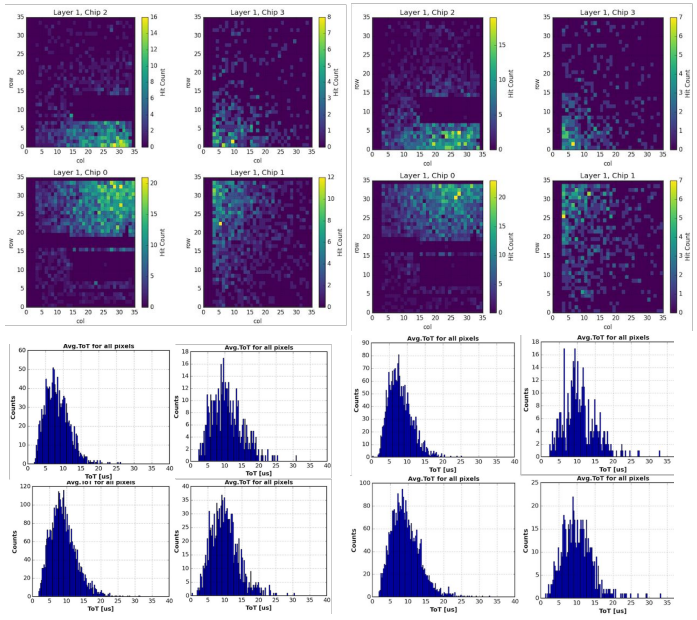
## Quad-chip

- Goal: Verify external-clock operation and basic readout stability
- First attempt: AstroPix quad-chip + ASTEP HW board + Cmod A7 + ASTEP SW/FW
  - 10 MHz single-ended clock via PMOD → working as intended

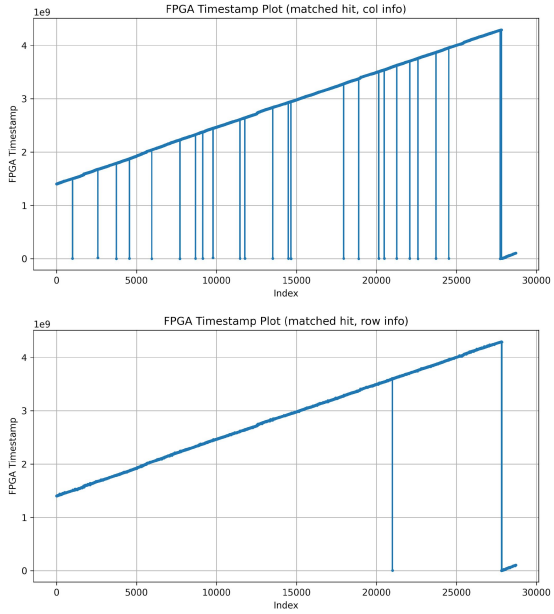




- internal clock vs external clock




- FPGA TS (external clock) for **5-min** run

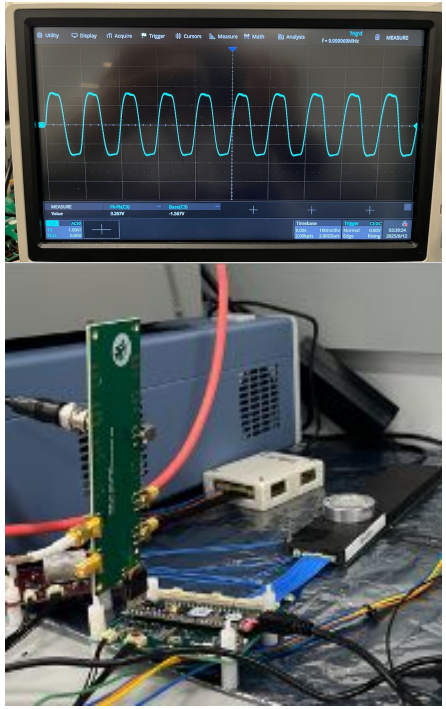



**→ Verified operation of the 10 MHz external clock with the quad-chip by showing consistent results compared to the internal clock.**

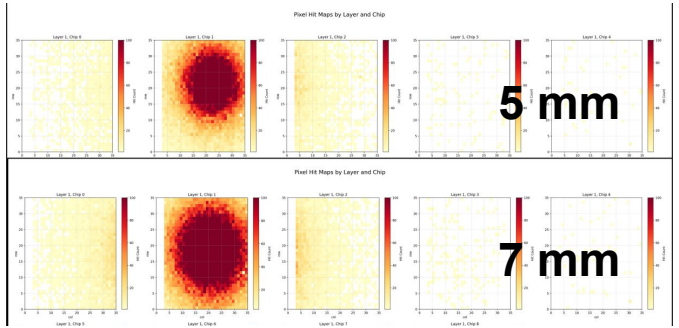
# System Testing for Integration: External Clock Testing (2)

## 9-chip Module

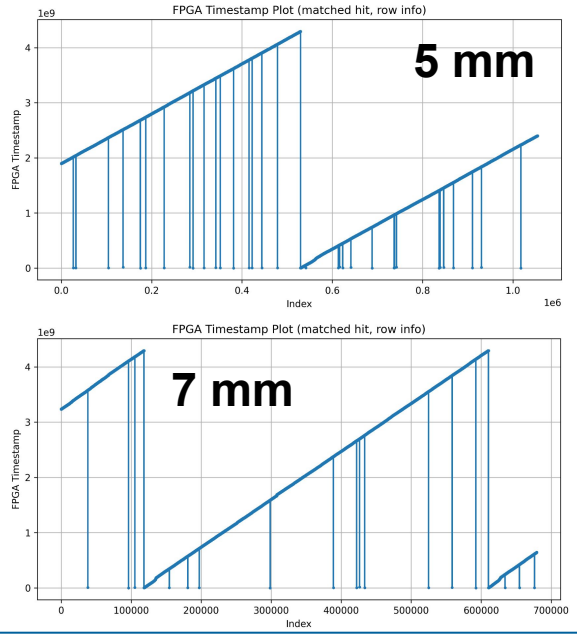
- Goal: Verify external-clock operation and basic readout stability
- First attempt: AstroPix 9-chip + ASTEP HW board + Cmod A7 + ASTEP SW/FW
  - 10 MHz single-ended clock via PMOD → working as intended



- Hit map with 5/7mm collimator




- FPGA TS (external clock) for **10-min** run




→ **Verified operation of the 10 MHz external clock with the 9-chip module and the current setup**