BERKELEY LAB
Bringing Science Solutions to the World

A summary of the recent SVT working meeting

Ernst Sichtermann

ePIC TIC meeting
August 4, 2025 – Zoom

SVT working meeting at SBU – July 9–11,2025

Courtesy Nicole Apadula

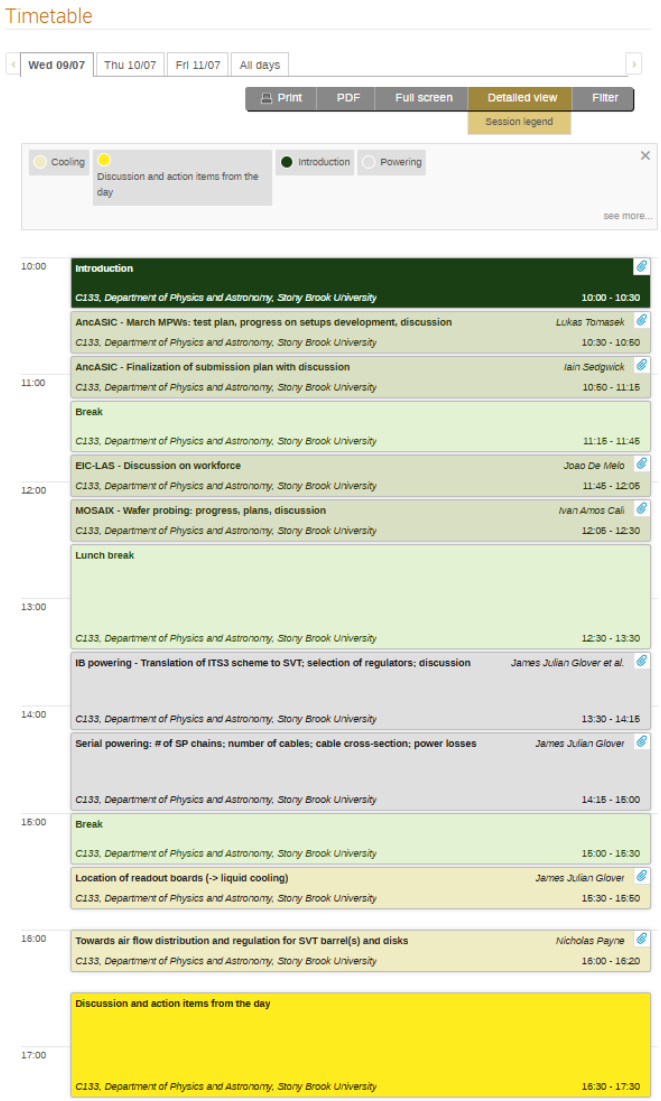
Productive working meeting; many topics covered,

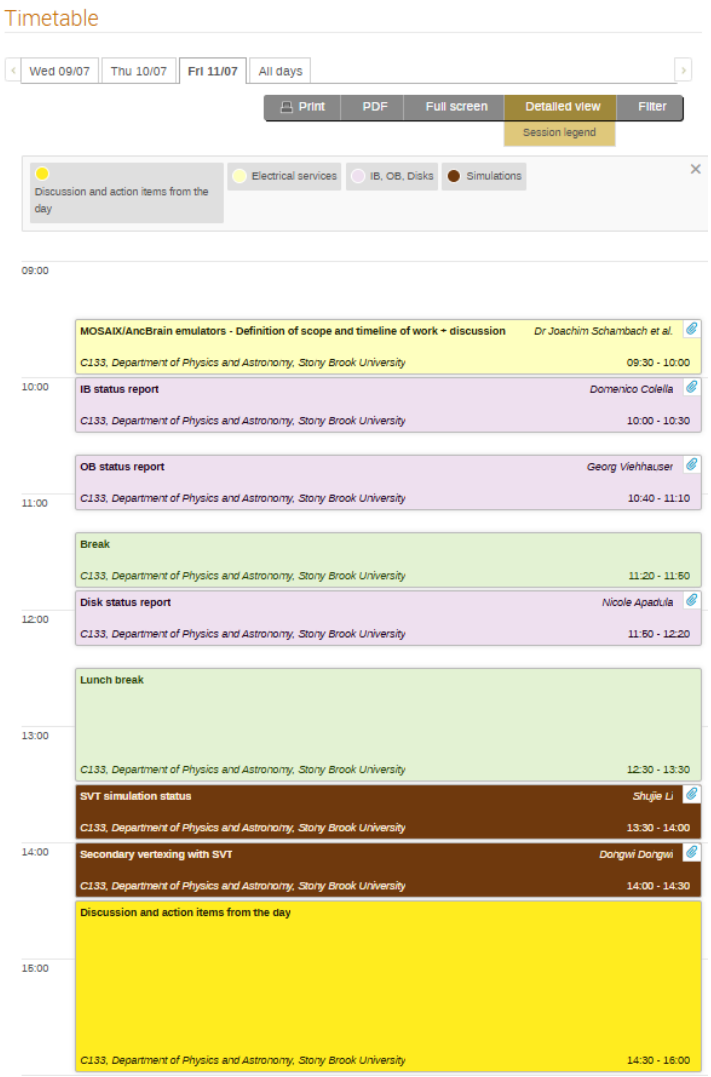
46 registered participants; about equally split between in-person and online,

Thanks to all who participated, in person and online! Thanks to CFNS for hosting us.

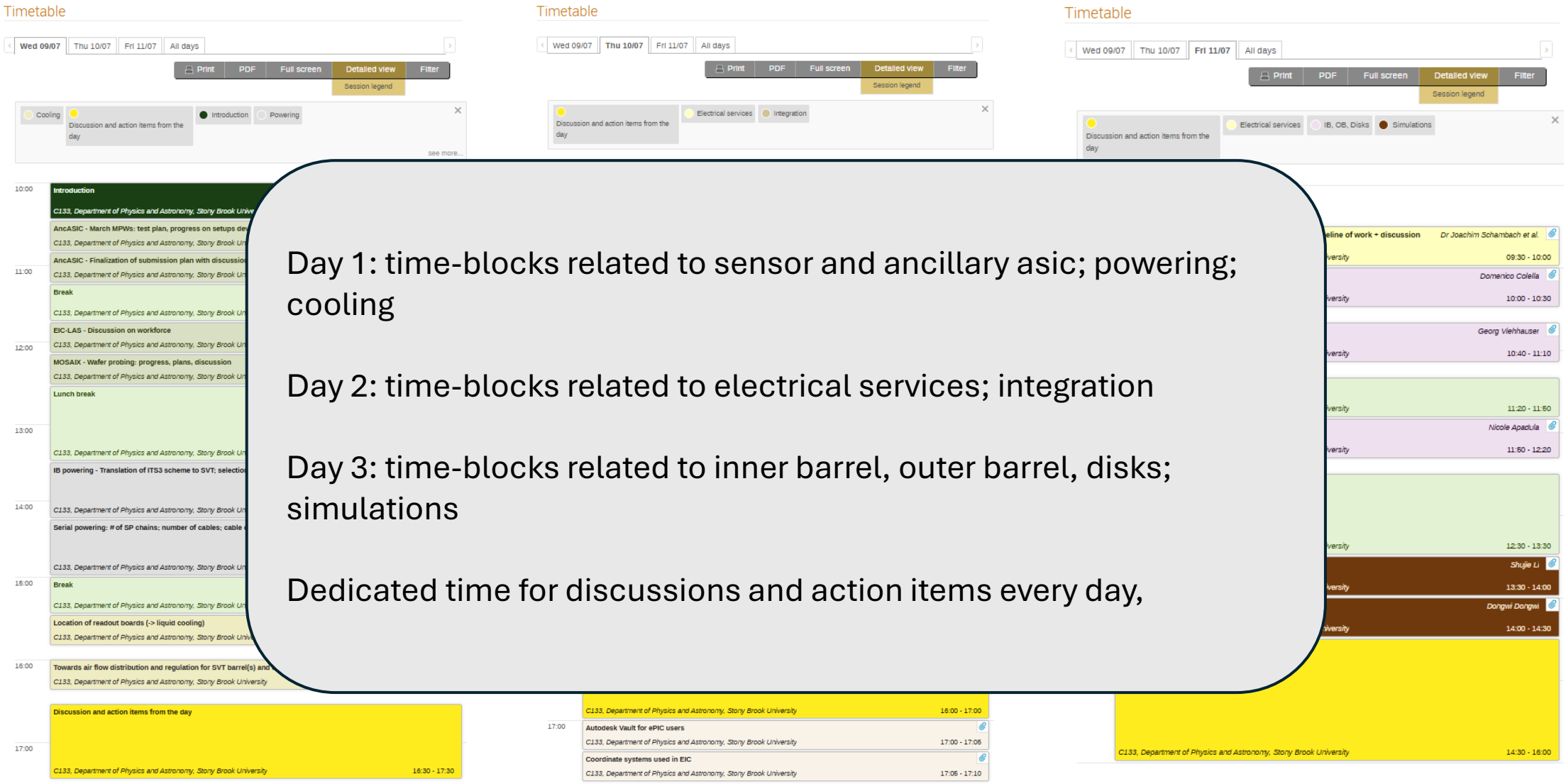
All materials are posted at: https://indico.bnl.gov/event/28216/

SVT working meeting at SBU – July 9–11,2025





SVT working meeting at SBU – July 9–11,2025



Day 1: time-blocks related to sensor and ancillary asic; powering; cooling

Day 2: time-blocks related to electrical services; integration

Day 3: time-blocks related to inner barrel, outer barrel, disks; simulations

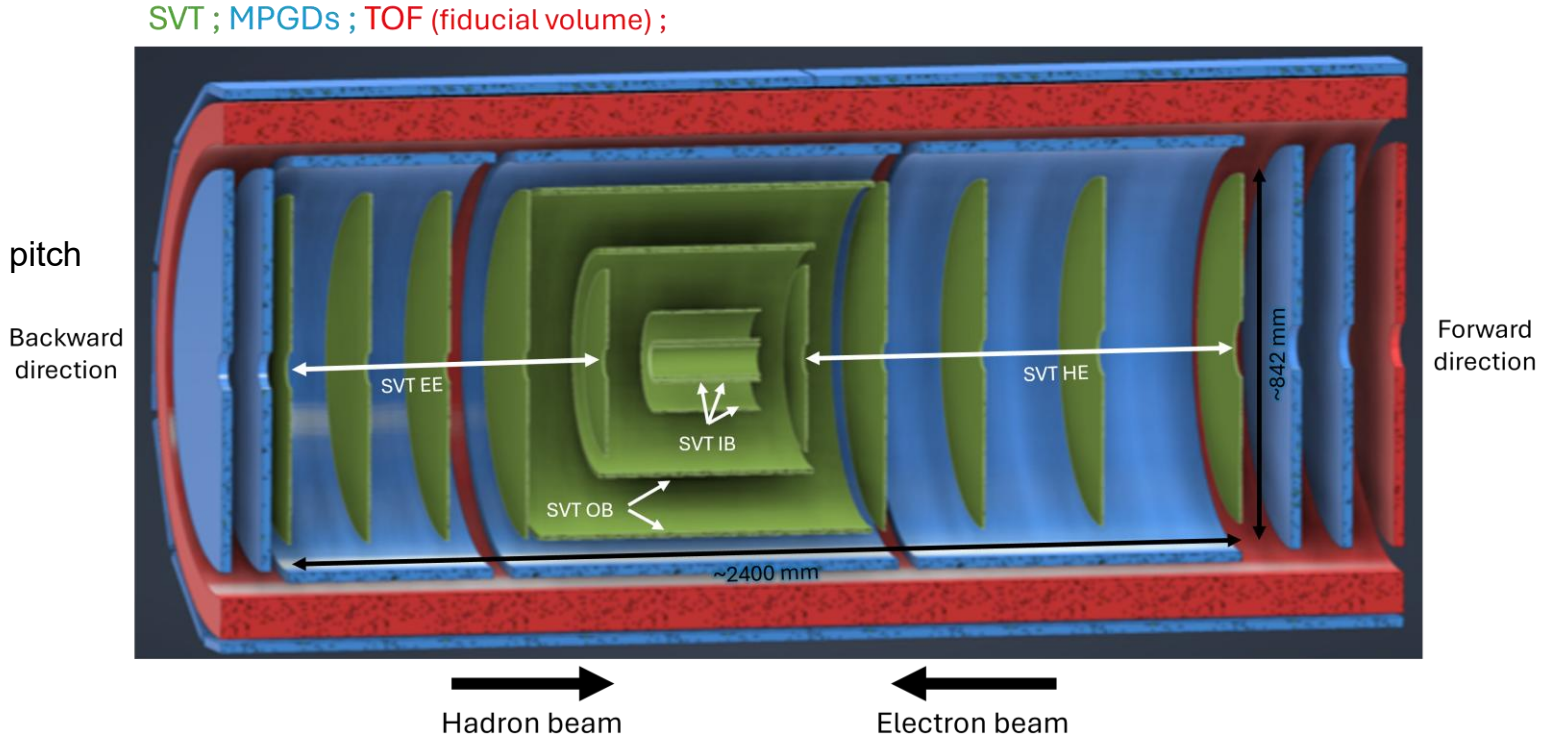
Dedicated time for discussions and action items every day,

SVT Concept

Inner Barrel (IB)
- Three layers, L0, L1, L2,
- Radii of ~ 36, 48, 120 mm
- Length of approx. 27 cm
- x/X_0 ~ 0.05% per layer
- Curved, thinned, wafer-scale sensor, ~20um pixel pitch

Outer Barrel (OB)
- Two layers, L3, L4
- Radii of ~ 27 and 42 cm
- X/X_0 ~0.25% and ~0.55%
- Stitched sensor, ~20um pixel pitch
- More conventional structure w. staves

Electron/Hadron Endcaps (EE, HE)
- Two arrays with five disks
- x/X_0 ~0.25% per disk
- Stitched sensor, ~20um pixel pitch
- More conventional structure w. halve disks



Constrained by beampipe + 5mm at the inner barrel and disk radii; $r_{SVT} < 43$ cm; $-105 < z_{SVT} < 135$ cm,

Lengths for L2—L4 increase so as to project back to z = 0; disk radii adjust accordingly,

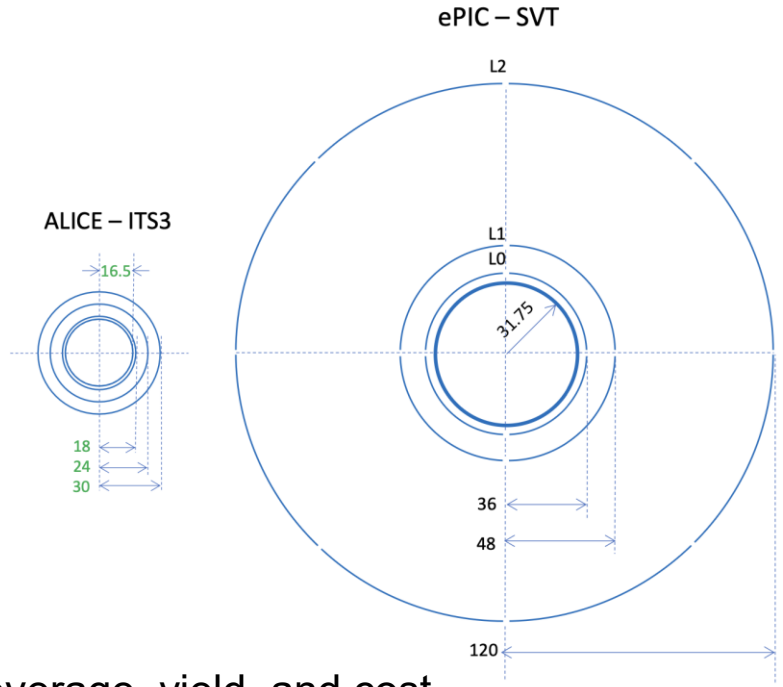
Optimized for acceptance and resolutions within constraints,

Clamshell of detector halves; beam-pipe bake-out with SVT installed,

OB staves, IB halves, and half Disks will be shipped to BNL – installation sequence OB, IB, disks.

SVT Sensor and Ancillary ASIC

For reference



1. ITS3-like Inner-Barrel layers

- Re-use the **ITS3 sensor** as is
- Adapt the ITS3 detector concept to the EIC:
  - Mechanics of bent layers — sensor and support — for the larger EIC radii
  - Services and cooling design and routing for the EIC acceptance requirements
  - Considerations related to in-situ beam-pipe bake-out at the EIC

2. EIC variant for the staves in the Outer Barrel and the Endcap Disks

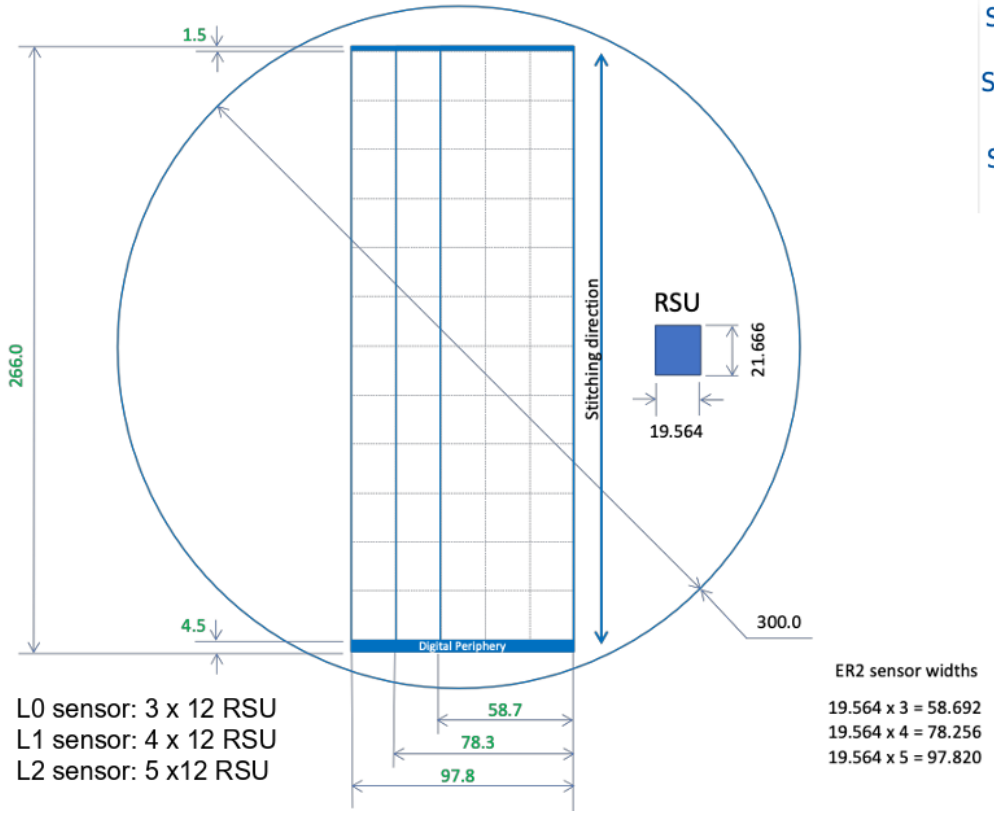
- **EIC Large Area Sensor (LAS)**, i.e. ITS3 sensor optimized for large-area coverage, yield, and cost
  - EIC LAS will be stitched, but not to wafer scale; functionality and interfaces stay largely unchanged
  - Size(s) of the EIC LAS defined by requirements for full coverage and yields, cost; studies have shown 5 and/or 6 RSUs
  - Approximately 4,000 EIC-LAS sensors will be used in the OB and Disks,
- More conventional carbon composite mechanical support structures with integrated cooling
- Lightweight electrical interfaces with **Ancillary ASIC** and aluminum flexible printed circuit technology

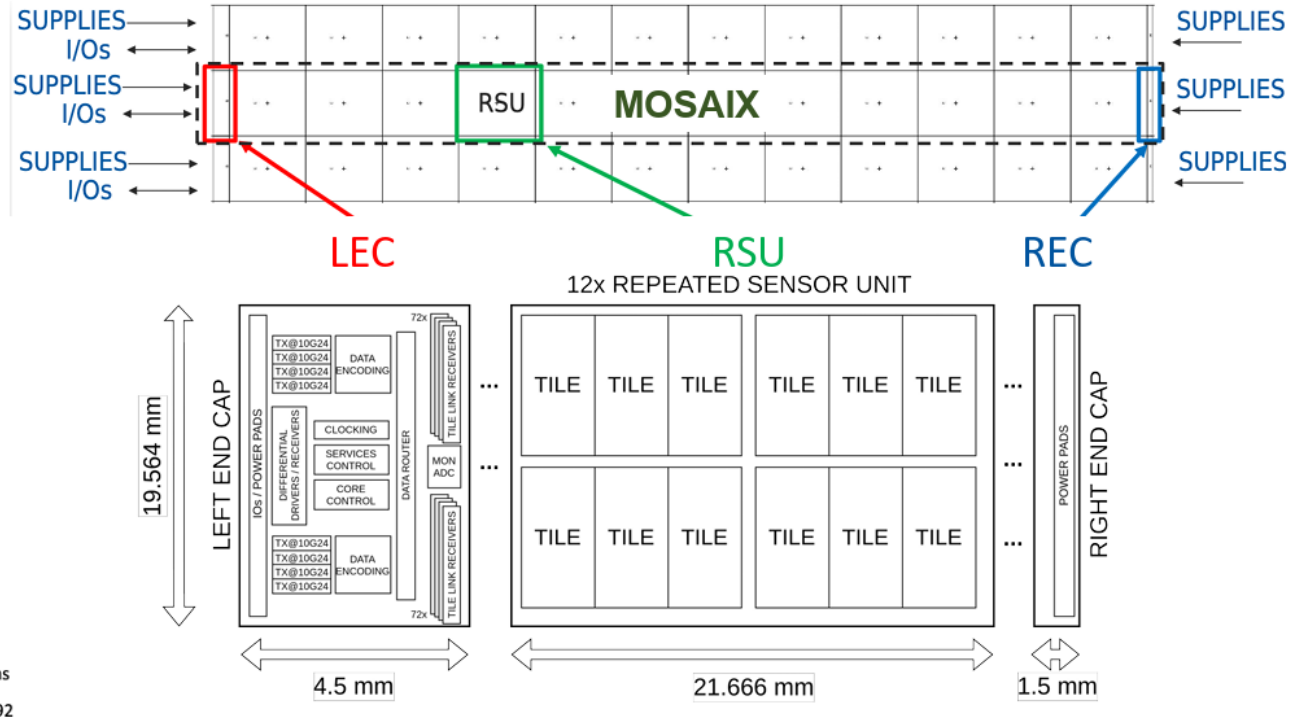
Ongoing characterization – wafer-probing development, irradiation and test beams, thermal and mechanical tests,

Preparation for production testing – probing of all ER3, EIC-LAS, ancillary ASIC.

MOSAIX

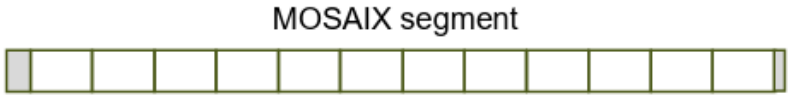
- MOSAIX (ER2) is a full feature prototype of the sensor for ALICE ITS3 and ePIC SVT IB,
- Wafer scale sensor design using the stitching technique,
- Process: TPSCo 65 nm CMOS Imaging Sensors,
- MOSAIX design leads to production sensor (ER3)





MOSAIX to EIC-LAS

Inner Barrel



- 12 RSUs
- 8 data links
- 7 slow control links
- Direct powering

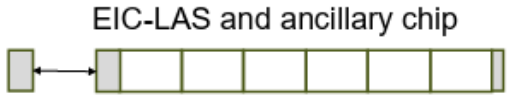
Improve yield and coverage

Lower material budget

Lower material budget, fit integration requirements

Lower material budget, fit integration requirements

Outer Barrel, E/H Endcaps



- **5 or 6 RSUs**
- **Single data link**

EIC-LAS

- Multiplex slow control
- Serial powering

Ancillary ASIC

Powering and Readout

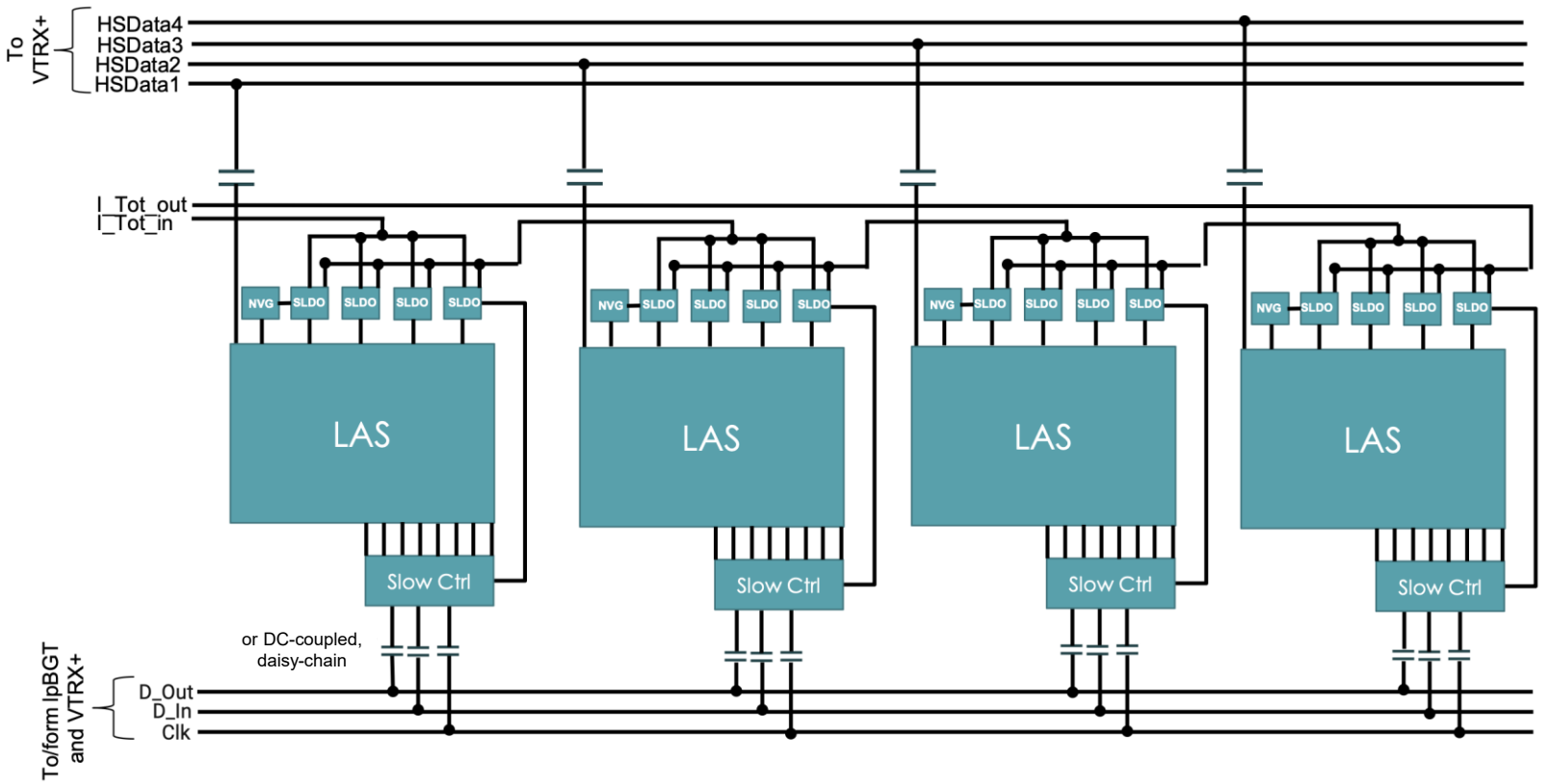
Inner Barrel will be directly powered and read out, adopting (and adapting) the ITS3 design,

Doing so for the outer barrel and/or disks would incur prohibitive service loads,

Instead, the outer barrel and disk design uses:

- serial powering of up to 4 EIC-LAS sensors,
- Multiplexing of slow control,

Powering and readout scheme for the Outer Barrel and Disks



Transition to fiber near the sensor; aggregate fibers outside of the detector and before the FELIX DAC board,

Configuration and powering of VTRx+ and FPC slow control will be handled by one or more types of control board

Ancillary ASIC

Lukas Tomasek (CTU)

MPW1/MPW2

MPW1 - AncASICXT011_P1:

- Negative Voltage Generator (NVG)
- SLDO Pre-Regulator
- CML Transceiver
- Transistor Test Structures (for radiation hardness validation of XT011 process)

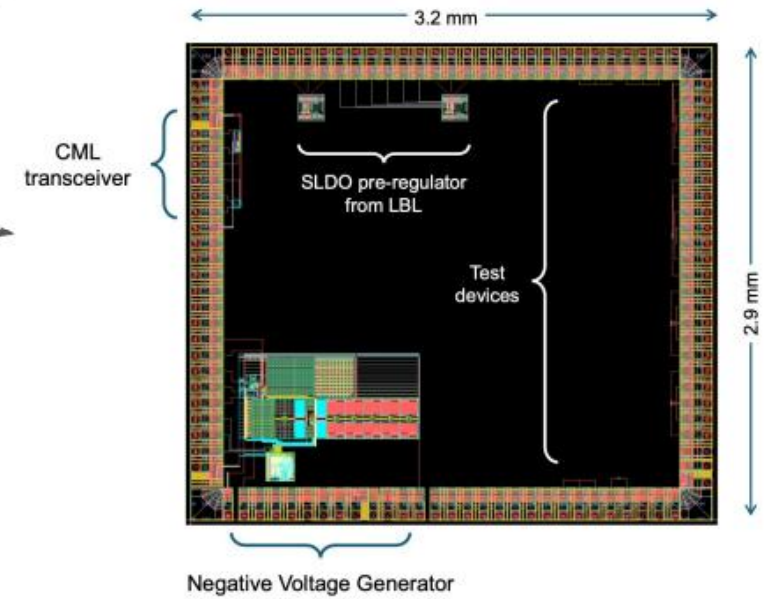
MPW2 - SLDO:

- SLDO by RAL

Details:

- **45 individual chiplets for each MPW1&2**
- already submitted
- **Delivery from the fab September 26, 2025**

1st Prototype: AncASIC sub-blocks and test devices



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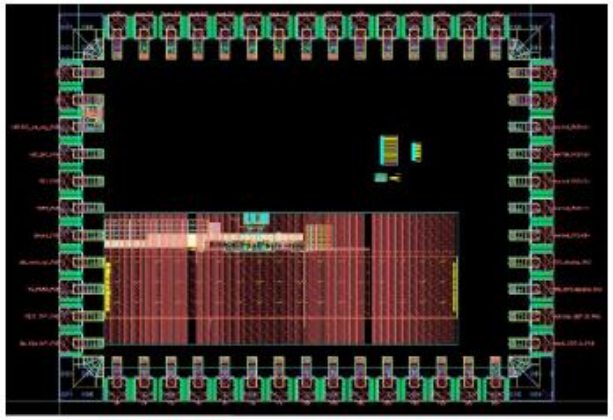

Science and Technology Facilities Council

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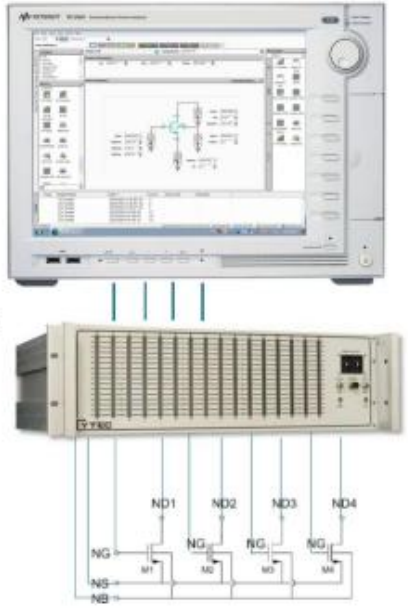
MPW1/MPW2 have blocks for power regulation (SLDO), bias voltage regulation; test structures
MPW3 complements this with slow control; design in progress, targeting Summer/Fall submission

Testing HW status MPW1

- **MPW1 Carrier Board** will be designed by Zhegwei Xue from LBL with help from BNL (Grzegorz, Niccolo) to start the design for functionality testing
- **Evaluation setup for test structure characterization and irradiation testing** with ^{60}Co source available at BNL

Evaluation setup

- Currently we have two B1500A semiconductor analyzers, with 4/5 SMU units each and one C-V unit
- Re-commissioning a switching matrix to test multiple devices
- The irradiation facility allows to have some instruments close to the source (w/ appropriate shielding) and to wire additional connections/communication out to the "control room"



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Irradiation facility

- Instrumentation dpt. owned and managed facility
- ^{60}Co source with 450 Ci activity in 2020
- Characterization of handheld-size samples at high dose rates (~10-20 krad/hour)
- Dosimetry with radiation protection division
- Used for strip detectors and asic for ATLAS, sPHENIX SiPM radiation damage

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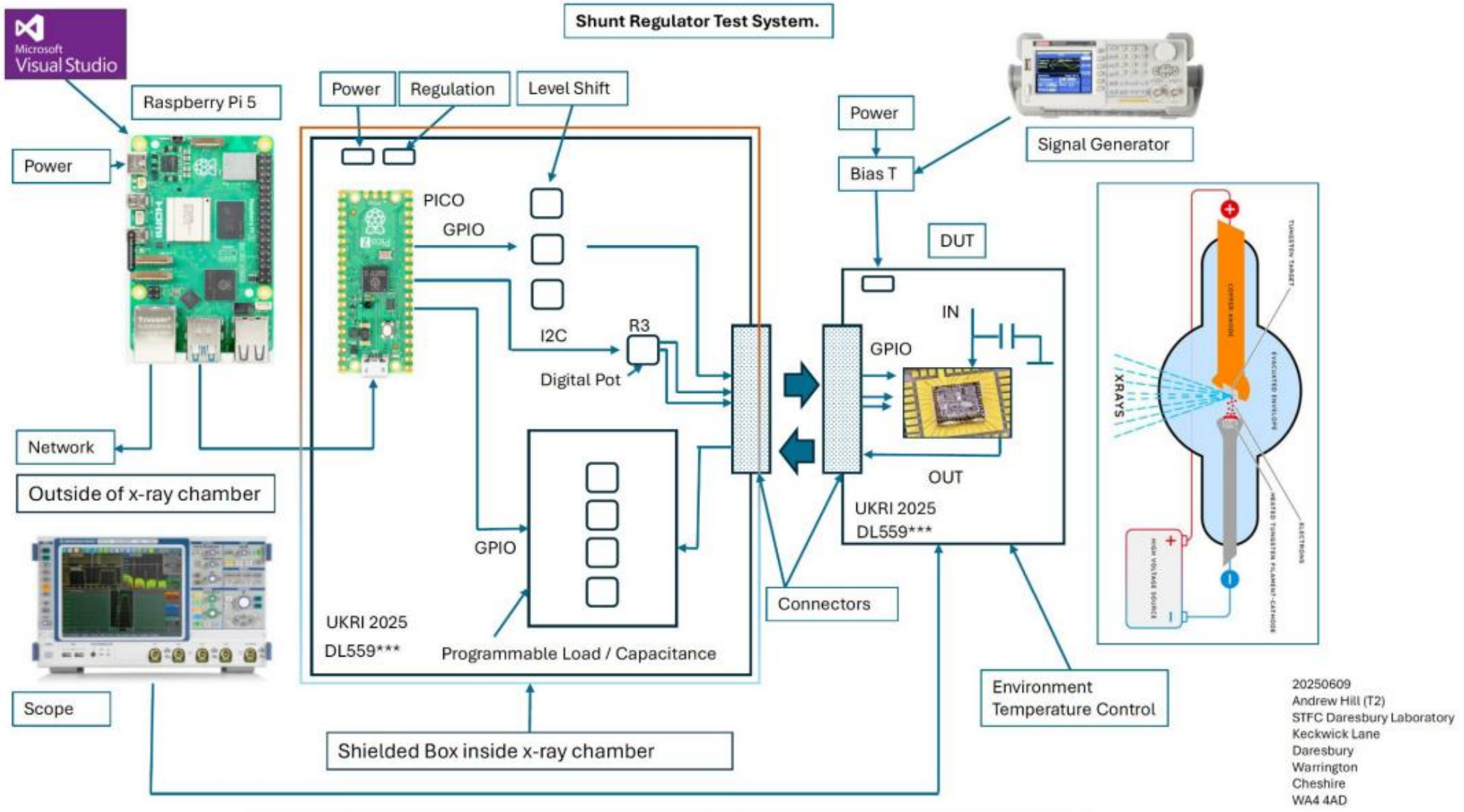
Lukas Tomasek (CTU)

Testing HW status MPW2

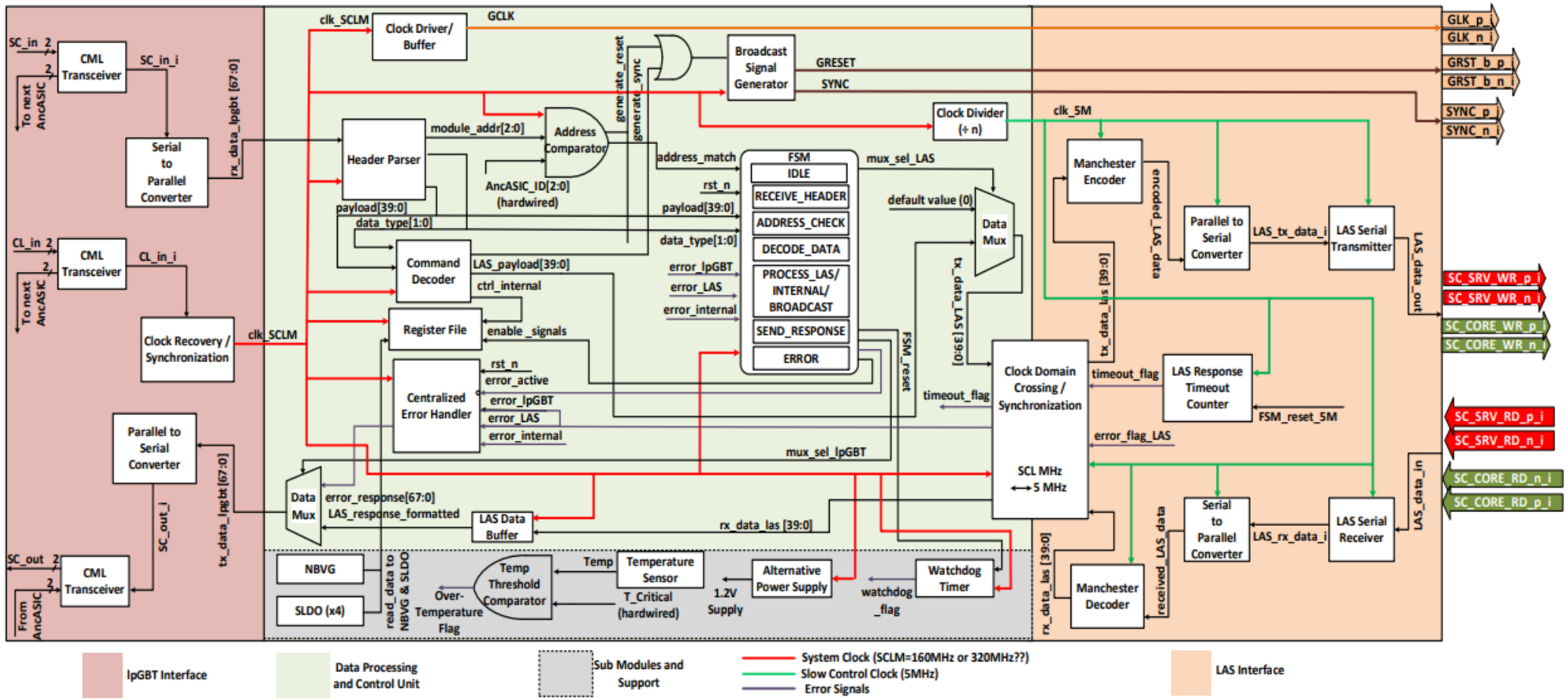
Shunt Regulator Test System by Andrew Hill, STFC Daresbury Laboratory



Ancillary ASIC – MPW3

Arif Iqbal (BNL)
Zhengwei Xue (LBNL)

EIC-AncBrain Block Diagram



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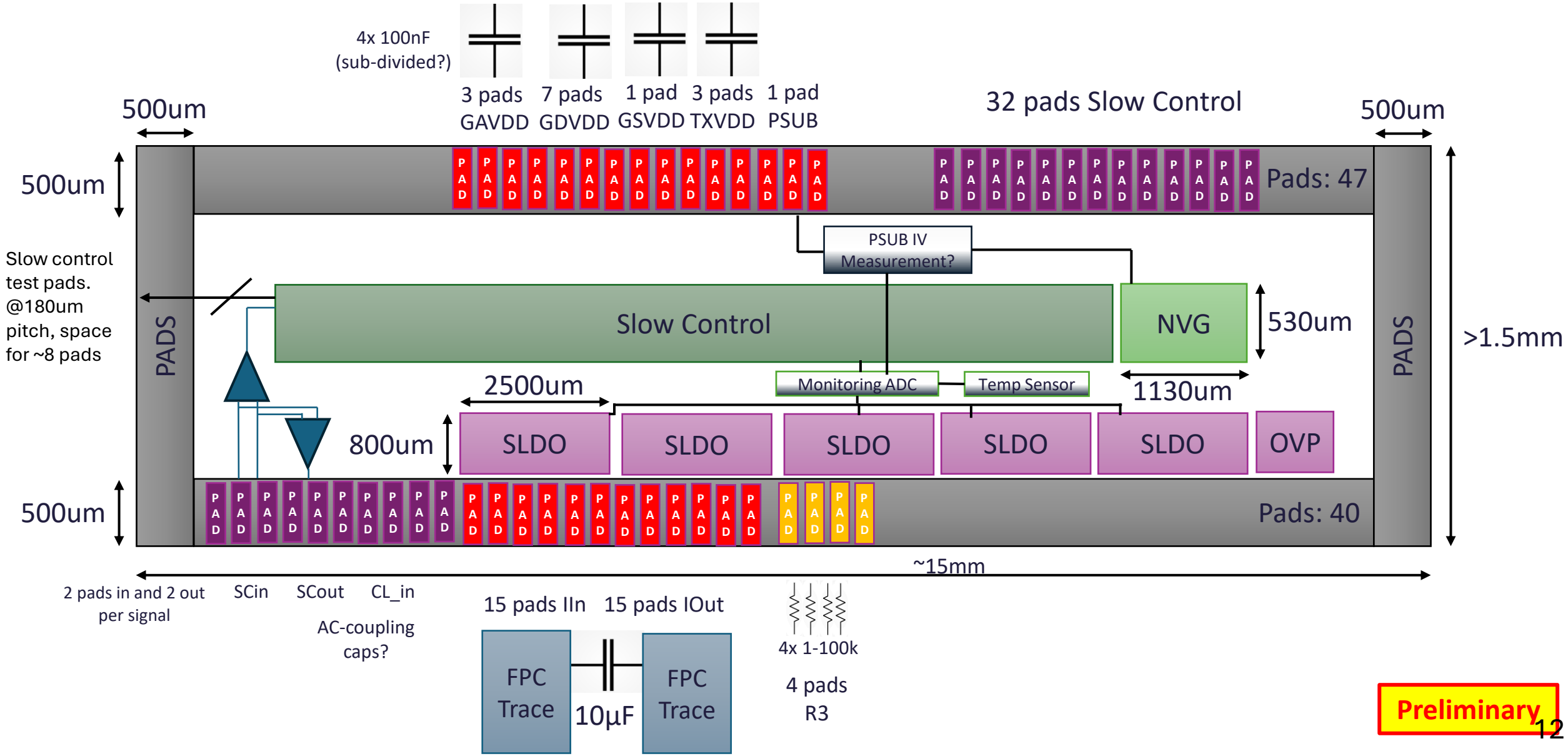
Ongoing design / simulation; hardware emulation, c.f. https://indico.bnl.gov/event/28216/contributions/109420/
Target MPW3 submission to Xfab this September /November.

Iain Sedgwick (RAL)

Current AncASIC Plan



Preliminary

Summary of Key Points

- ER2 submission imminent (aiming for the 2nd week of Jully)
  - ER3 (production) submission scheduled ~1 year after ER2 submission
- EIC-LAS Sensor Development (~7 months)
  - Reduce LEC to one channel
  - Bypass Serializer LDOs
  - Final integrity checks and tape-out
- Importance of Agreement for Access to the MOSAIX Database
  - Full access to all technical details is still pending
  - Work on EIC-LAS cannot begin until database access is available
  - Accurate estimates of the effort and timeline for EIC-LAS modifications depend on complete technical information

Ivan Amos Cali (MIT)

WAFER PROBING STATION at CERN

- MPI TS-3500 SE Automated test system
  - Installed at CERN in the DSF (Departmental Silicon Facility) lab

- Main specifications:
  - Designed to be able to load up to 300 mm (12”) wafers
    - **Micro-holes (200 um) chuck for thin wafers handling**
  - RF setup with possibility to test up to 110GHz and beyond
  - Several cameras installed: wide, **chuck, off-axis (vertical probing)**, VCE
    - Automatic Probe To Pad Alignment compensation
  - Extended probe card holder (see later)
  - Wafer wallet could be added for fully automatized process

- Goal:
  - **Commission test setup before being distributed to the institutes**
  - Test all the ITS3 ER2 wafers + (N) SVT ER2 wafers
  - Participate in the SVT production testing

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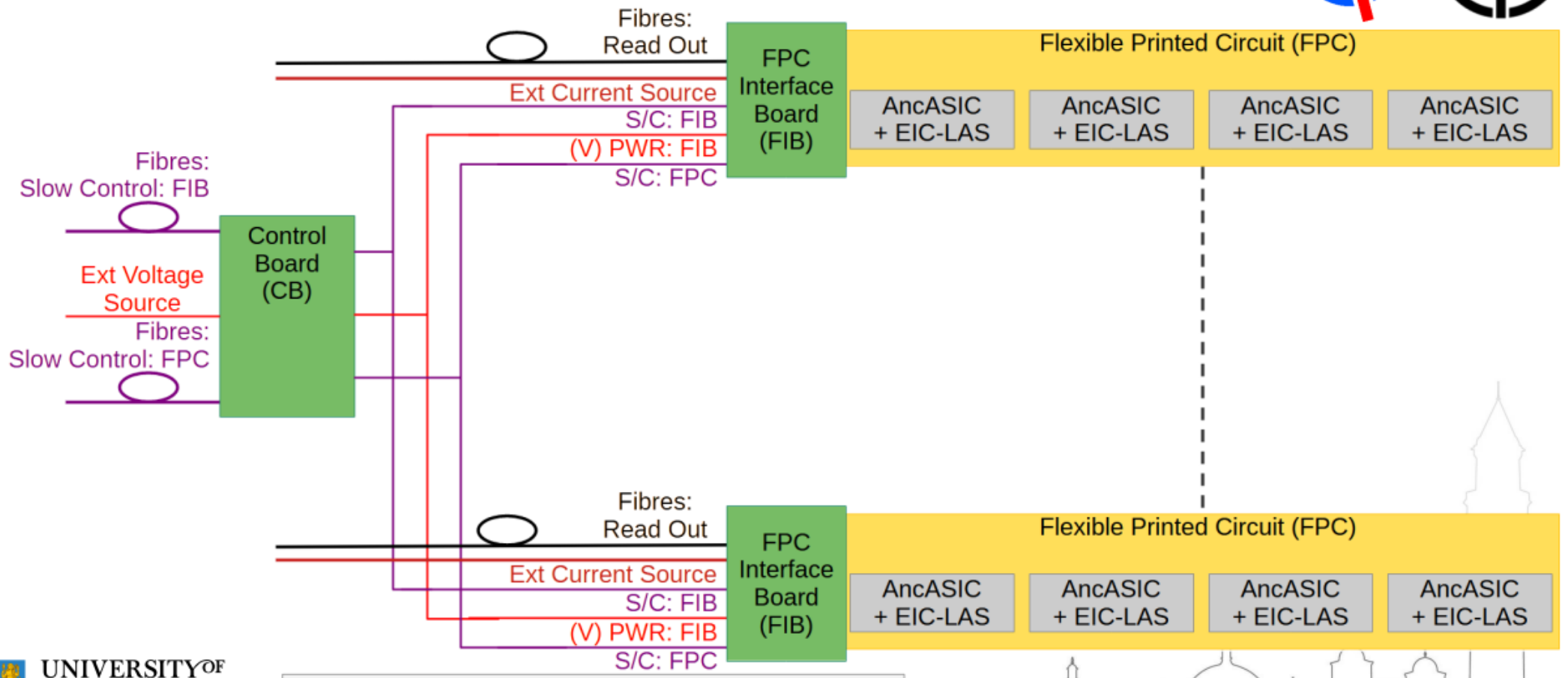
CONCLUSIONS

- Prototype probe card with vertical probe technology **fully validated**
- Design of MOSAIX probe card well advanced for single/multi point
- Design of MOSAIX/LAS probe card for multipoint still under discussion
- Probe card holder design for concept design 1 ready

James Glover (U. Birmingham)

New OB/Disk Readout Architecture

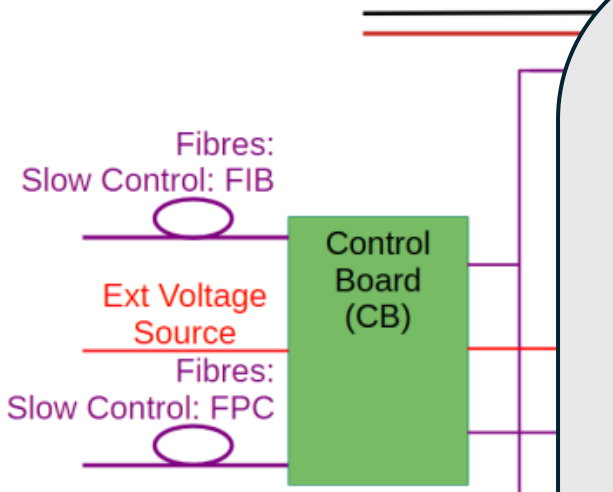


UNIVERSITY OF BIRMINGHAM

See the internal FIB and CB designs in backup.

James Glover (U. Birmingham)

New OB/Disk Readout Architecture



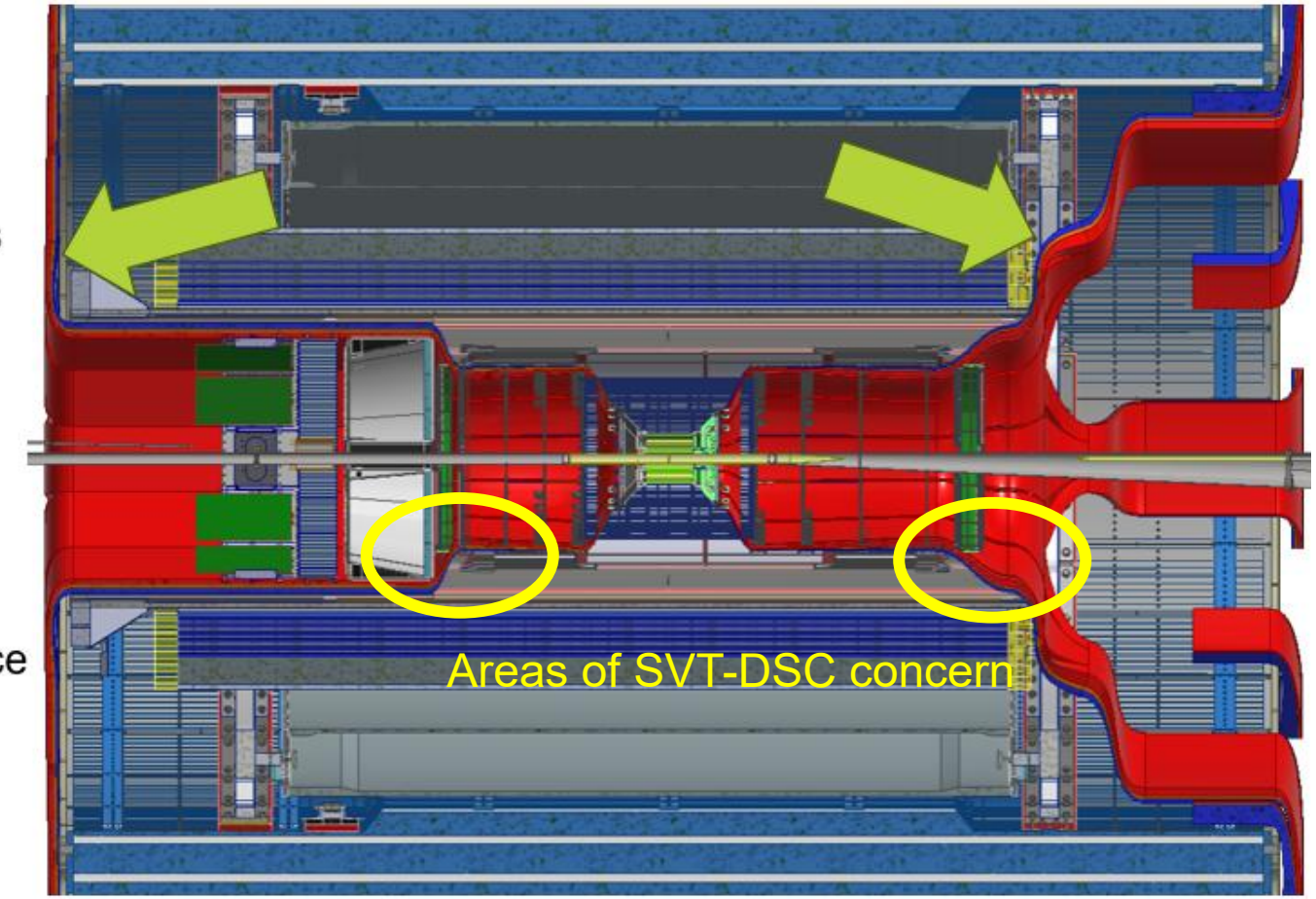
What has changed?

- Previously planning (hoping) to send S/Cs for as many VTRx+ (FIBs) as possible – utilise most of the 16 e-links of a lpGBT.
- Has become clear that VTRx+ I^2C is very specific, and communication will only work via the (3) I^2C master ports of a lpGBT.
- This greatly reduces the number of VTRx+ (FIBs) controllable by 1 lpGBT – if a 1:4 serial multiplexer is used:
  - Reduces from 1(lpGBT) : 48(VTRx+) (assuming 4 e-links reserved for onboard use).
  - To 1(lpGBT) : 12(VTRx+).
- Now, both FPC-CB and FIB-CB would be 1(parent) : 12(children) boards.

Roland Wimmer (BNL)

Planned Disconnect Locations

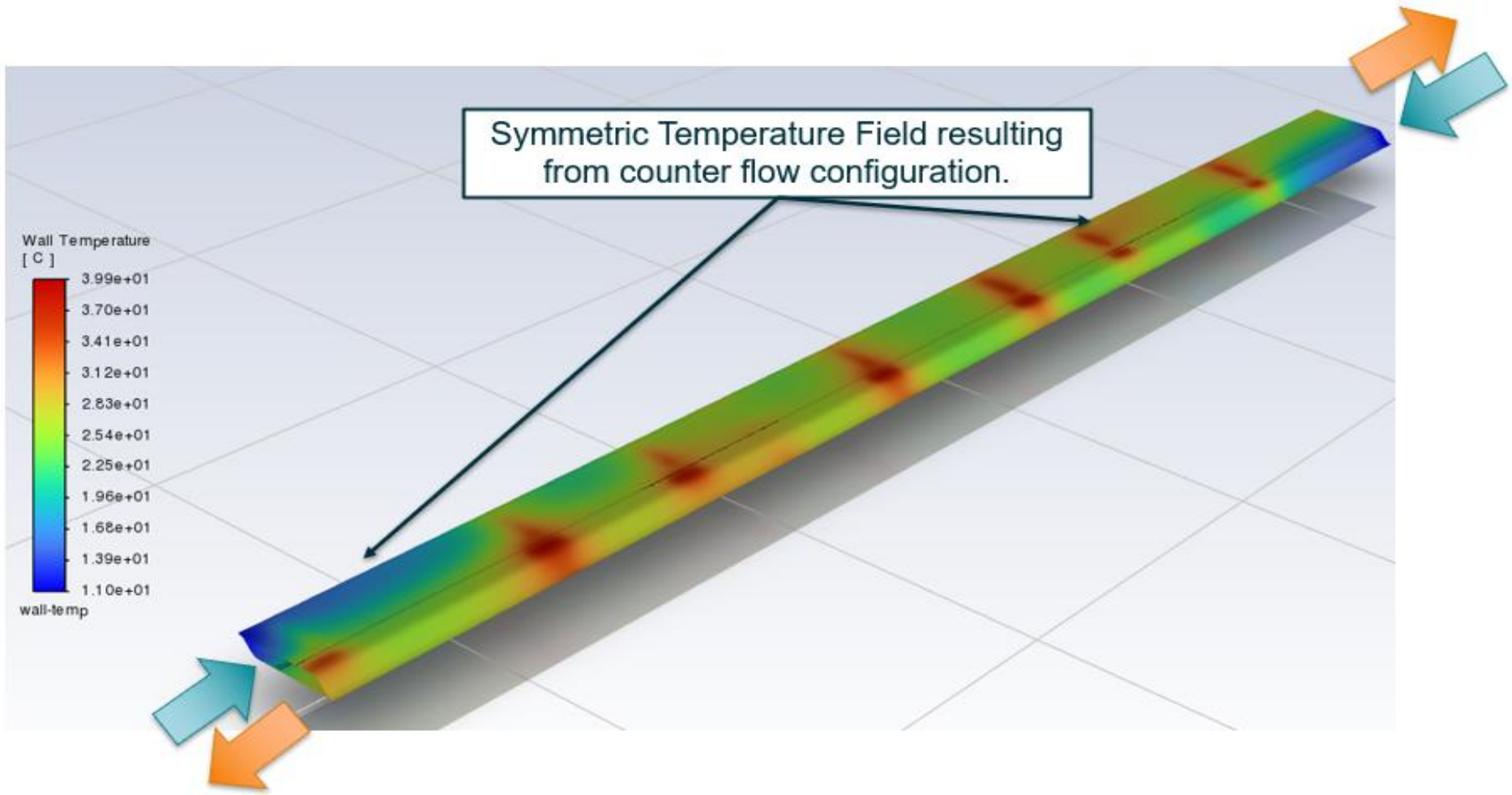
- Planning on having 1 disconnect location on each side of the detector
- Backward disconnect will be just past the DIRC electronics
- Forward disconnect will be between the barrel EMCAL and the dRICH
- These are the 2 “earliest” locations with potentially enough space for connectors
- Rule of thumb is connectors take twice the amount of space as the cable itself. Finding enough space will be extremely difficult



Ongoing effort to finalize SVT service needs / envelopes; addres current oversubscription of currently available space in electron endcap,
SVT general meetings past July 22 (grounding) and tomorrow; WP4+WP6 meetings – work in progress; none of these are to be taken standalone as a final word.

cooling

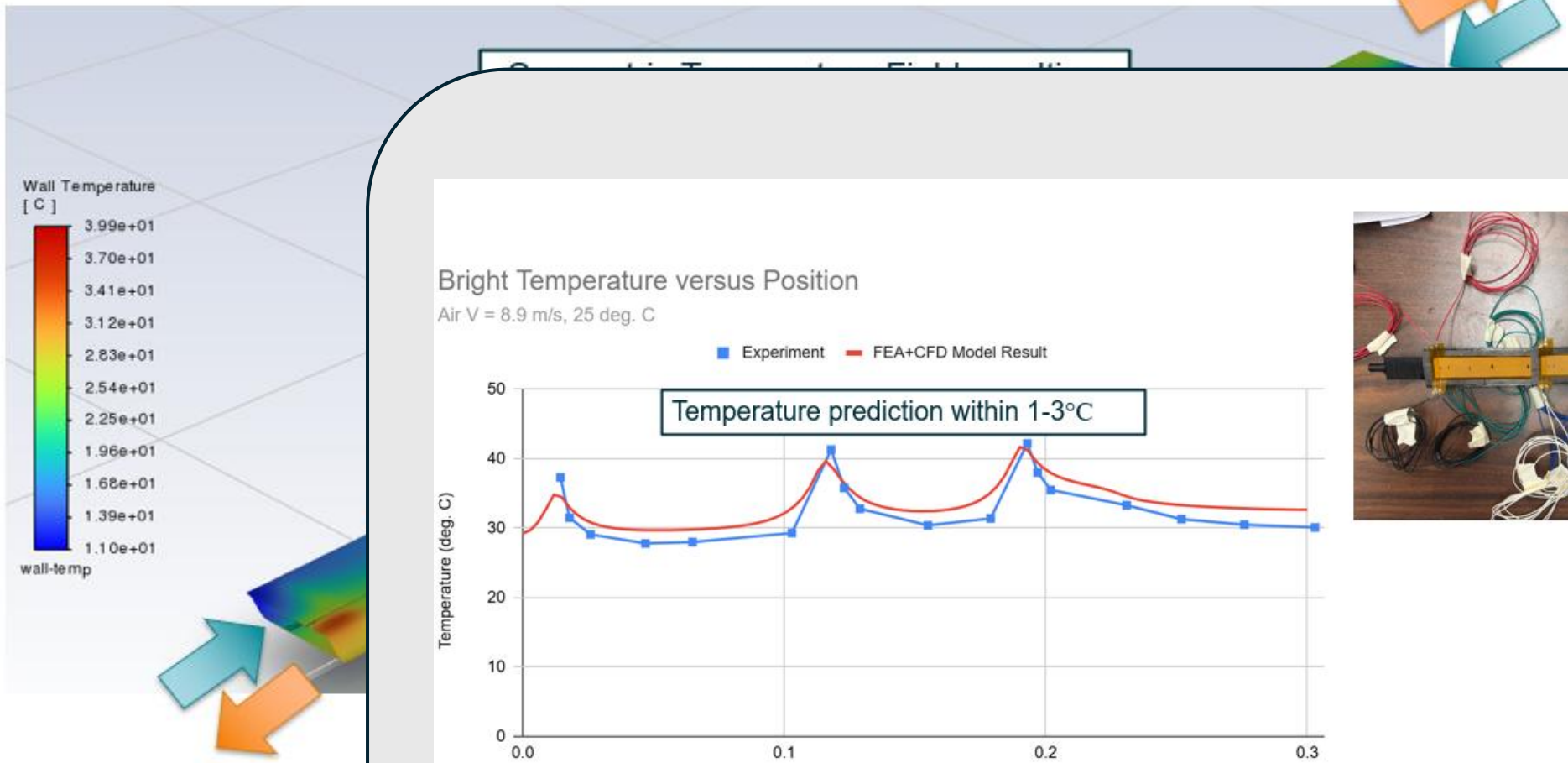
Nick Payne (LBNL)



Scaling up thus far local CFD / FEA calculations for heat loads – shown here are channels of a disk

cooling

Nick Payne (LBNL)



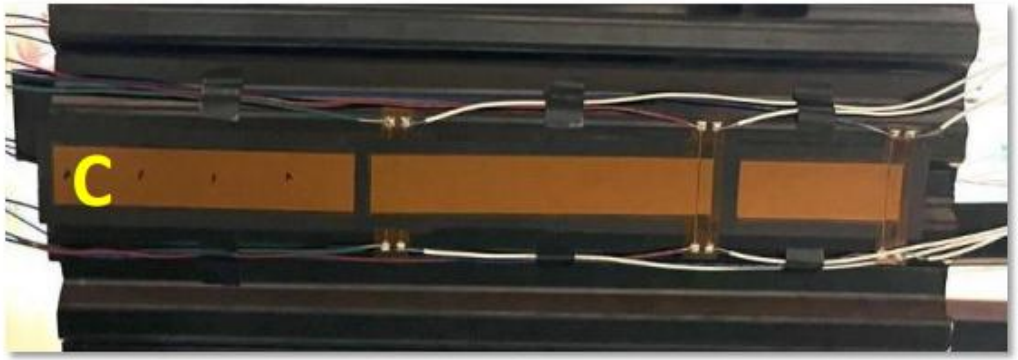
Scaling up thus far loc

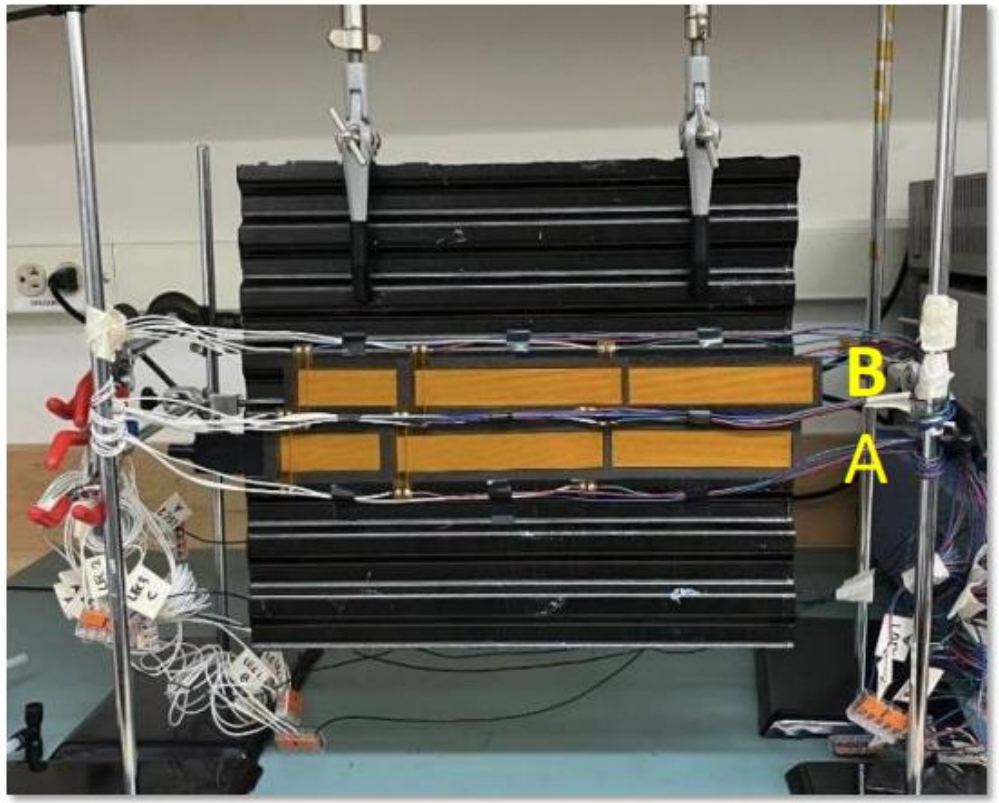
Confronting the modeling with bench-test data

Nicole Apadula (LBNL)

New thermal test piece

- Test proximity to neighbors
- 2 populated rows on the front
- 1 populated row on the back





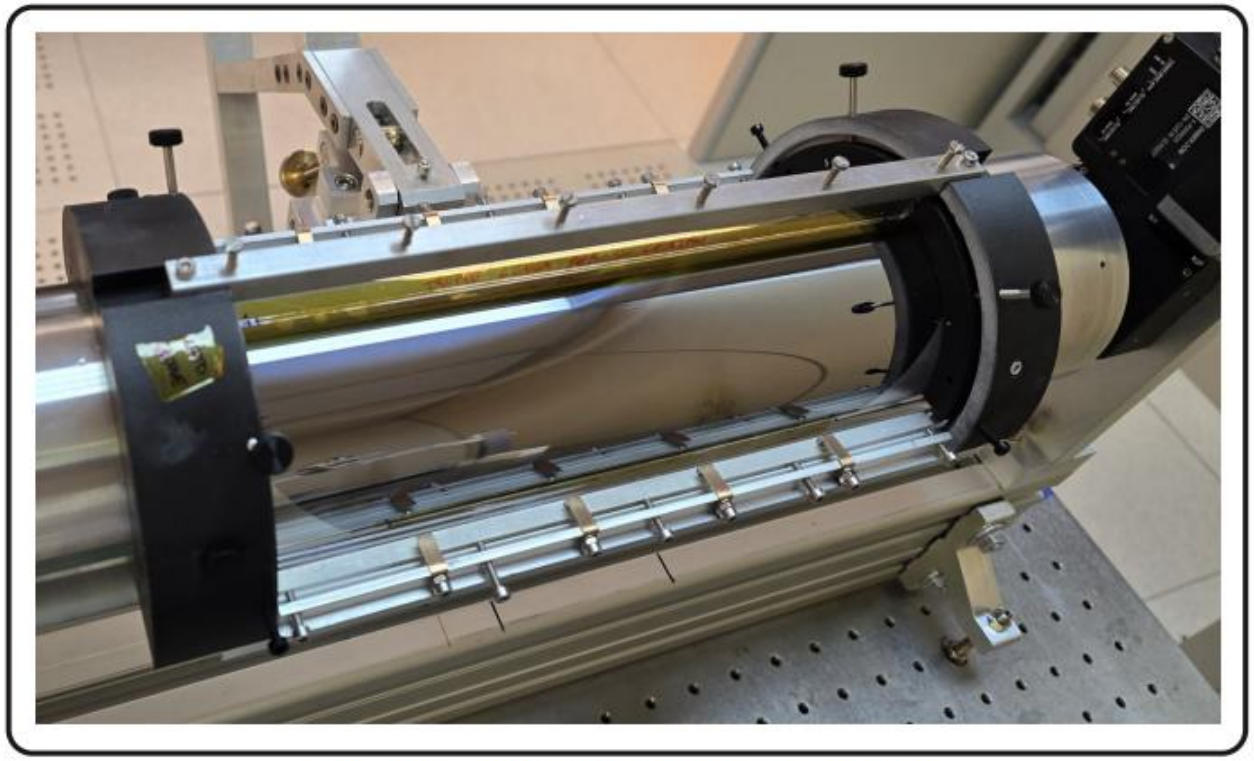
Credit: Katie Gray

Inner Barrel

PRESENT STATUS AND FUTURE ACTIVITIES

L0-L1 assembly procedure

- Sensors alignment and joining
- Joint sensors bending
- FPC to joint sensors interconnection
- Local support structures gluing
- Services integration in layer
- L0-L1 half-barrel assembly
- L0-L1 half-barrel integration to L2



Local support gluing tools rapidly evolving toward final requirements

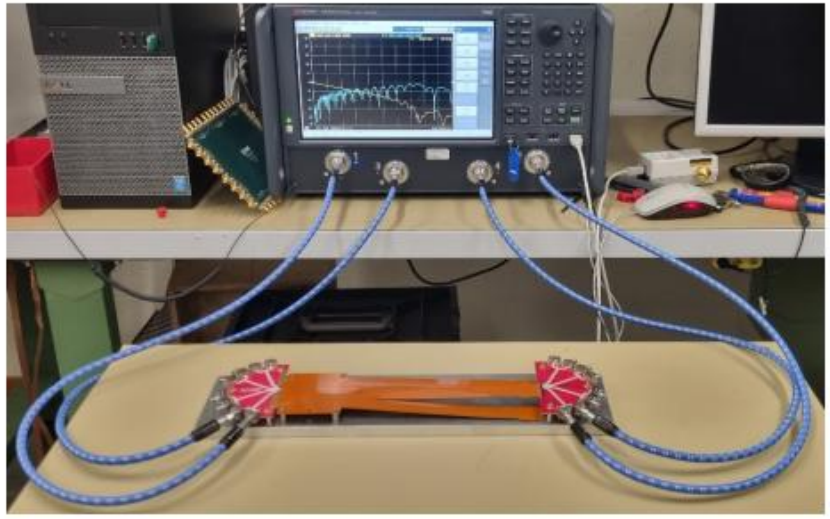
Domenico Colella (Bari)

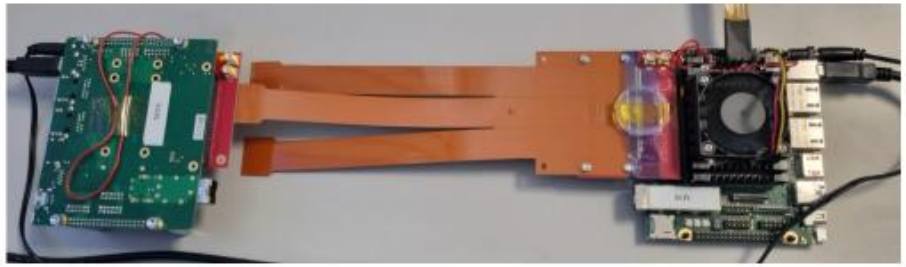
PRESENT STATUS AND FUTURE ACTIVITIES

Flexible Printed Circuit

- FPC development activities
  - Design and production of test pieces, selection of aluminium based technology
  - Development of procedures and tools for FPC bending and interconnection to the sensor
  - Qualification tests of flat and bent FPC test pieces
    - Mainly signal integrity tests of high speed links at 10.24 Gbps - S-Parameter measurement (VNA), eye diagram (High speed scope), BERT (FPGA)

- Ongoing and planned activities in 2025
  - Ongoing discussion with LTU and Daresbury for the production of simple FPC test pieces - 25 cm long, differential lines
  - Commissioning of setup and first signal integrity tests of ITS3 FPC (flat configuration)
  - FPGA boards, adapter boards and ITS3 FPC prototype acquired





ITS3 FPC test setup and interconnections

Georg Viehhauser (Oxford)

Bonding trials

- Wire bonds:
  - Sensor to module carrier/bridge FPC
  - AncASIC to module carrier/bridge FPC
- TAB bridge FPC to main FPC
- Bonding tests (using prototype FPCs from LTU)

TAB:

Lessons learned:
- Alignment important (to 50 µm)
- Reducing step height important

Wire bonding:

- Different aluminium foils
- No major difference in bonding behaviour
- Required parameter adjustment beyond standard settings
- Foil bond strength showed higher variation compared to gold board
- Back support critical

- Optimisation ongoing

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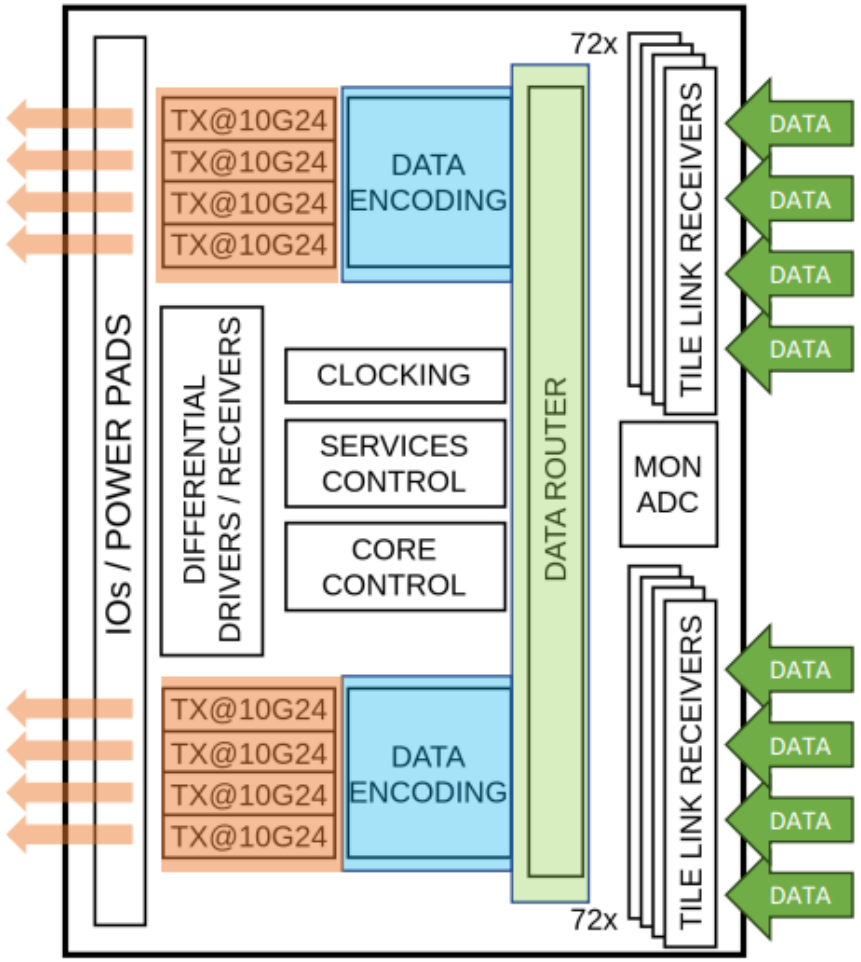
MOSAIX to EIC-LAS : LEC Modifications

- Reduce LEC to one channel
  - Bypass Serializer LDOs
    - Study on the performance before and after removing LDOs.
    - Dedicated decap cells, star routing (supply), and functional adjustments (no LDO controls).
  - Data **Encoding** and **Router** (serialization of the data to a single channel)
    - Challenge to adapt/change
    - Slow control needs to be modified



Simulations

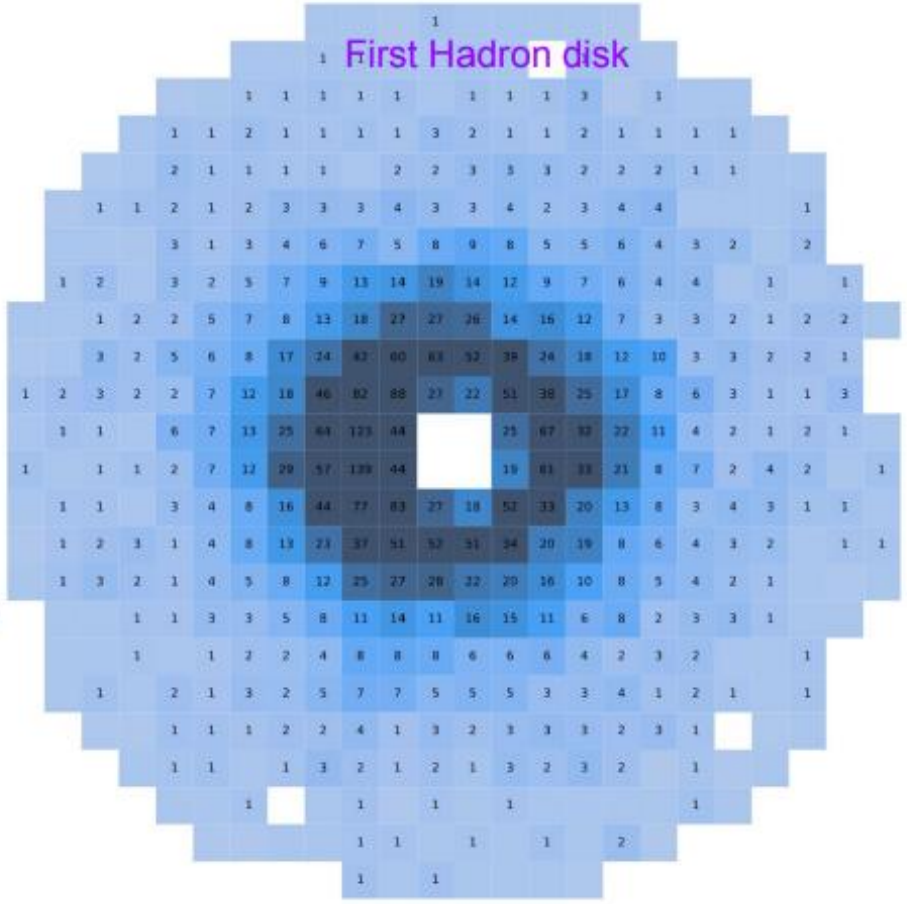
Beam Background Impact at Hit Level

Hits from charged beam particles:
plot digitized hits (edep > 0.54 keV) for each SVT surface
→ check number of hits per 2cm x 2cm square (size of RSU)

→ show result in **ms** (500 x 2us slices)

Hits distribution on disks

- x v.s. y, one square = one RSU
- First Hadron disk : max=135 hits / ms
- All disk hits:
  - distributions are similar: high density near the beampipe
  - Max hits=195/ms on H-disk 3



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Tracking with background covered (also) in the recent EICUG / ePIC Collaboration meeting, see e.g. Barak Schmookler's overview -- https://indico.jlab.org/event/934/contributions/17080/

Important caveat – SR was not correctly mixed into the background sample, c.f. Sakhib Rahman in past Tuesday's Physics and Detector Simulation meeting – https://indico.bnl.gov/event/26993/

Closing Comments

Productive SVT 3-day working meeting at SBU -- materials at: https://indico.bnl.gov/event/28216/

Multiple topics not covered in this summary, e.g.

Global assembly – PST installation concept and integration in ePIC (Sushrut Karmarkar, Thu),

MOSAIX mockup board, e.g. for “ancBrain” emulation and steps towards chain tests (Jo Schambach, Fri),

QCD science / displaced vertices (Bishoy Dongwi, Fri),

Many thanks to everyone who participated, and to CFNS for hosting us.

Active follow up, bi-weekly SVT general meetings – Tue at noon, https://indico.bnl.gov/category/496/; SVT WP4 + WP6 meetings,

Next meeting of this kind in ~6 months; initial planning started.

References

Recent overviews:

- 10th Detector Advisory Committee meeting – SVT talks by Joao de Melo, Iain Sedgwick, Ernst Sichtermann, c.f. https://indico.bnl.gov/event/26584/
- 2025 Detector R&D Day – SVT talk by Laura Gonella, c.f. https://indico.bnl.gov/event/27200/

January 2025 SVT workfest at the ePIC collaboration meeting, c.f. https://agenda.infn.it/event/43344/

July 2025 SVT working meeting, c.f. https://indico.bnl.gov/event/28216/

SVT top-level indico: https://indico.bnl.gov/category/496/

Main mailing list: https://lists.bnl.gov/sympa/info/epic-svt-ib-l

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