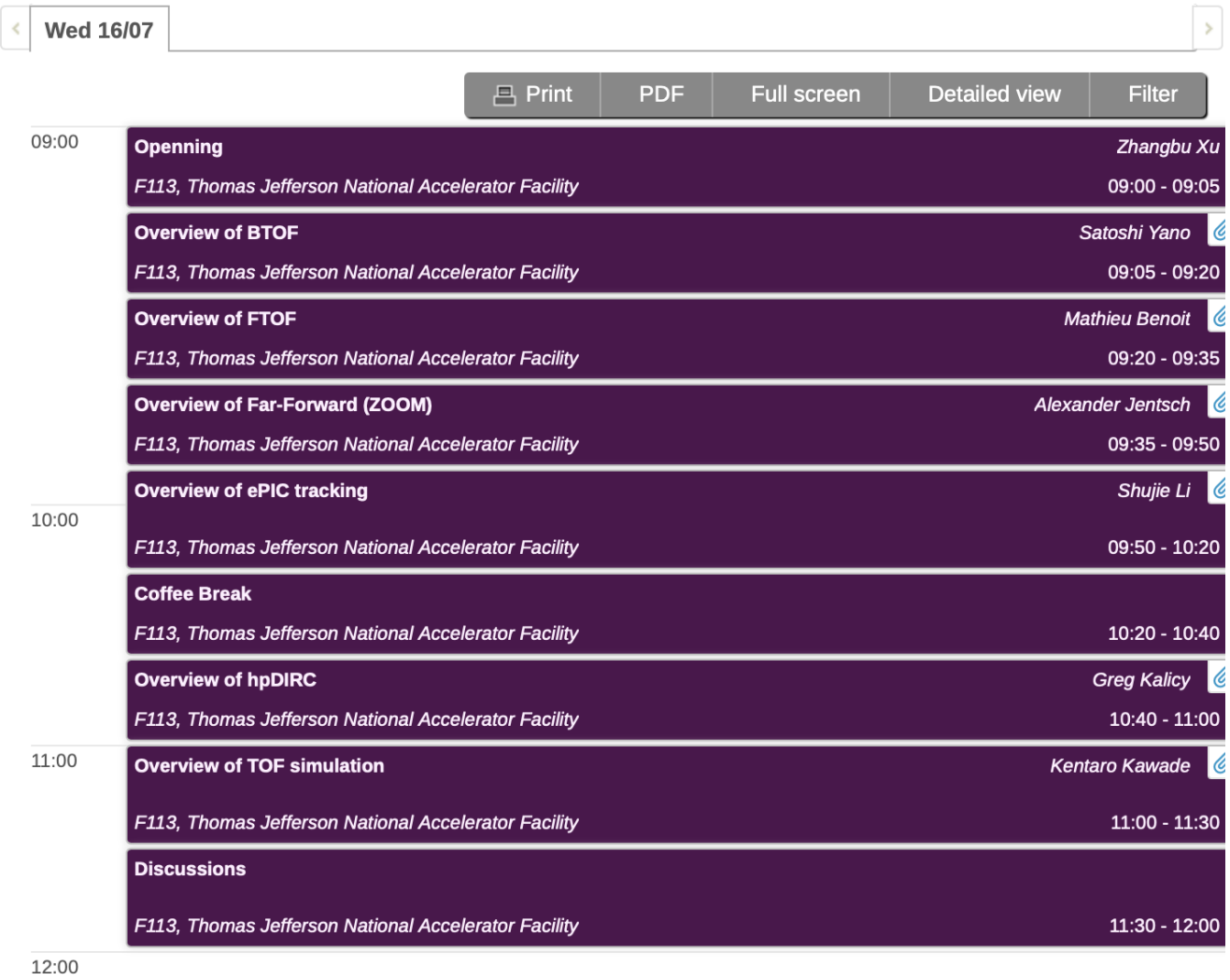
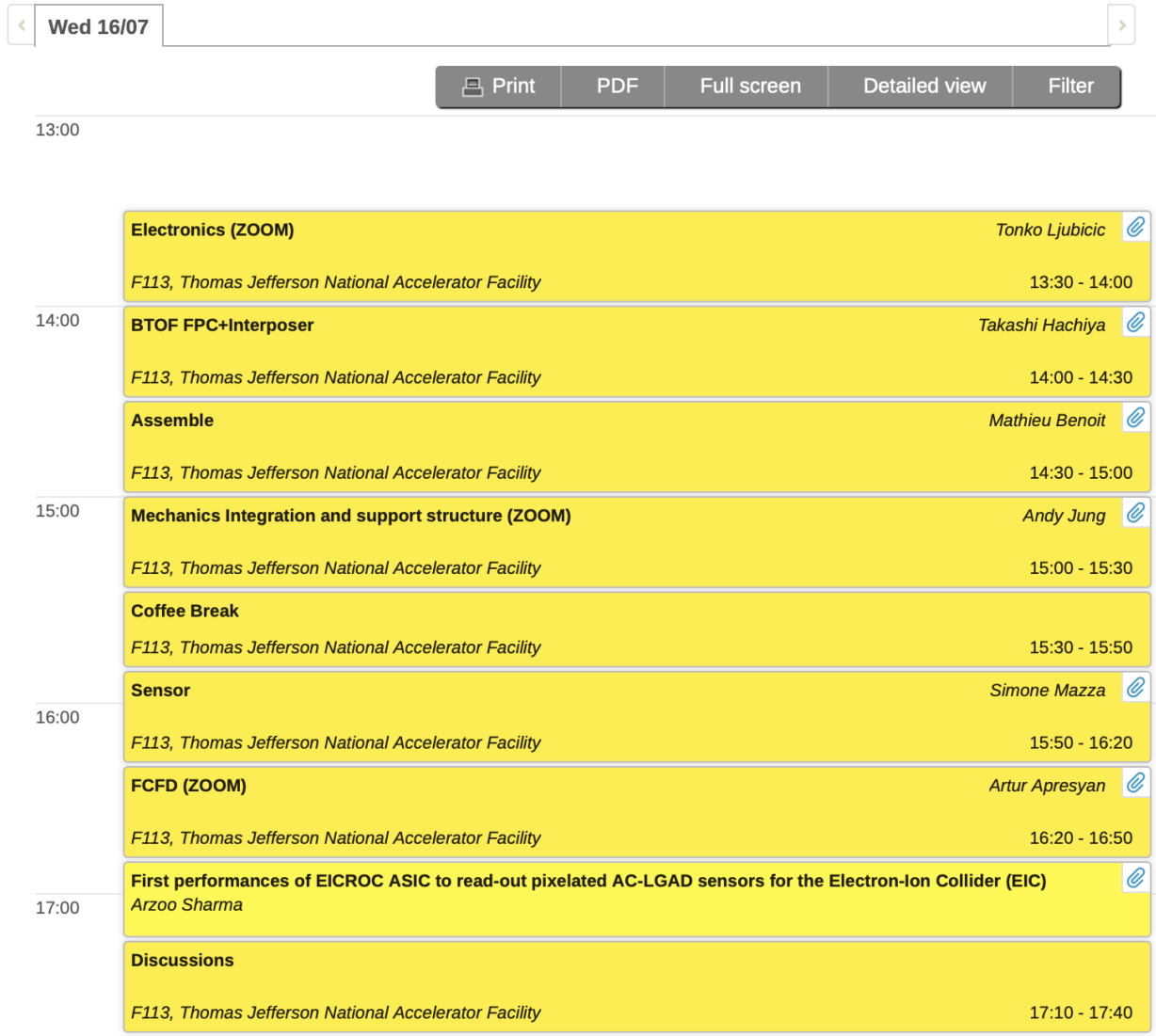
Summary of AC-LGAD Workfest 07/17/2025

Zhangbu Xu for TOF DSC

Full-day meeting agenda

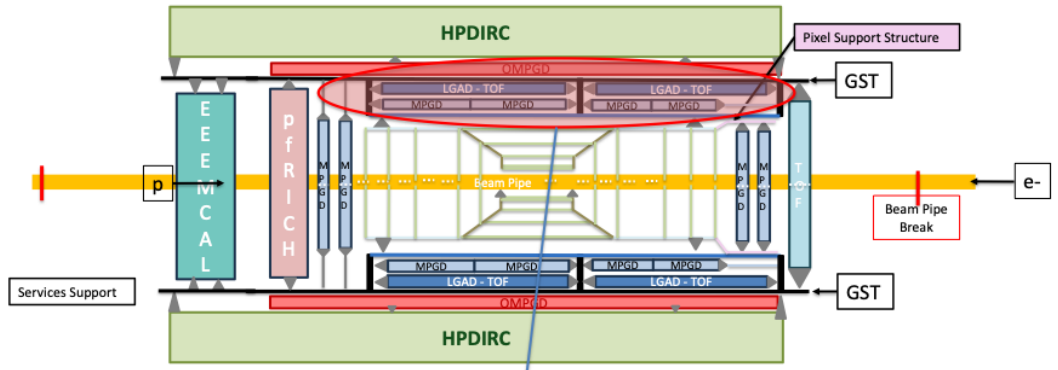




Mechanics, supports and services

Andy Jung (Purdue)

Global Support Tube / GST

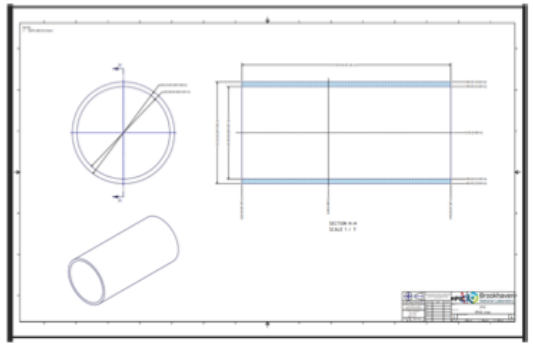


- ePIC Detector Support Hierarchy Y-Z View
- Presumed latest version, Jan 2025.
- Since May 2024:
  - GST extended beyond EEEMCal, support discussed

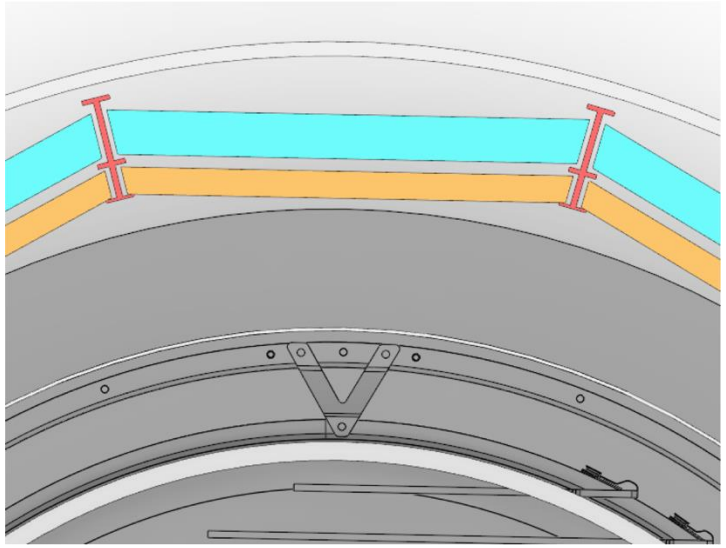
- Significant changes to achieve serviceability & ease maintenance
- Closer to the original bTOF support I suggested back in 2023
- No engagement rings anymore but "bTOF trays"

TOF assembly

- The TOF and Cymbal will be segmented in 12 sectors along the r-phi plane inside the GST.
- This will enable installation and removal of the TOF + Cymbal sectors
- This is a second degree envelope model with interfaces for both the AC-LGAD barrel* and the Cymbal barrel mounts as positioned in the 12 sectors.
- This design allows for complete coverage in r-phi plane
- There will be some split / loss of coverage in the z which is unavoidable. (originally was 5mm due to engagement rings – still on that scale)



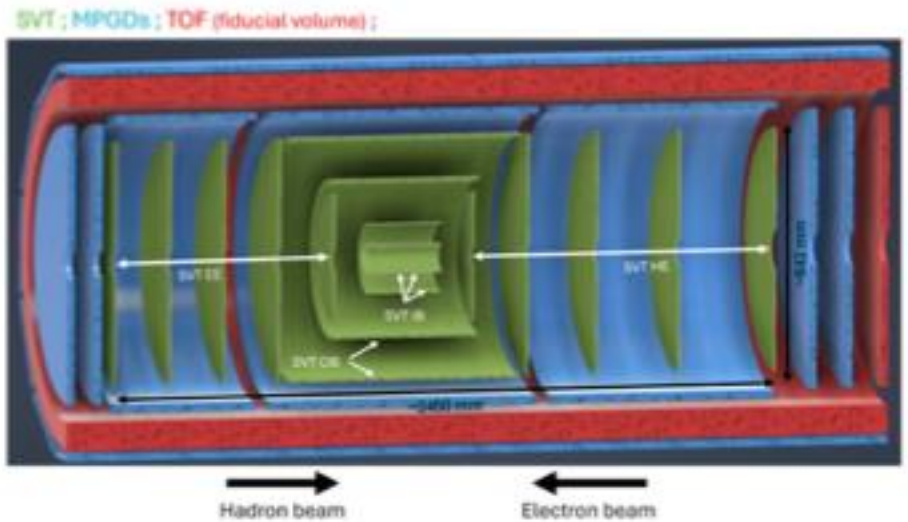
From Dan's envelope model March_2025



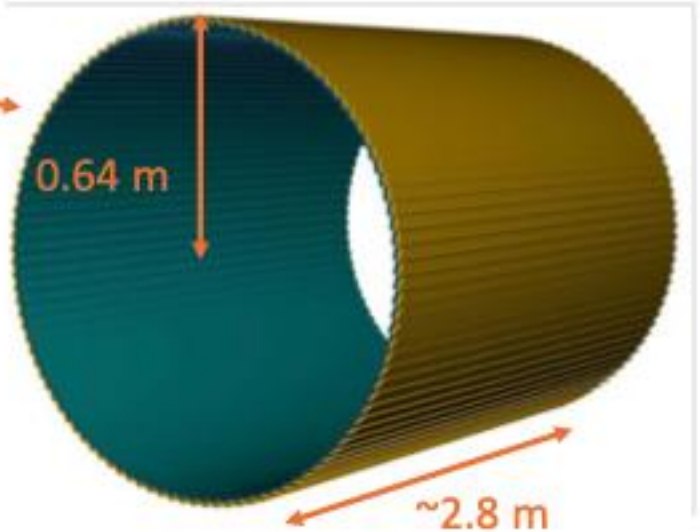
- Significant changes in global support structure for TOF
- Eliminate engagement rings
- Introduce trails
- 12 (east and west each) TOF trays bundled together with Cymbal
- Each tray can be serviced independently
- Services still run on both ends
- Retrieve trays only from hadron side (forward)
- Need final structure and tray design

Recap of Barrel-TOF

Satoshi Yano

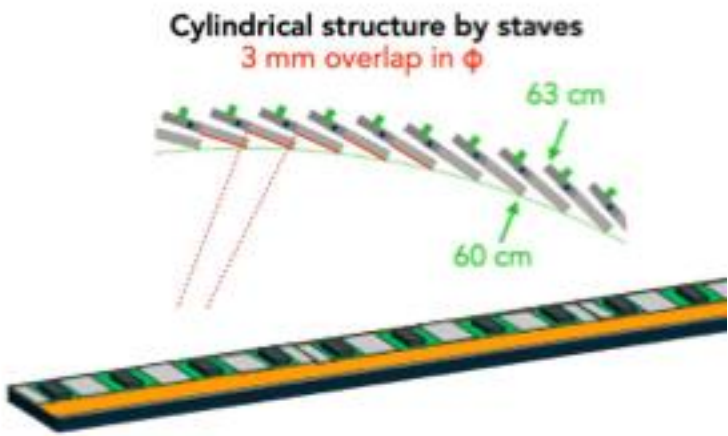


Barrel-TOF (BTOF)



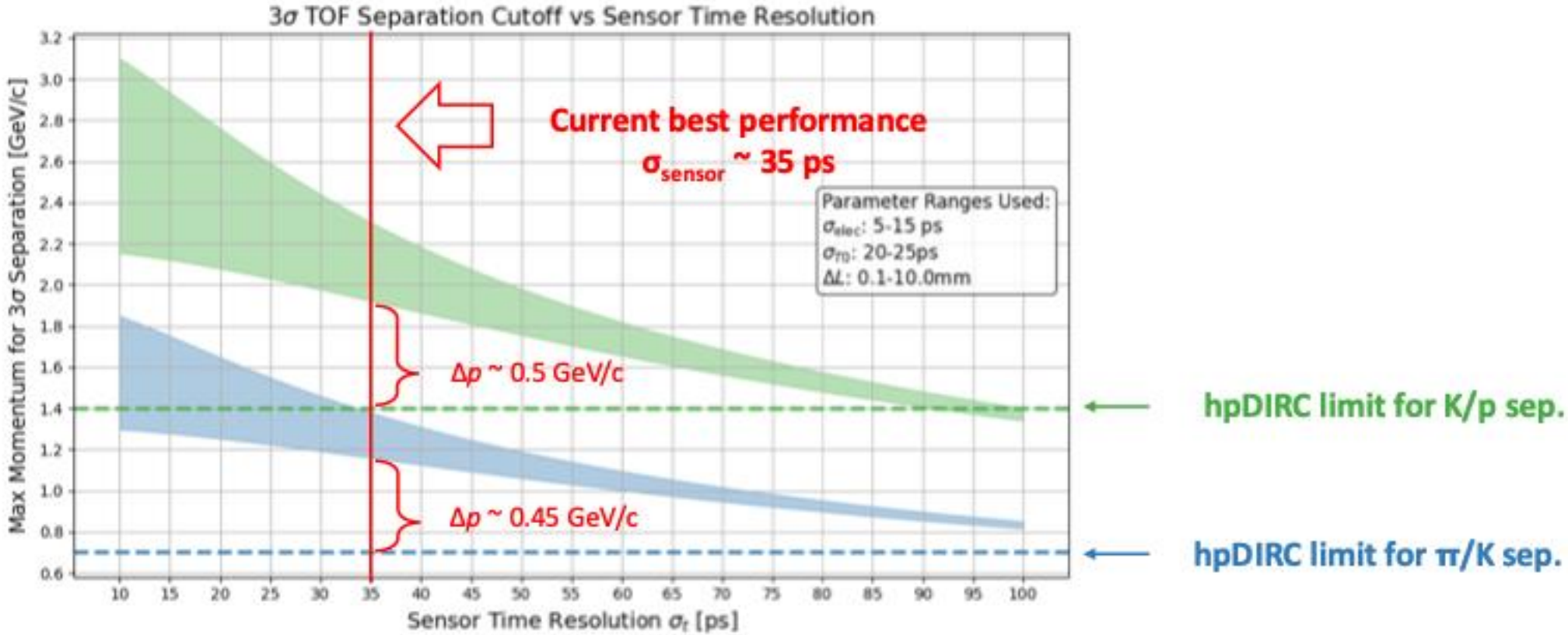
-1.33<η<1.74

144 x Staves



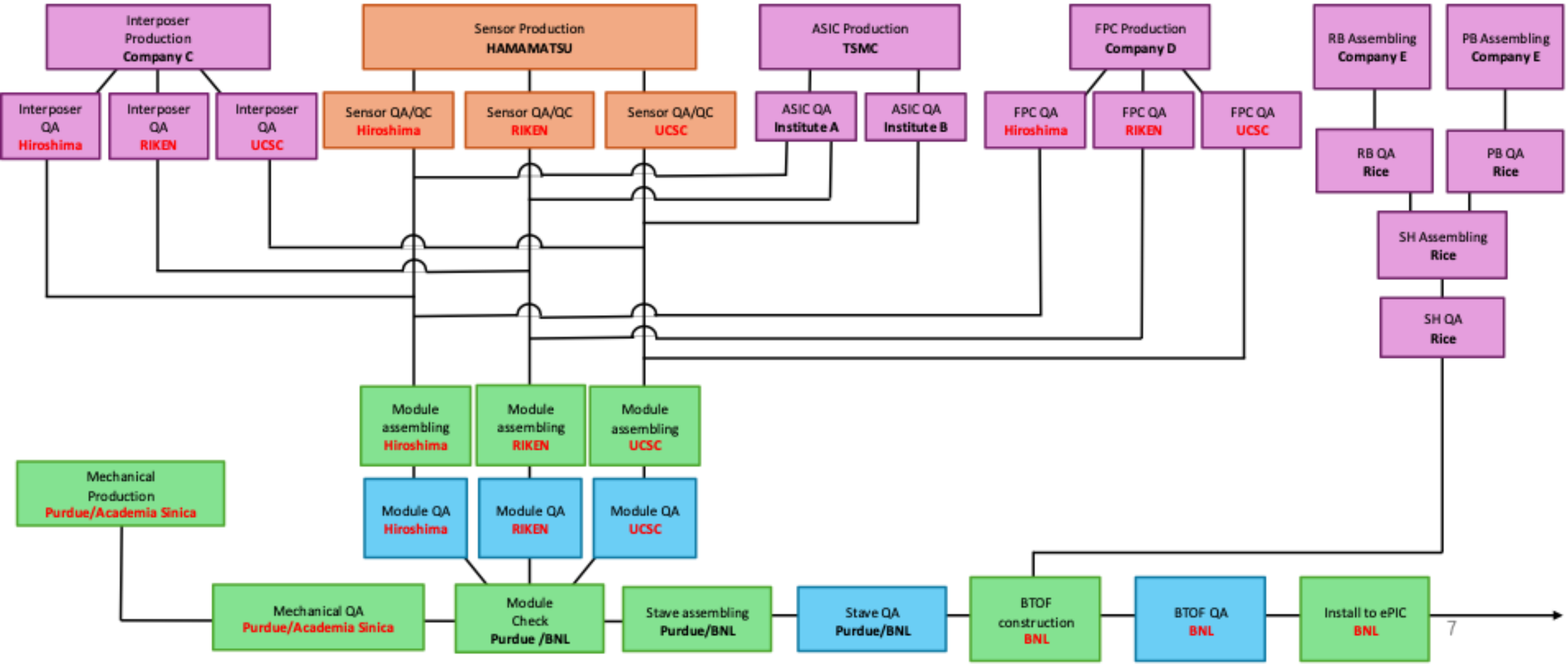
- The ePIC AC-LGAD TOF is PID, tracking and background rejection detector for mid-rapidity (BTOF: -1.33<η<1.74)
- Cylindrical shape is composed of 144 tilted staves (288 half-staves)
- Strip-type AC-LGAD sensor is used to meet the requirement of ~35 ps and ~30 um timing and spatial resolution respectively

Sensor Timing Resolution v.s. Overlap with hpDIRC



- Even in the worst case scenario, with current sensor performance (σ_{sensor}~35 ps), there is an overlap area with hpDIRC → **Already no PID hole!**
- σ_{sensor}> 90 ps doesn't have overlapping region with hpDIRC in K/p separation any more

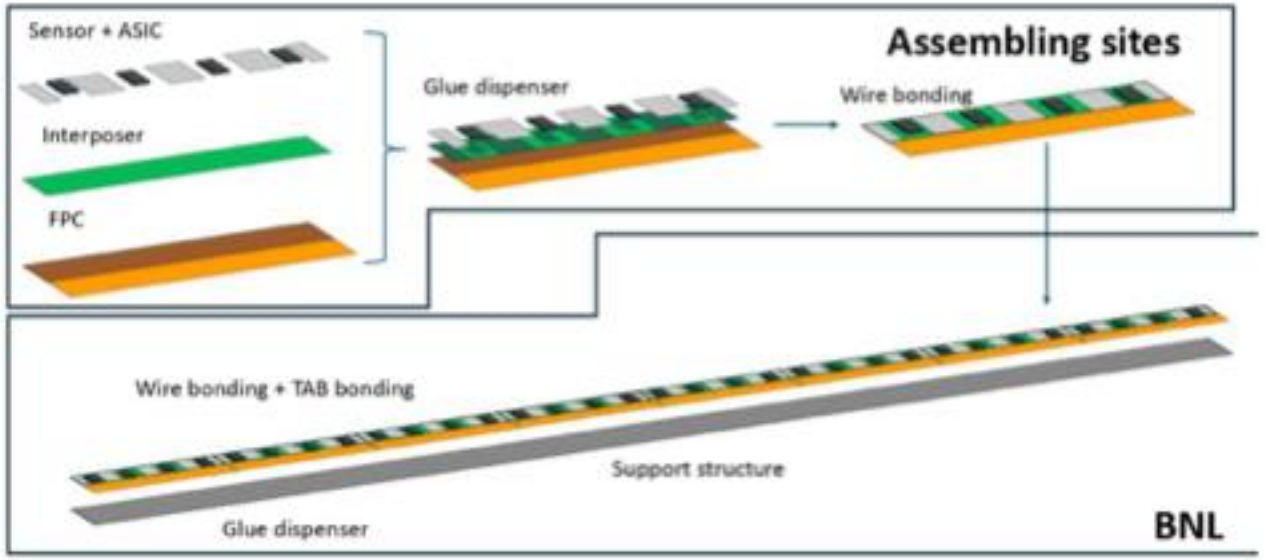
Detector Assembling Workflow

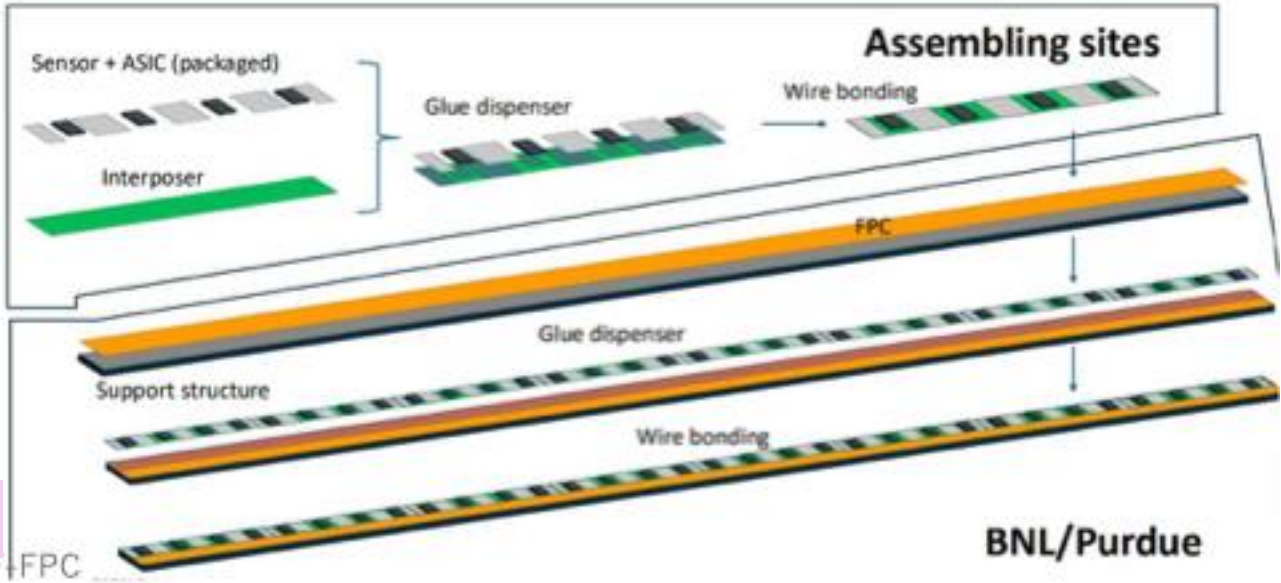


Things to make very long FPC & interposer

- **Length : 135cm x 6 cm**
  - The structure is similar with INTT's bus extender (max 130 cm), ATLAS-ITK FPC (135cm)
  - How to make it? Is it feasible?
    - One large FPC? Connecting short FPC?
    - If connected, how? What about TAB bonding?
    - If long, can we make it?
- **All in FPC**
  - Signal lines/HV/LV/GND in FPC
- **N signal lines in FPC?**
  - Depends on ASIC, ~200 lines from 32 ASICs ?
  - N layers of FPC ? , Based on our experience from the INTT, signal layer should be one for the yield rate
- **Signal transmission quality**
  - 640Mbps by lpGBT-> impedance control necessary

Takashi Hachiya (Nara Women's University)



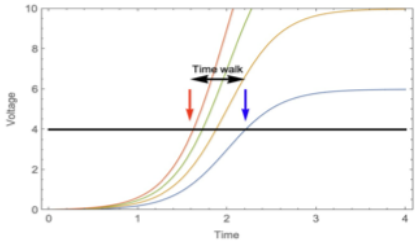


25cm demo-prototype, design on connection to SH started

FCFD design for BTOF

Introduction

- A robust fast-timing measurement technique for LGADs
- CFD approach achieves excellent performance, especially for low S/N systems, such as LGADs (NIM A 940 (2019), pp 119-124)
  - CFD-based readout is much simpler in operation and maintenance
  - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc…
- Time-walk effect is well known & must be corrected for best performance
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution



FCFDv1 2023—24 proton beam test
DC-LGAD 32ps, not optimal for AC-LGAD 40—45ps

FCFDv1.1 received in June, good preliminary checks, test beam at DESY during collaboration week

Anticipated timeline

- Optimization of the analog front-end to reduce footprint, and add ADC
  - Estimate around 2-3 months
- Design of the TDC and FCD
  - Estimate around 2-3 months each, total ~6 months
- Design of the I2C
  - Estimate around 3 months
- Produce a small test chip to verify design changes and testing
  - Small chip will test the new front-end and new ADC, new TDC
  - To be submitted **by the end of 2025**

Anticipated timeline

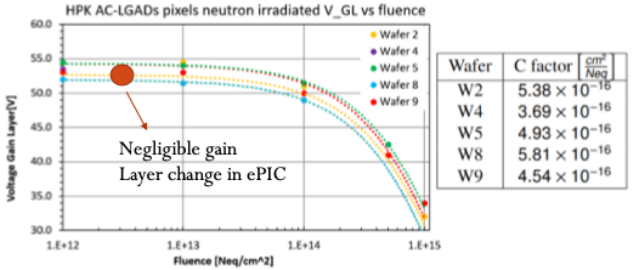
- Design of the clock and power distribution
  - Estimate about 2-3 months
- Readout
  - Estimate 5-6 months
- Integration and Verification:
  - Estimate about ~6 months, will go in parallel as blocks are developed
- Submission of the first prototype full chip : **around 10-12 months**

- Proposal is to design a 32-channel prototype as a next version
  - First full ROC, with many new components
  - Demonstrate all components of the chip, power and clock distribution, overall performance
  - Can be tested with the full system, build modules, integration, etc
  - An economical solution which allows to test most of the main questions

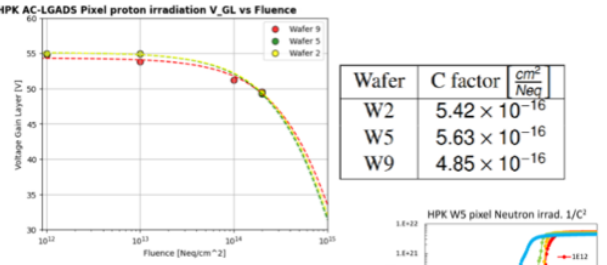
AC-LGAD sensor radiation testing an inventory

Irradiation effects on AC-LGADs

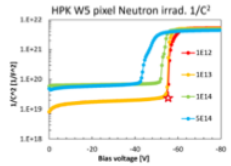
- Neutron (IJS) and proton (FNAL) irradiation on 2023 HPK production
- Up to 1e13 Neq, no significant change in sensor IV properties and gain layer doping
  - Leakage current scales with bulk volume
  - Current and breakdown voltage increases with fluence (as expected)
- Gain layer doping proportional to Vgl (gain layer depletion voltage) or 'foot' (star in the plot)
  - Degradation parameter, 'c' factor, from fit on the distribution vs fluence
- Behavior across wafers is consistent
- Comparable results for protons and neutrons
- See: https://arxiv.org/abs/2503.16658



Wafer	C factor $\left[\frac{cm^2}{Neq}\right]$
W2	5.38×10^{-16}
W4	3.69×10^{-16}
W5	4.93×10^{-16}
W8	5.81×10^{-16}
W9	4.54×10^{-16}

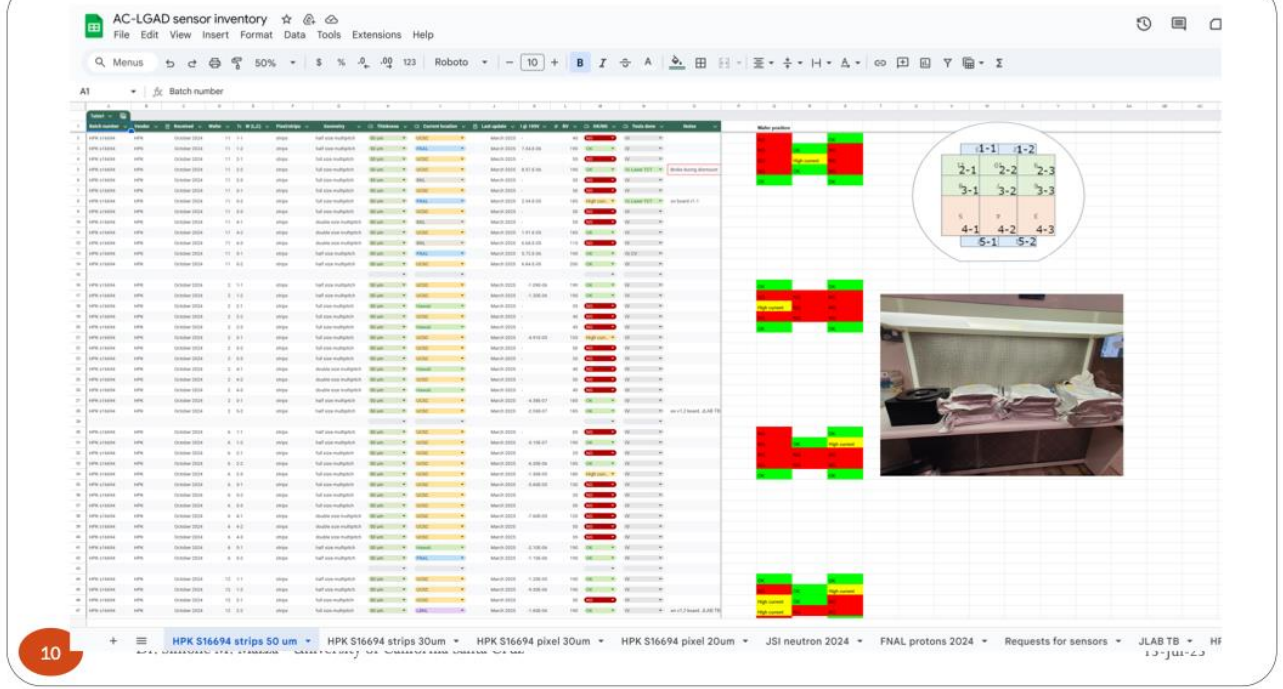


Wafer	C factor $\left[\frac{cm^2}{Neq}\right]$
W2	5.42×10^{-16}
W5	5.63×10^{-16}
W9	4.85×10^{-16}



5 Dr. Simone M. Mazza - University of California Santa Cruz

Student: J. Ding, M. Davis



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Sensors for the ePICTOF layer are reaching maturity

- Tested effect of radiation damage on AC-LGADs, no unforeseen effect observed (especially for low radiation level at ePIC)
- Received first large-scale AC-LGAD production from HPK, first results are good ? still a lot to test!
- Running a test beam here & now!
- Additional test beam planned this year at KEK for full-size sensor testing and readout electronic testing
- An additional HPK production is ongoing
- Another FBK production is ongoing, allow for another vendor characterization

Forward TOF design, assembly and schedule

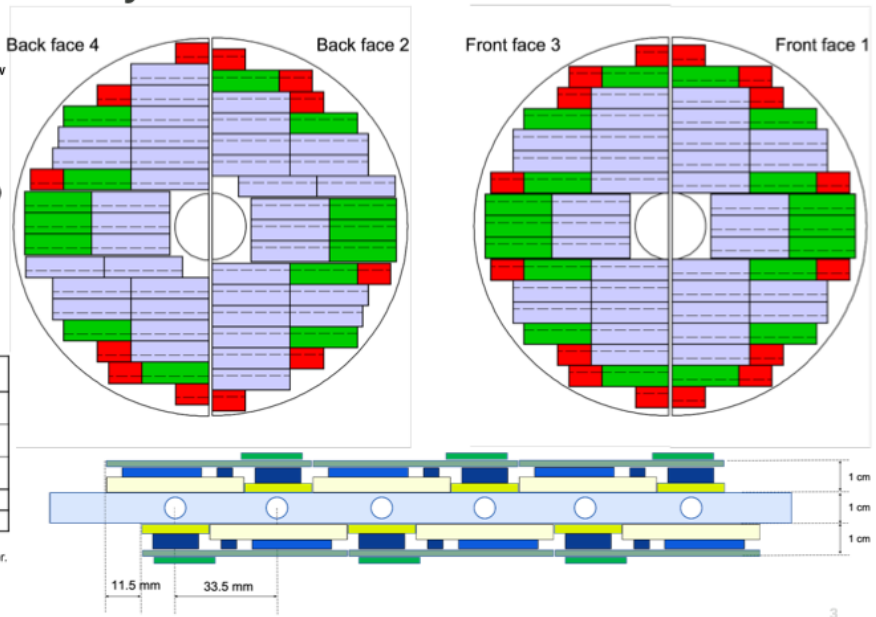
Forward TOF Detector Layout

To estimate the material budget, we consider the follow composition:
•Sensor: 300 microns (0.3%X0)
•ASICs: 400 microns (0.4%X0)
•RB and PB PCB board: 2 mm kapton (0.7%X0)
•Module PCB board: 0.6 mm kapton (0.2%X0)
•Aluminium nitride (AlN) base plate: 0.5mm (1.1%X0)
•Cooling and support: 5%X0 (Detailed design ongoing)

Total material budget is currently estimated to be: 7.7% X0

Type	FACE 1 & 3	FACE 2 & 4	Total
3 module SH	8	6	28
6 module SH	9	8	34
7 module SH	17	18	70
Modules	197	192	**778**
Sensors	788	768	**3112**

Number of Service Hybrids (SH) and modules of the detector.



OAK RIDGE National Laboratory

Schedule and baselining

Modules

- A series of 3 demonstrators planned for module assembly. The demonstrator will allow to baseline module concept and assembly procedure
  - Show-and-tell **(summer 25)**
  - Thermo-mechanical **(Q4 25)**
  - Functional **(Q2-3 2026)**
- EICROC1A/B submission waiting for final EICROC1B design, we expect availability Q4 25. EICROC2 is baseline.
- Sensor production with HPK ongoing to validate EICROC0B performance , next production aimed at final design baseline.

Service Hybrids and readout

- Power board demonstrator **in production**
  - Will allow to measure power consumption and heat dissipation
- Readout board demonstrator **designed, waiting for PED fund for production**
  - Will allow to test interface to FELIX, clock distribution etc.
- EICROC2 digital interface specification **will be required for the final design** of the boards.
- FLX-155 board identified for readout

Mechanical Integration

- The module concept defines the granularity for integration to mechanical support
- Design ramping up for disk support , **first model expected Q4 2025**
- Assembly and integration kinematics to be established along the design of the support and **refined in 2026.**

OAK RIDGE National Laboratory

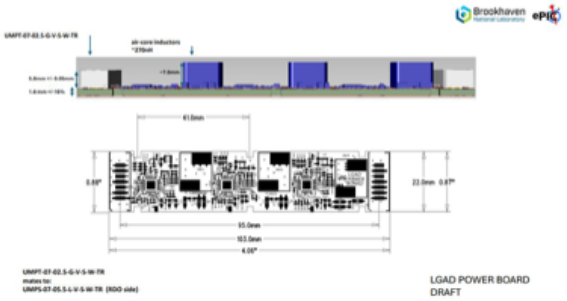
TOF electronics: readout/powerboard/DAQ

FTOF Readout Board (RBv1)

- Status
  - Schematics completed ✔
  - PCB design completed✔
  - PCB being manufactured (2 weeks)
  - Parts ordered
  - Assembled boards expected in 1 month (mid-Aug)
  - Testing (Aug,Sep,Oct)
- we used the CMS ETL Readout Board (very similar to ours) to already complete: ✔
  - DAM Streaming Firmware using our "FELIX-lite" candidate PCIe FPGA board (Alinx AXAu15)
  - develop and debug lpGBT configuration & control
    - lpGBT was in the FEC12/10Gbs mode running at the EIC-type clock of 315.2 MHz
      - 39.4 MHz recovered at lpGBT
  - develop and debug a "typical ASIC" interface to lpGBT using the CMS ETROC ASIC
- ⇒ we are ready to start debugging our RBv1 as soon as it arrives from the assembly house

FTOF Power Board (PBv1)

- PBv1 designed and started by Tim Camarda (BNL)
  - responsibility moved to Steve Boose (BNL) but with Tim's continuing help
- Recent Status from Tim
  - The power board PCBs are scheduled to ship out **in a few days.**
  - Instrumentation has the solder stencil and they say they can start when we get the boards and parts in.
  - The parts are on order.
  - We will populate **one circuit first** for testing/ evaluation.



BTOF RDO Evolution (and Power Board?)

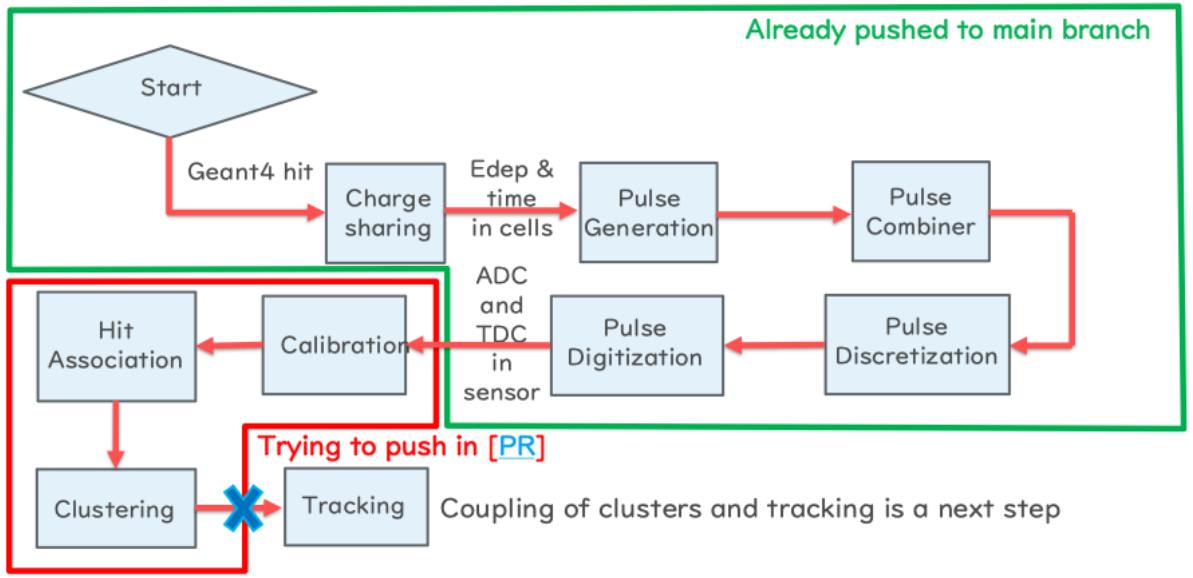
- What we know now
  - RDO will have **1 Master lpGBT** and **3 Slave lpGBTs** connected to **1 VTRX+**
  - each lpGBT will use the VTRX's TX channel
  - Master lpGBT will additionally use VTRX's RX channel for configuration and clock recovery
  - **we will connect 16 FCFD ASICs to each lpGBT** ⇒ total 64 ASICs per RDO
- What we assume now
  - FCFD ASIC: **320 Mbs data rate, 1 differential data link per ASIC**
- What we need to know
  - **external constraints on the size of the RDO**
  - other BTOF groups which are willing to contribute (apart from Rice)?
  - how are the ASICs connected? **Connector?**
    - this contributes to the size/footprint of the BTOF RDO
- Issues
  - **funding???**
  - long (~1.4m) signal traces to/from ASICs and lpGBT
    - this is something we should start testing **now**
      - clock jitter
      - signal/data integrity
      - even I2C might be problematic
  - power distribution is unknown (and Tim is gone)

Short-term (up to end of 2025)

- EICROC1 ASIC "Characterization Board" interface to RBv1 [Mike, TL, …]
  - the Test Board needs to be available first (?) as well as the ASIC (?) [Omega Group]
  - and later with 32x32 pixel sensor [Mathieu et al]
- Possibly also the FTOF-specific EICROC1 ASIC Module Board? TBD…
- William's SFP FMC with the GTU interface fiber and clocking [William, TL]
  - with GTU emulation in AXAU15
  - this enables the final clock distribution mechanism ⇒ important step
  - (I am unsure about the status – need to check)
- **TClink:** CERN's Temperature Controlled Link ⇒ required for TOF [TL]
  - CERN-developed FPGA firmware for Xilinx Ultrascale FPGAs
  - I'd like to use our FELIX-lite first to gain experience and to measure performance
- "User-quality" DAQ software [TL, others?]
  - with GUI etc

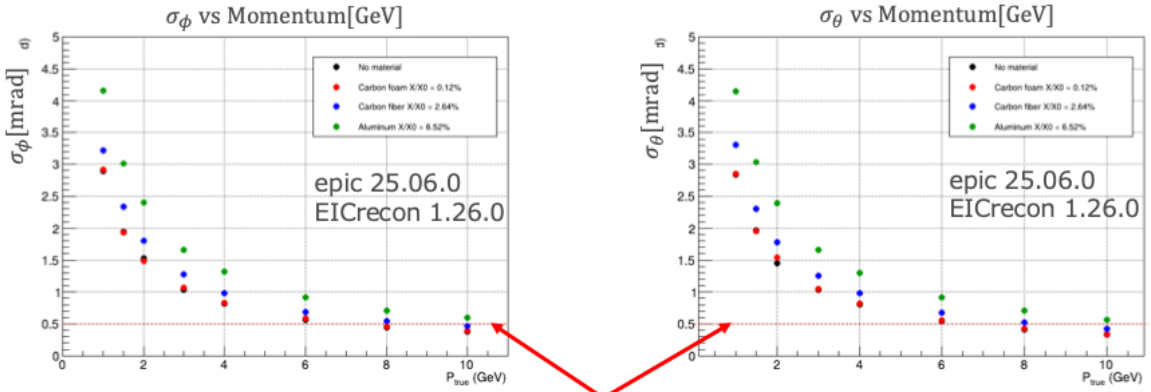
TOF simulation

BToF; Digitization work-flow design



Angular Resolution for different Materials

- Slight performance degradation observed with increasing material budget
  - Carbon foam keep the resolution close to requirement
  - But, not very sensitive to material budget → Can ToF be more dense?



Detector Requirements 0.5mrad @ 6GeV

Checked impact from finite timing and tracking pathlength resolution

- Timing resolution is crucial for PID performance

  Ex) 44ps timing resolution

  - 3 σ pi/K separation up to 1.2 GeV
  - 3 σ K/p separation up to 2.1 GeV

EICROC0 1st prototype

Arzoo Sharma

Charge sharing using MPV from Landau Fit

- **Event Selection: Hitbit for Pix 5=1 and Pix 5 with Max Amp after Pedestal subtraction.**
- **Landau Fitting to ADC distribution Normalized w.r.t. amplitude in Pix #05.**

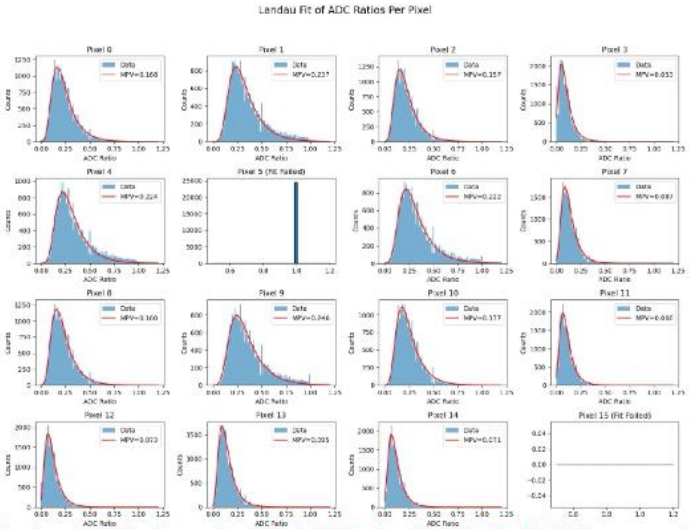
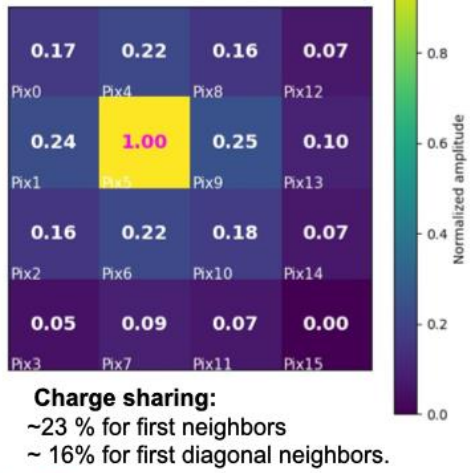


Fig.: Landau Fit to Normalized ADC distribution for hit in Pix 05. Fit is represented in red color.

Fig.: Charge Sharing ratio for hit in Pix 05.



Charge sharing:
~23 % for first neighbors
~ 16% for first diagonal neighbors.

Conclusions

- ✓ Beta source measurements performed with BNL 4x4 pixelated sensor Wire-Bonded to EICROC0 ASIC.
- ✓ 95 % of the events are cut with event selection cut (hit bit =1 in pixel of interest and has max amplitude).
- ✓ For pedestal subtraction, the far pixel chosen, which almost never crosses the threshold (implying corresponds to the noise).
- ✓ The analysis shows consistency with the scope data, while the method is more reliable.
- ✓ Charge sharing studied using Landau fitting.
- ✓ For central hit pixel Charge sharing is ~23 % for first neighbors ~ 16% for first diagonal neighbors. For edge hit pixel Charge sharing is ~32 % for first neighbors ~ 20 % for first diagonal neighbors.
- ✓ For all cases, diagonals have approximately 60 % of the charge sharing as compared to direct neighbor.

Future perspectives

- ➢ Further analysis Ongoing to determine charge sharing in all pixels and timing resolution.
- ➢ Ongoing measurements to acquire data for more statistics.
- ➢ Exhaustive study of all the sensor boards (BNL Flip Chip + BNL and HPK Wire-Bonded). (Future: Flip Chip Sensor without metallization for LASER setup)
- ➢ LASER setup completed; measurements commenced to investigate detector position and timing resolution.

Measurements with ^{90}Sr β source : Digital Readout

Pix-to-Pix Adjustment

- **Threshold adjustment** channel-by-channel performed.
- **Baseline adjustment** channel-by-channel done.

EICROC0 + wire-bonded BNL AC-LGAD

Detector Bias = -200 V
I ~ 0.06 microA

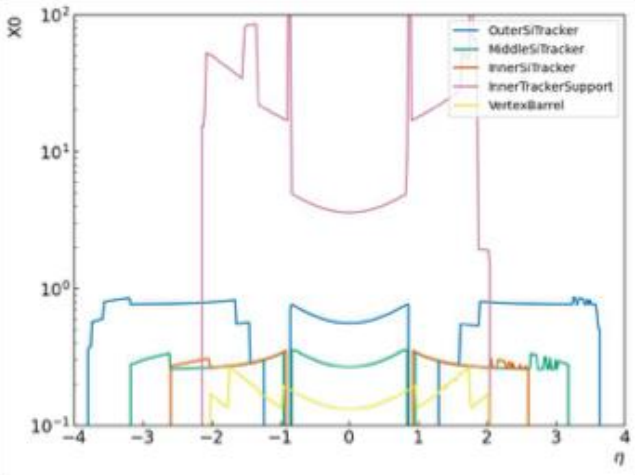
Adjustments performed for lower charge DAC Pulser 12 (~5 fC) [CMD pulse] and setting global threshold 300 DACu

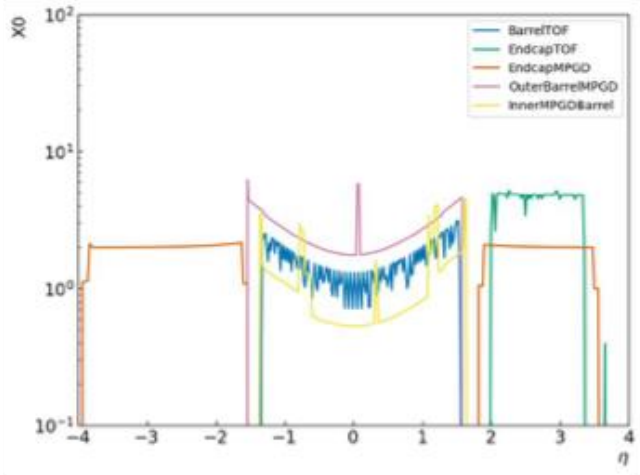
Tracking

Shujie Li (LBL)

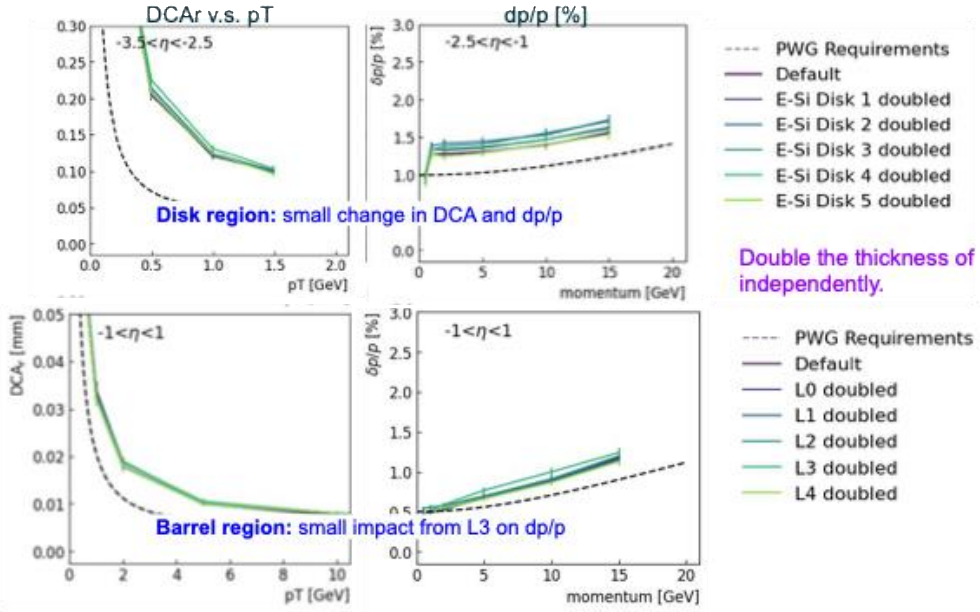
Material Scan

- ePIC 25.07.0 :
  - new material map
  - updated TOF geometry (see Tommy's talk on Tuesday)





Tracking Layer Material Thickness Study



Proposed tracking study for TOF

- **Geometry**:
  - Services and mechanical structures?
- BTOF and ETOF **impact** study:
  - with single particles, and background merged samples
  - In longer term, include timing info
- Material **thickness** study
- **Reconstruction**:
  - Charge-sharing and clustering (signal threshold?)
  - Angular resolution at DIRC:
    - Consistency b/w MPGD and TOF?

Discussions?

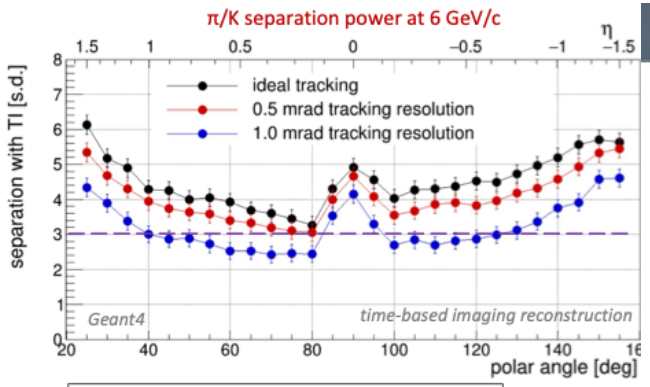
hpDIRC requirement and material budget

Expected hpDIRC Performance vs. Tracking

Impact of tracking angular resolution on hpDIRC performance

- π/K Cherenkov angle difference at 6 GeV/c: $\Delta\Theta_c \approx 3$ mrad
- Yellow Report tracking requirement: 0.5 mrad resolution at 6 GeV/c
- Track position (x_{bar}, z_{bar}) at DIRC with few mm precision

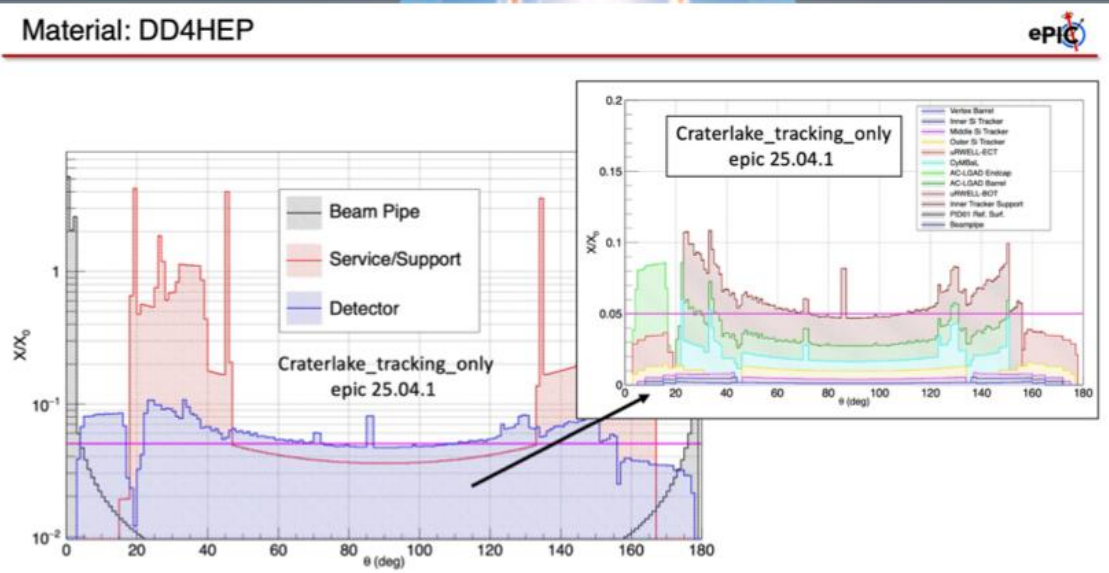
→ High-precision angular resolution crucial for reaching required hpDIRC performance.



Simulation studies performed with
- Stand-alone Geant4 simulation
- Single particles from particle gun
- 1.7T magnetic field, no other ePIC subsystems
- 100ps resolution

ePIC Track Resolution

Material: DD4HEP

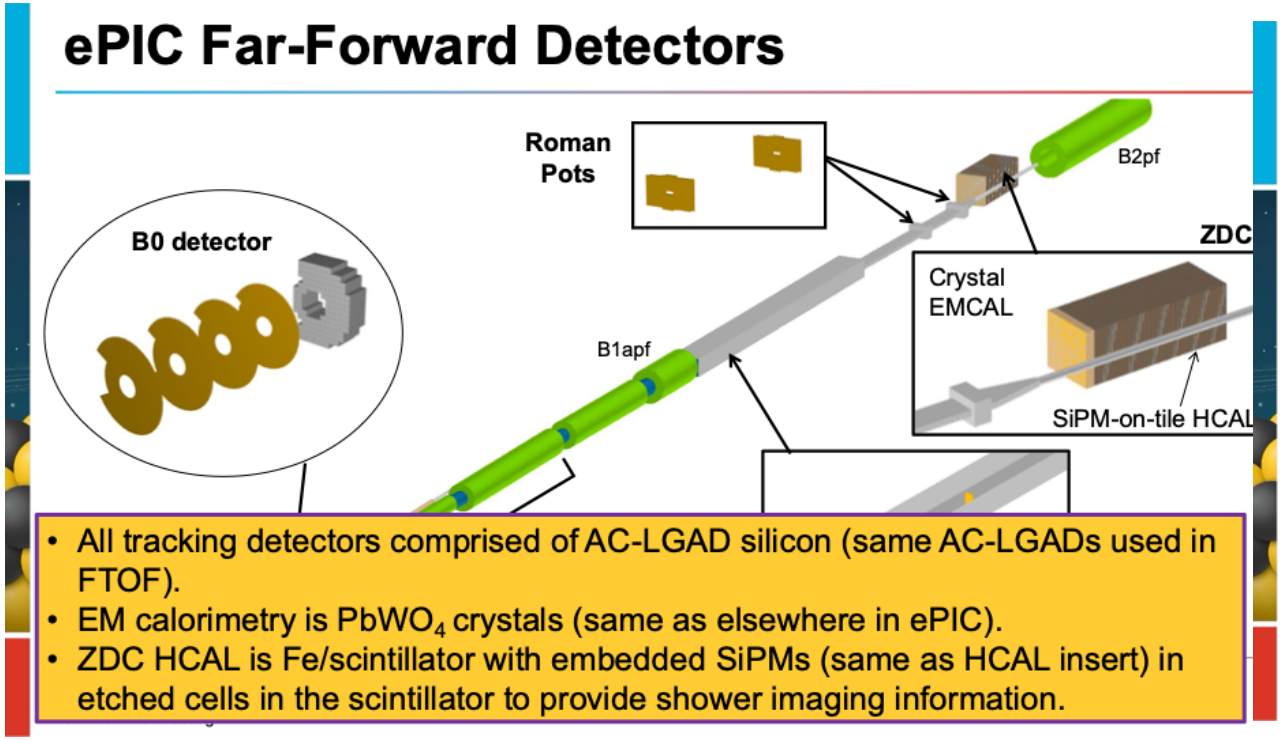


DIRC Annual Meeting July 1st ,2025

Matt Posik (TU)

It appears that BTOF material is not the dominant component.

AC-LGAD for Far-Forward Detectors



Summary (AC-LGADs detectors)

- AC-LGAD work is progressing apace.
  - Expect to have both EICROC1 + 32x32 channel AC-LGAD "in-hand" (in the lab) by late Fall 2025.
  - PCB design for the staves will begin, in-earnest, once we receive the EICROC1 schematic.
  - Final version of ASIC expected Fall 2026.
- Cooling concepts being studies, with RP/OMD having major progress in FY25.
  - B0 can be cooled using air/CO2 + capillaries; RP + OMD require more-complex cooling solution in-vacuum.
- Based on progress thus far, all detectors will be able to reach necessary design maturity by end of the year for baselining.
  - Construction readiness for late 2026 expected, assuming AC-LGAD components ready for tracking detectors.

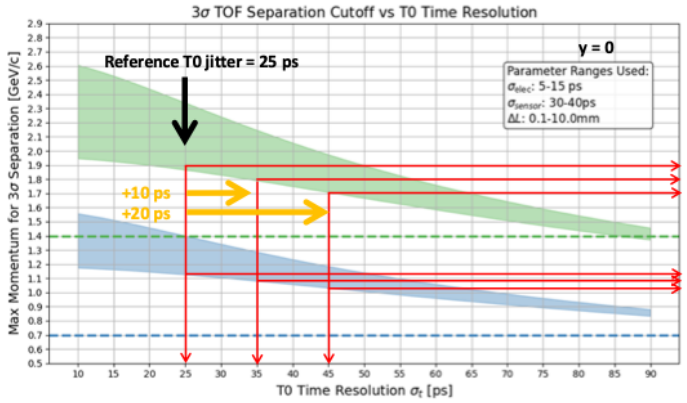
Item	Work needed	Status
4x4 AC-LGAD + EICROC0 testing	Finalize testing of full sensor + readout	Almost complete – Summer 2025
Testing of 32x32 LGAD + EICROC1	Prepare and test sensors (just received); receive testboards + ASICs	Expect to begin sensor testing + characterization Summer 2025; full tests Fall 2025,
Cooling (RP/OMD)	RP/OMD cooling concept simulations making rapid progress – need to have staves in-hand for lab tests.	Concept is promising, can meet needs (in simulation) – once preliminary design of stave is ready, can update simulations (early Fall 2025); tests of full setup aimed for Spring 2026 (assuming Fall 2025 availability of EICROC1).
Cooling (B0 Tracker)	Concrete workup of cooling system needed	Needs to have a preliminary design before PDR in Winter 2025.

Sensors chosen due to capability to provide precise timing (~35 ps) and spatial resolution (~ 20um, or less).

- Timing a primary capability of LGADs, in-general (FF has less-stringent requirement compared to TOF).
- Spatial resolution delivered via charge sharing (500um pixels → normally deliver ~ 140um spatial resolution, previous beam tests show ~20um possible with charge sharing). Especially important for the B0 tracking.
- Power consumption of the ASICs expected to be ~ 1-2 mW/ch.
- Presently, 4x4 sensor + ASIC assembly has been tested.
- 32x32 channel AC-LGADs received at UIC in late May.
- EICROC1 (32x32) expected in Fall to begin testing.

TOF resolutions and DAQ requirements

T0 Timing Resolution v.s. PID performance (BTOF case)



Δp ~ **0.1 GeV/c** per additional 10ps jitter for K/p sep.

Δp ~ **0.05 GeV/c** per additional 10ps jitter for π/p sep.

- In σ_{T0} = 25 ps case, the overlap region is shifted by ~0.05 GeV/c for π/K sep. and ~ 0.1 GeV/c for K/p sep. when the additional jitter is 10 ps

"Reasonable Estimates of full time resolution"

Feature	pfRICH (ps)	Barrel TOF (ps)	Forward TOF (ps)	Notes
Sensor	40	35	20	
ASIC Analog	11	11	10	Large Hits
ASIC Digital Precision	25	25	6	Modifiable?
Fiber Delay	24	24	24	Assume 6 deg C
lpGBT	30	30	30	Assume 6 deg C
RDO	6	6	6	FPGA
DAM	6	6	6	FPGA
GTU	6	6	6	FPGA
Delivered Clock	24	24	24*	Assume partial Tc
Collision T0	25	25	25	20-30 ps
Total	71	69	58	Dumb Quadrature

1. Need to identify clearly event-by-event "jitter":
   Sensor, ASIC Analog/Digital,
   RDO, DAM, GTU?

2. Uncertainty that can be calibrated online/offline due to slow variation:
   fiber delay, lpGBT, delivered Clock

3. Required by certain physics cases:
   collision T0 (only required for exclusive single hadron production)

My proposal is that when discussing TOF timing requirement, we should really focus on item#1

Other items discussed

- PED requests for 2026
- Beam tests
- PDR review in November 2025
- Assembly sites, procedures and construction