

8/21 INTT meeting

Digital-Control-analysis

Rikkyo university M1 TOMOKI HARADA

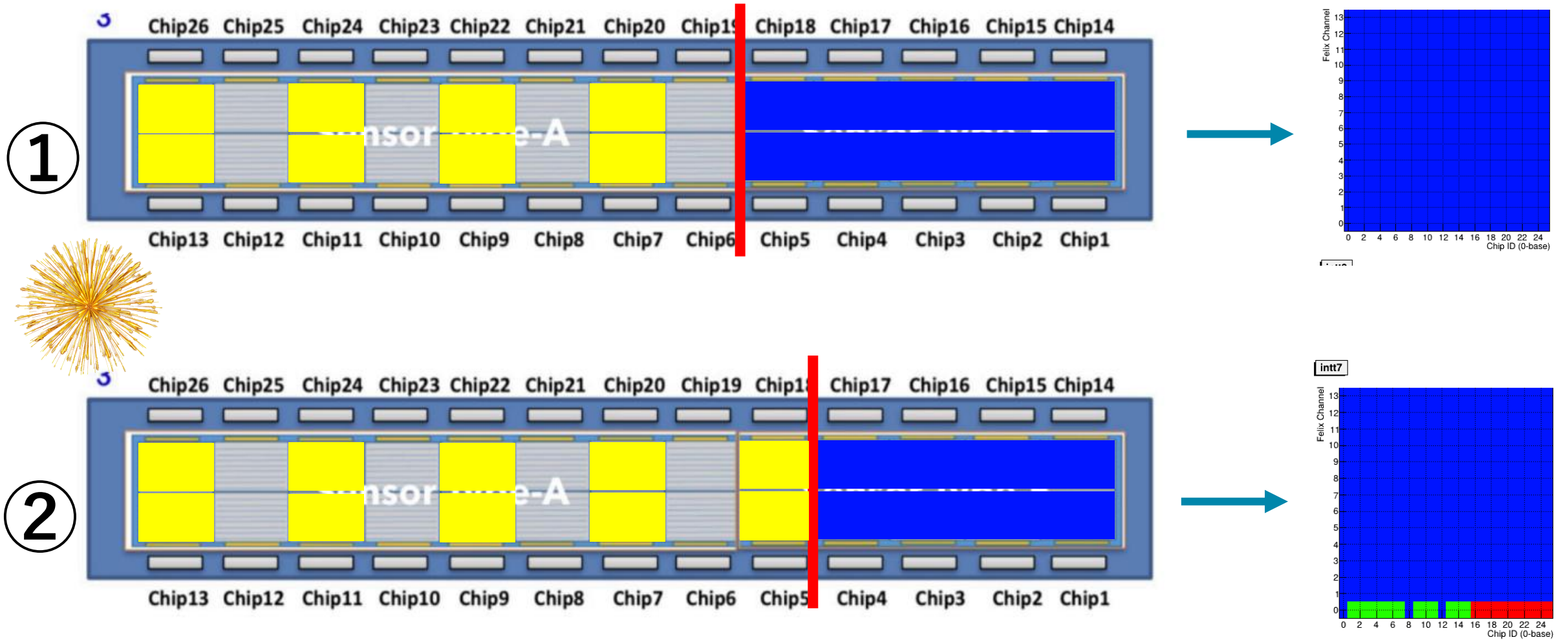
- I reported my study at SCM. → and, requested some runs.
- We could take 3 runs for digital control test. → Unfortunately, 1 half-ladder became HOT. But, the other half ladder could be successfully recovered!
- I reported the results of these runs at SCM → applying the particular parameter operating for all half-entry chips except one hot half-ladder.



- 8/15 There was the opportunity to take cosmic → We could check about one half ladder with some digcon_map.
→ all half-entry chips of typeA(midrapidity area) = 8 chips could be recovered simultaneously.

P.S. I finished college assignments !
and finished taking 3 shift !

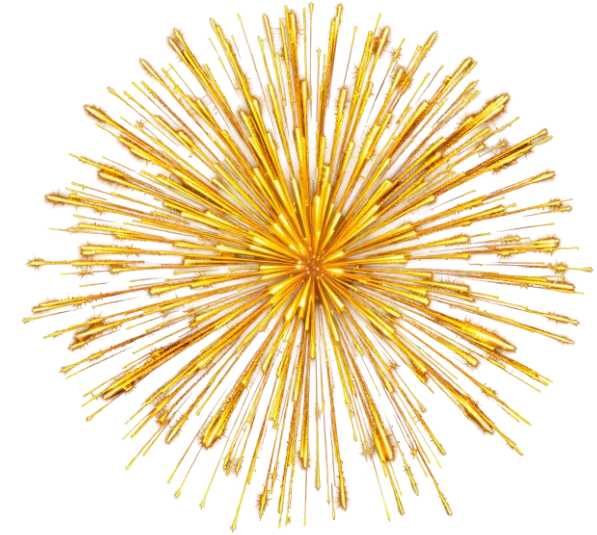
Today, I request the plots for Preliminary
After that, I will mainly work on making poster for IS.



I applied the digital-control-parameters operating for yellow chips above **in cosmic**.

Half-entry-chips chart

Felix Server	0	0	3	5	7	7
pid	3001	3001	3004	3006	3008	3008
module	6	7	13	3	0	1
chip id	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	15	21, 23, 25	16	1, 2, 3, 4, 5, 7, 9, 11, 13, 14, 15, 16, 17, 18, 20, 22, 24, 26	1, 2



now
38 chips + unstable half entry chips ~1.4% of total

Finally, we could recover 28 half-entry chips !

map : ~/INTT/map_digcon/latest/digcon_28halfentry.txt



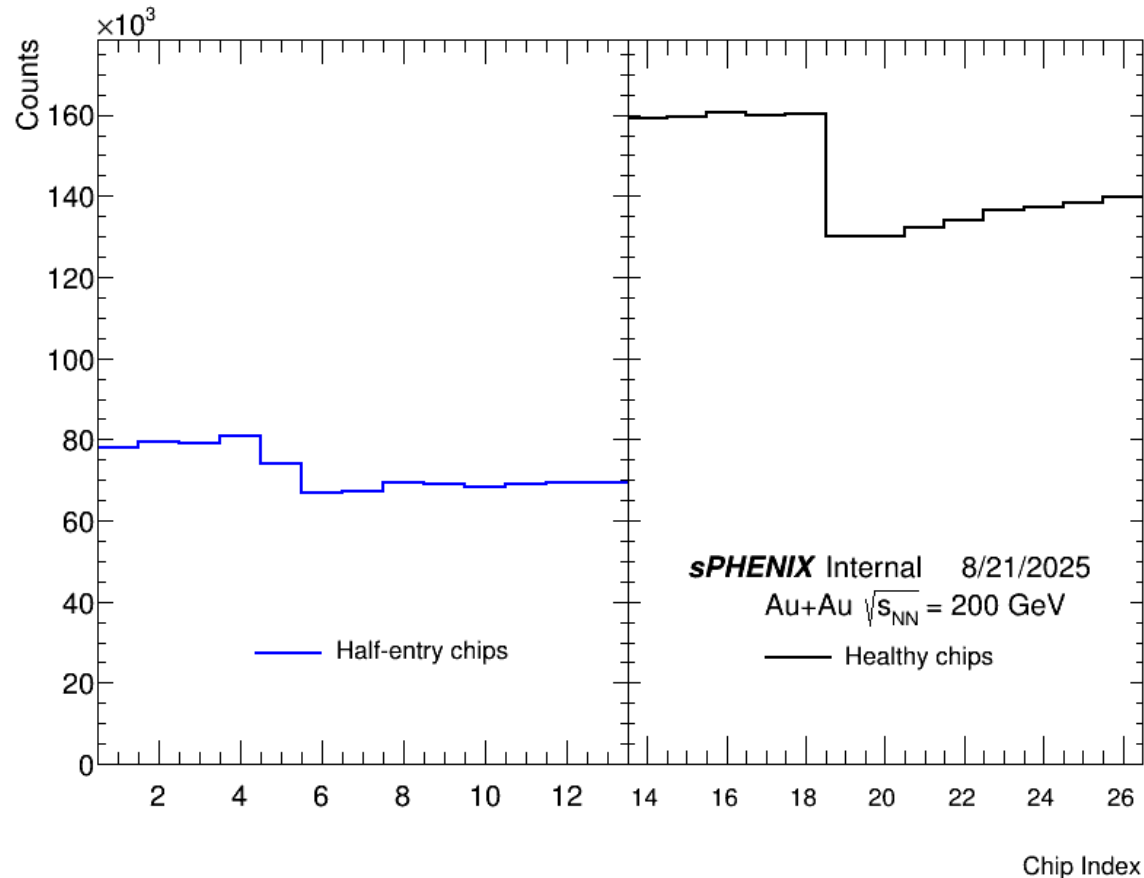
Monday, 3 chips of recovered half-entry became hot only 2 runs in 8 hours on the accidental. → I'll check.

8/21pre-GM Digital-Control-analysis

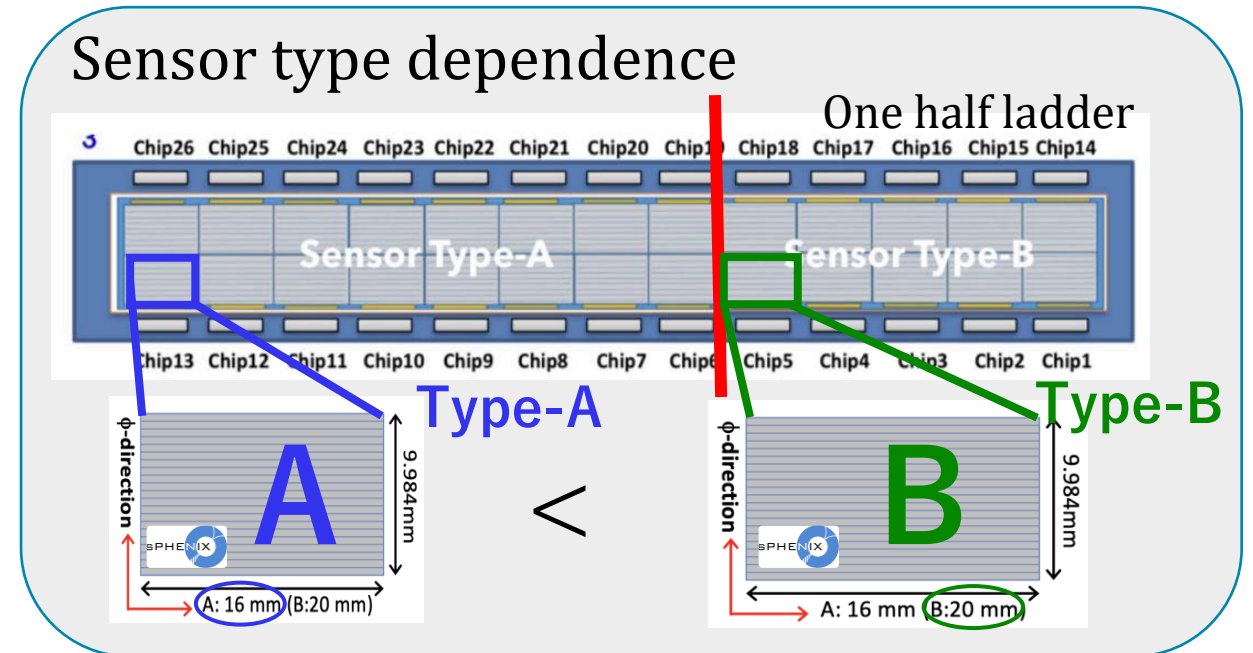
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Half entry issue

The INTT has long been known to exhibit a “**half-entry issue**,” where chips record only **half** of the expected hits due to a malfunction of one output line in the FPHX readout chip.

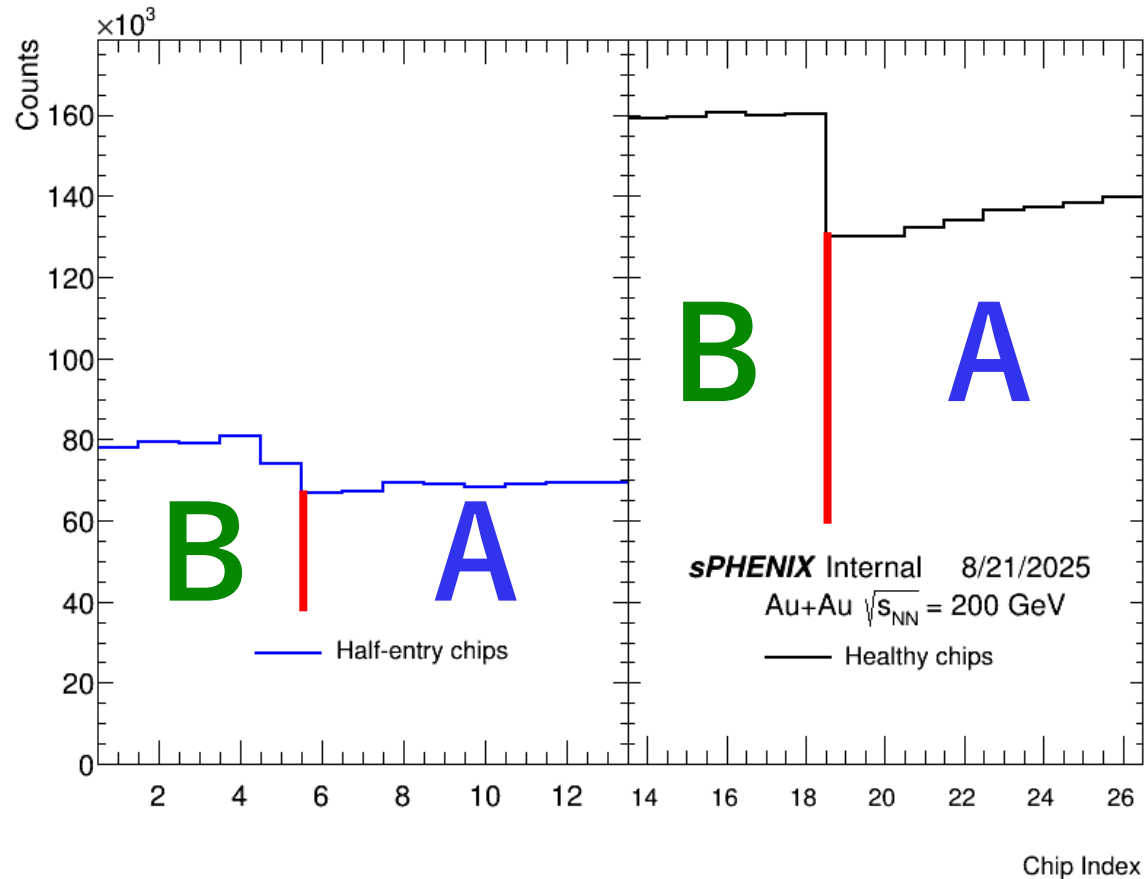


Entry count plot for one half-ladder.
Chips 1–13 are half-entry.

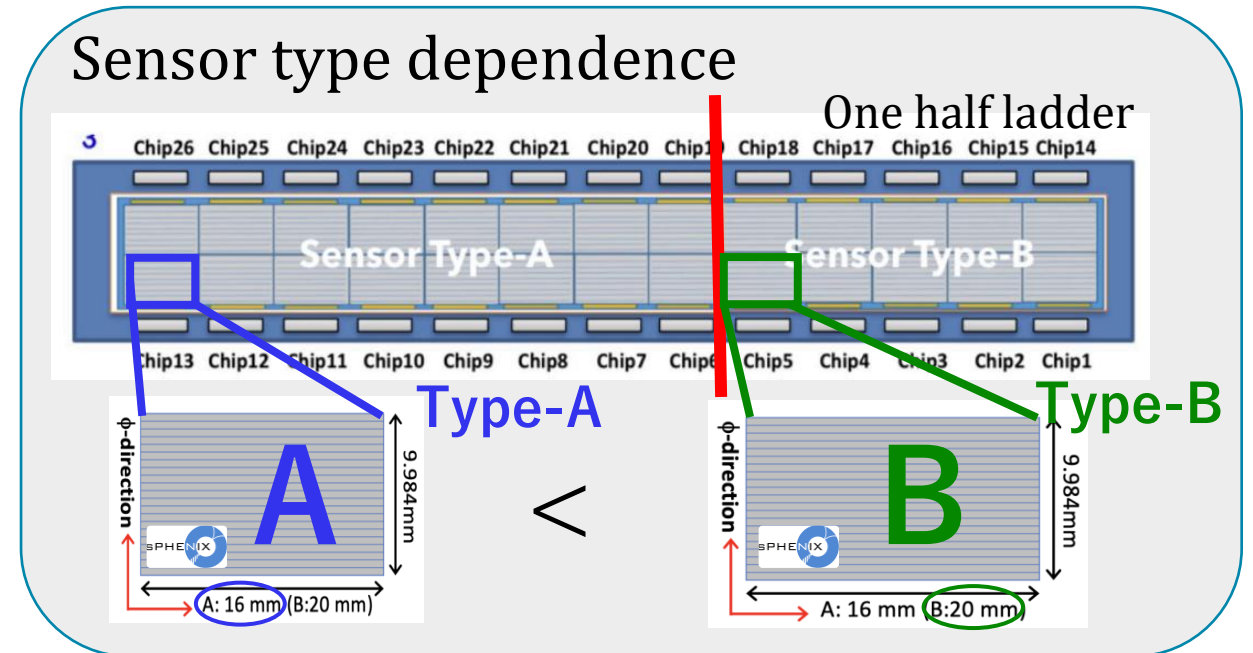


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Entry count plot for one half-ladder.
Chips 1–13 are half-entry.



Half entry issue

This issue happens in 38 chips/2912 chips(1.3 % of total).

We've already known "how many chips have this issue" , and "Where these are" as shown chart below.

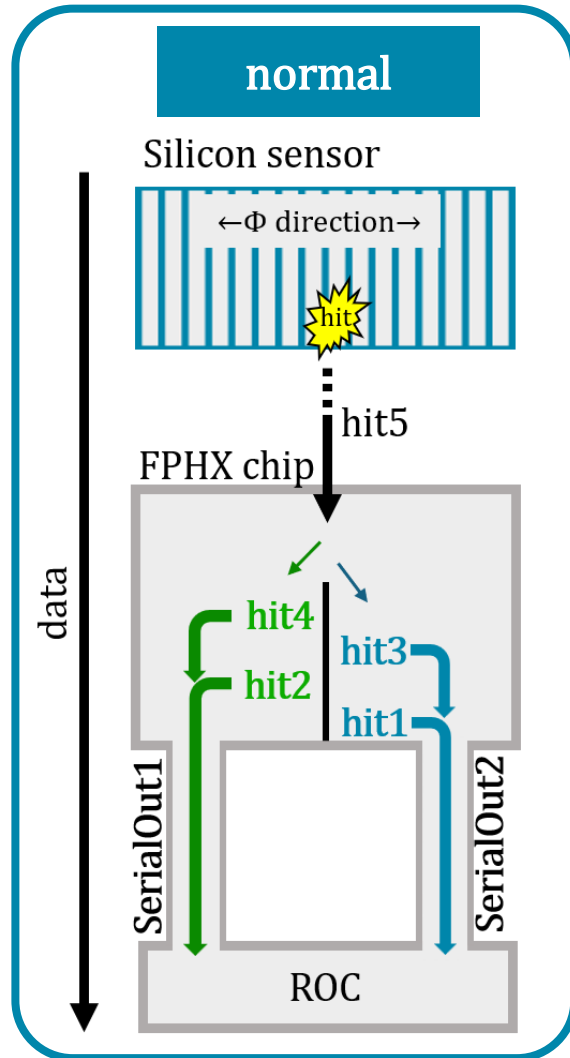
Half-entry-chips chart

Felix Server	0	0	3	5	7	7
pid	3001	3001	3004	3006	3008	3008
module	6	7	13	3	0	1
chip id	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	15	21, 23, 25	16	1, 2, 3, 4, 5, 7, 9, 11, 13, 14, 15, 16, 17, 18, 20, 22, 24, 26	1, 2

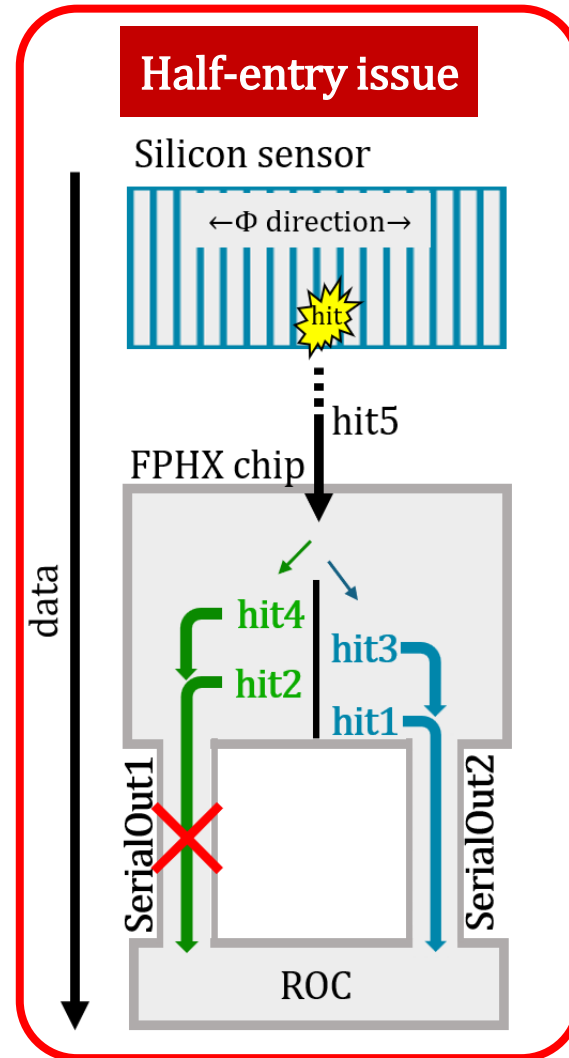
In this slide, focusing on this ladder

Half entry issue

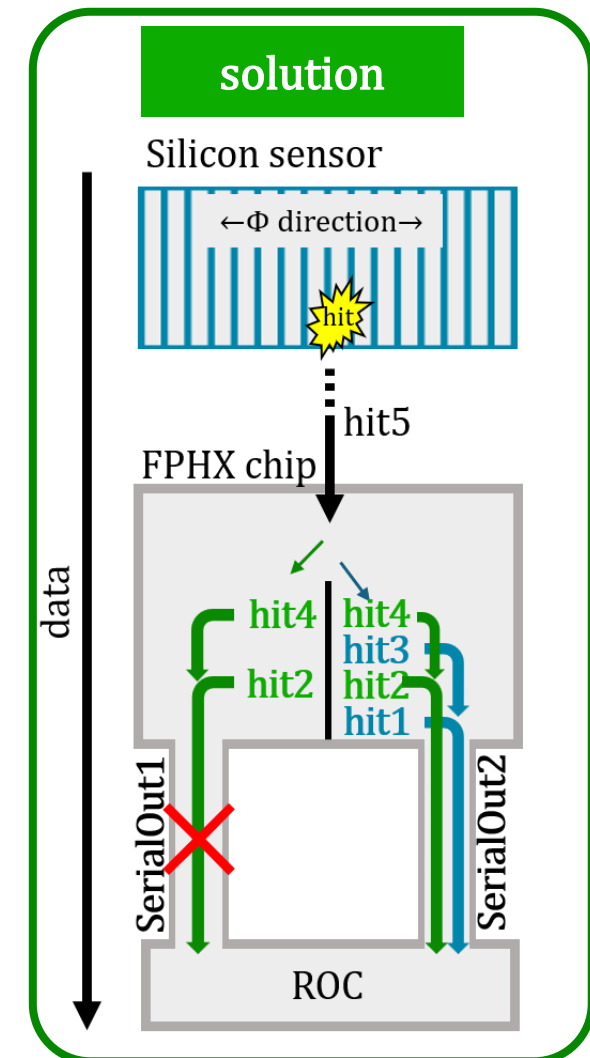
Mechanism of this issue



All hits are processed



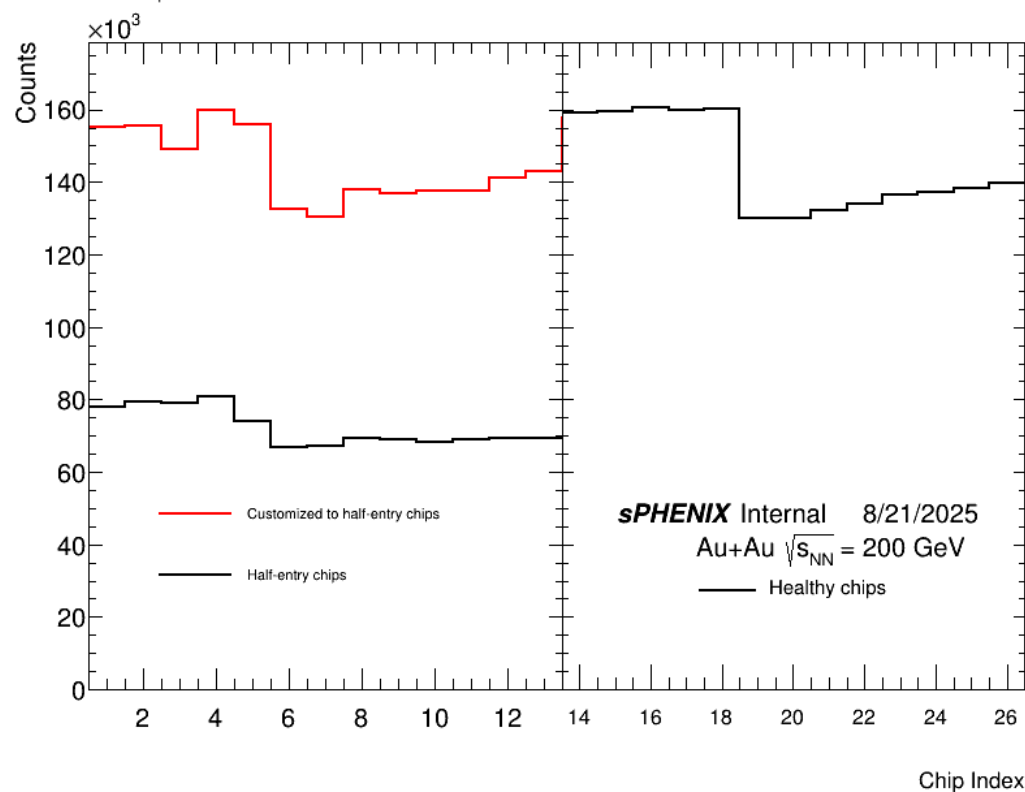
Half of hits are lost



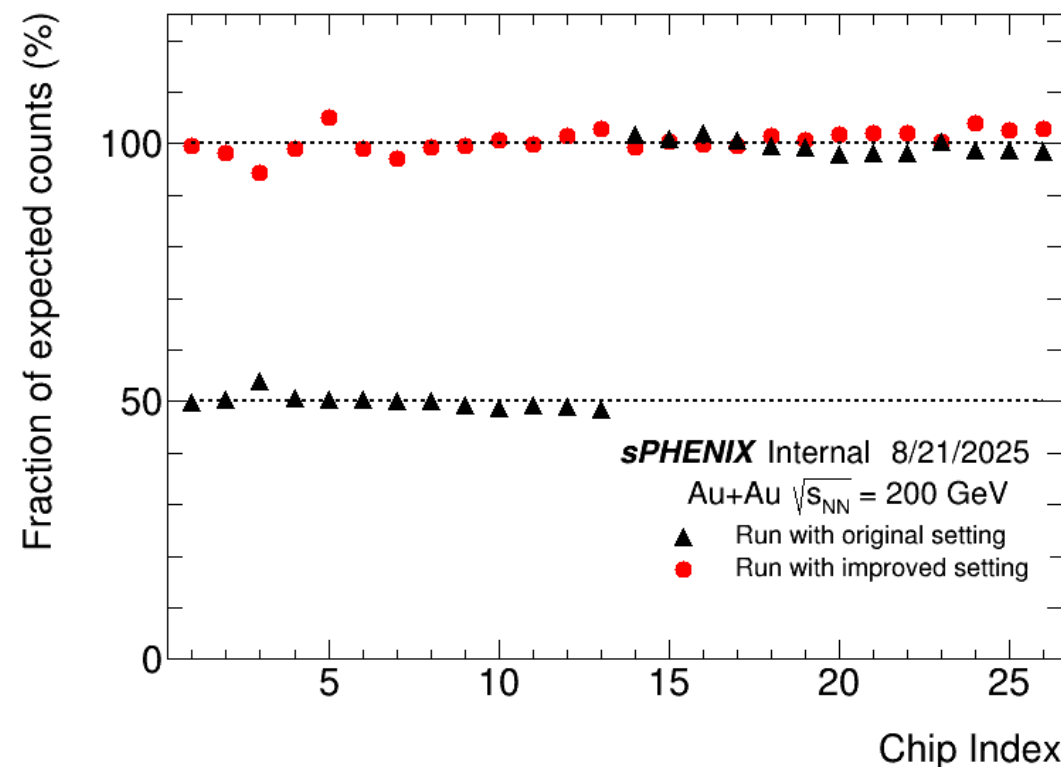
Lost hits are recovered

Study results

Felix Server	0
pid	3001
module	6
chip id	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13



Chip counts comparison between run with original and improved setting. Chip 1 to 13 are all half-entry chips on this half ladder.



From chips 1 to 13, recovery of the number of entries is observed, while from chips 14 to 26, reproducibility across different runs is confirmed.

ADC distribution

In order to confirm the validity of the recovered entries, I checked the ADC distribution.

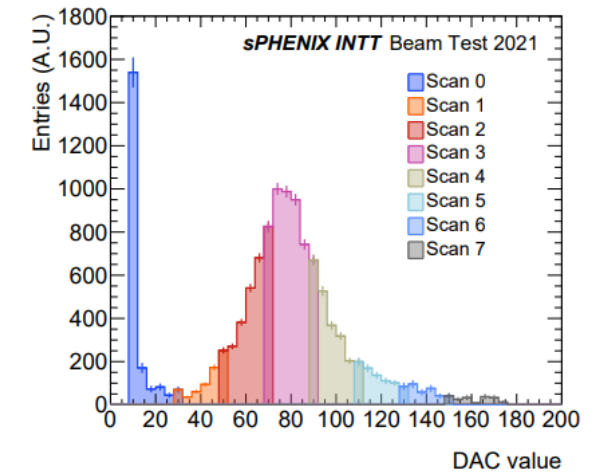
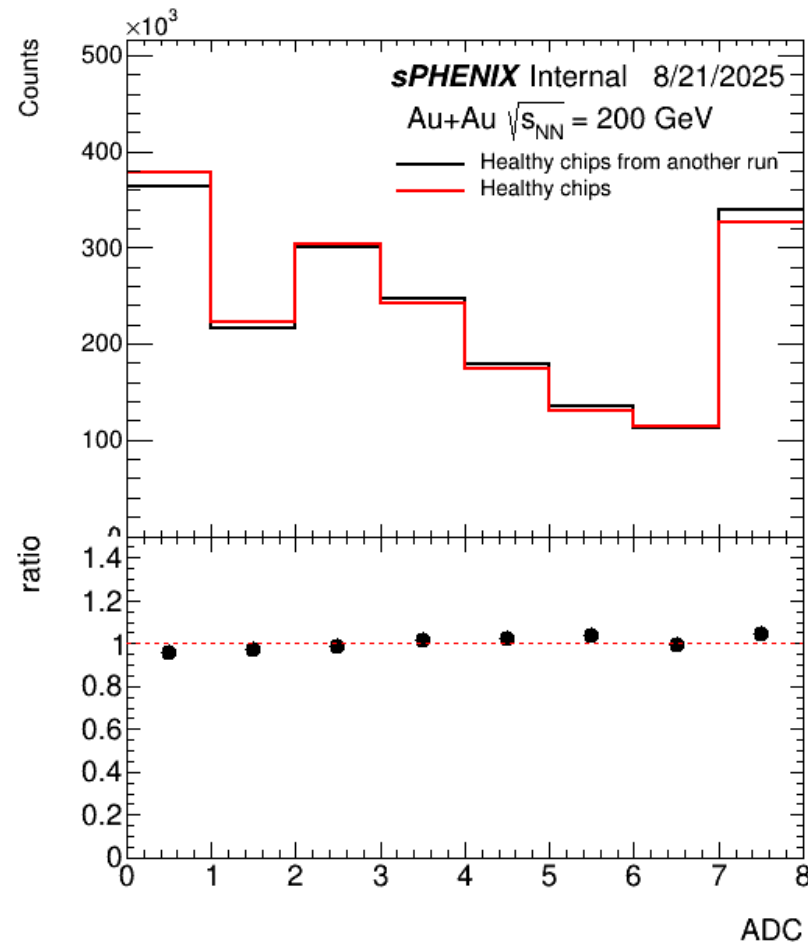
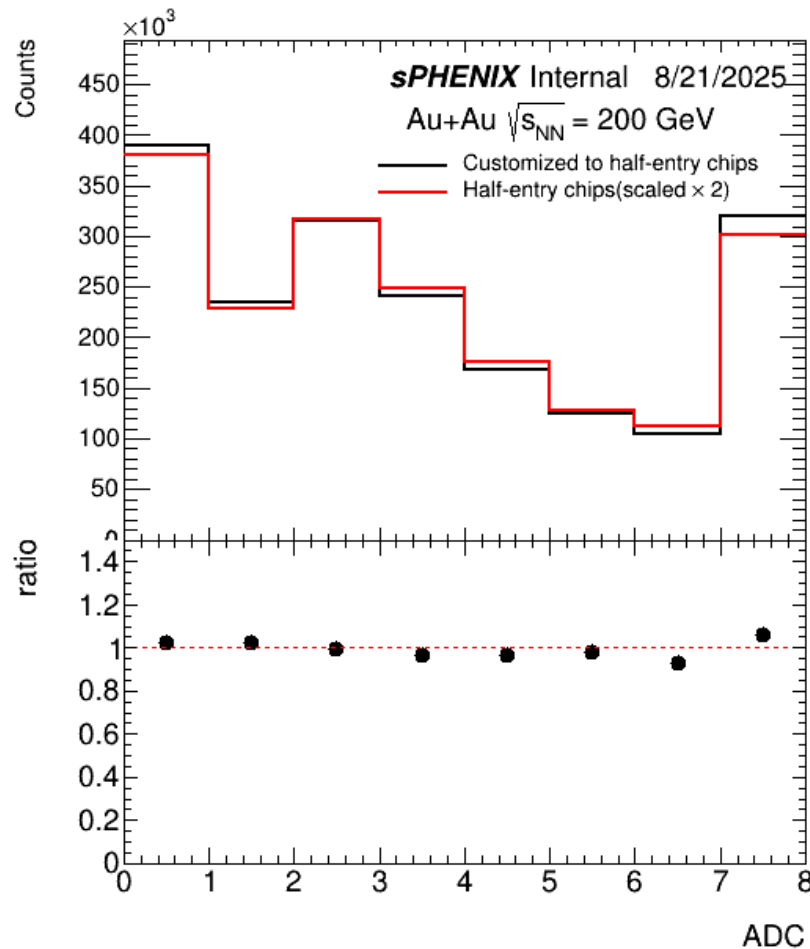



Figure 5: The energy-deposit distribution, constructed by the eight sequential measurements (histograms with different colors) after applying scaling factors, for a representative ladder (L_0).

<https://sphenix-invenio.sdcc.bnl.gov/records/384w0-rw788>
beam test

 When viewed in 3 bits,

