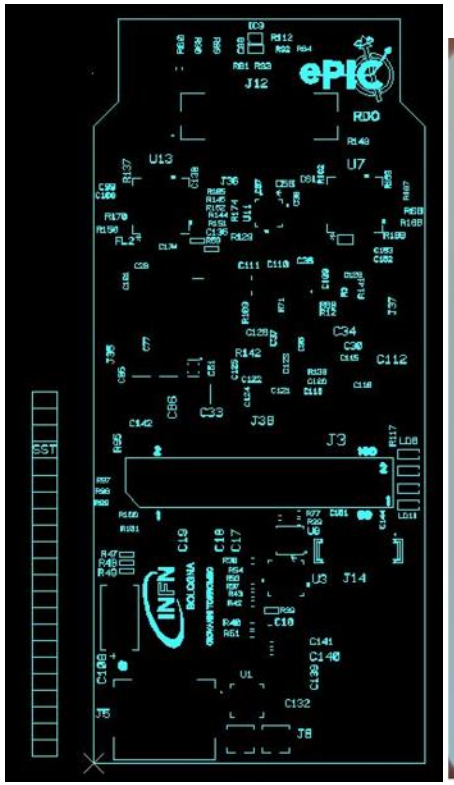
dRICH RDO
eRD109 report



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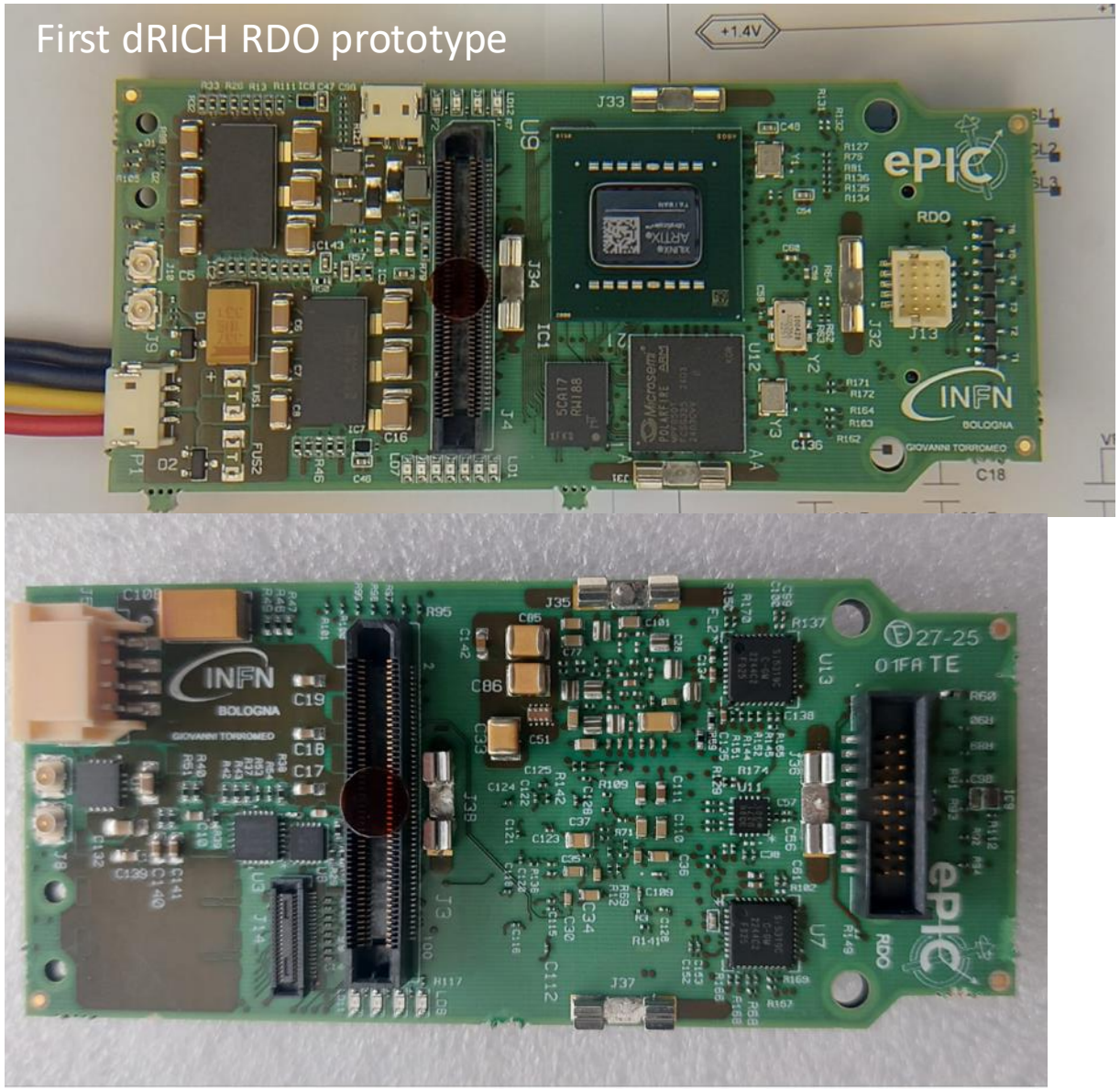
L. Rignanese, G. Torromeo
(INFN Bologna)

+ all dRICH group

eRD109 monthly report
August 7, 2025

dRICH RDO is getting real!

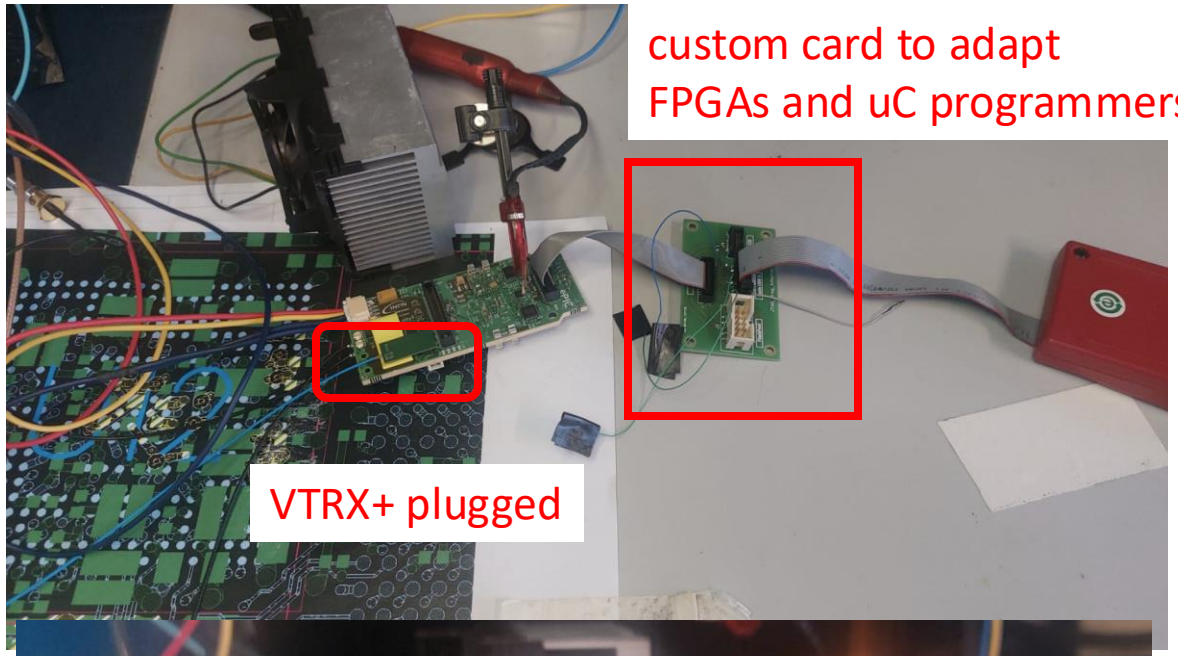


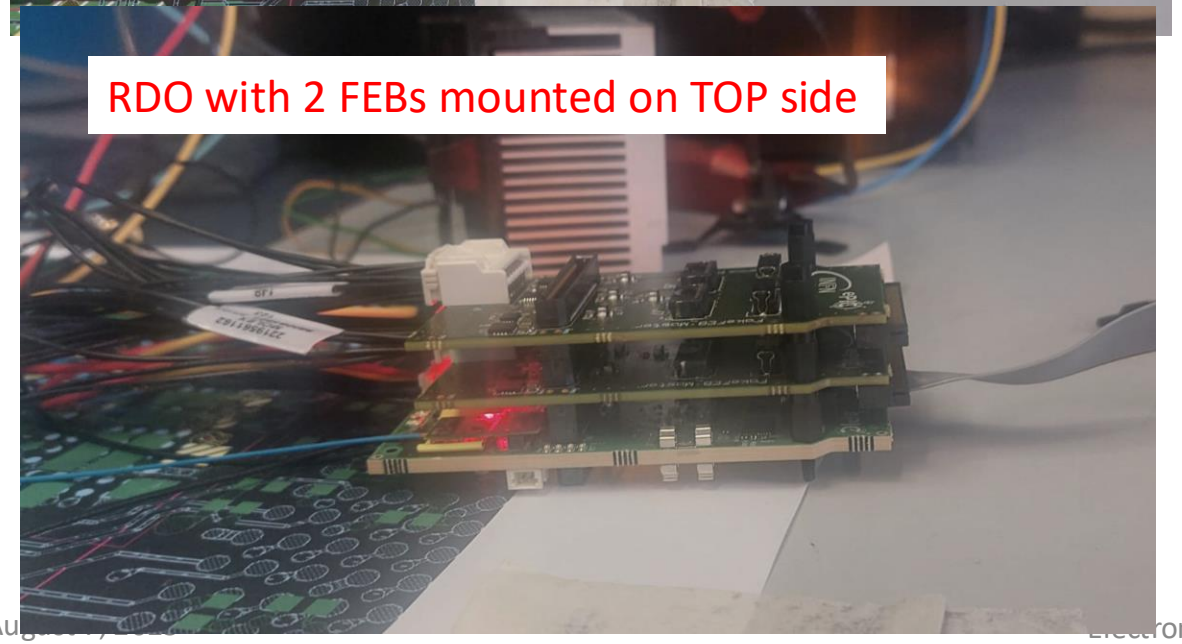
finally received **July 24!**
for update ”at large” about preparing work on RDO
see PA talk at ePIC Meeting, July 17

This report:

→ ongoing debug / tests on first two prototypes
→ plan (2025/2026)

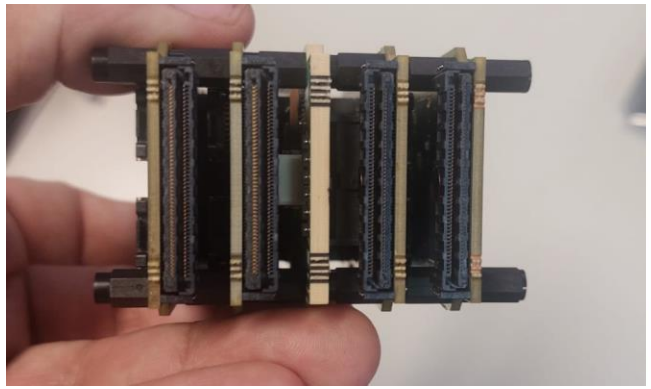
no longer 3D-rendering: some pics





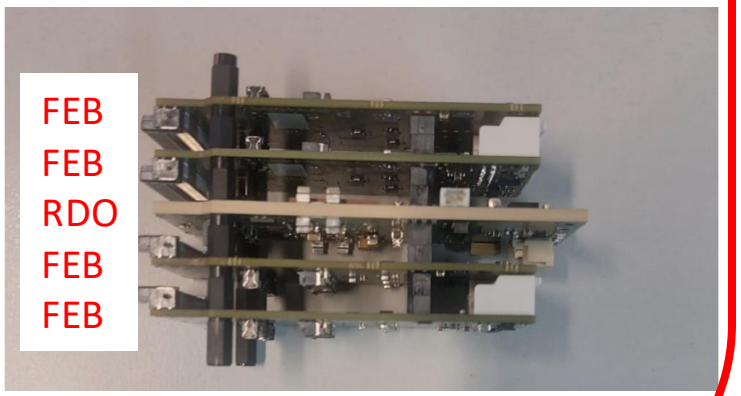
RDO+4 FEB dRICH

front side: connectors to SiPM

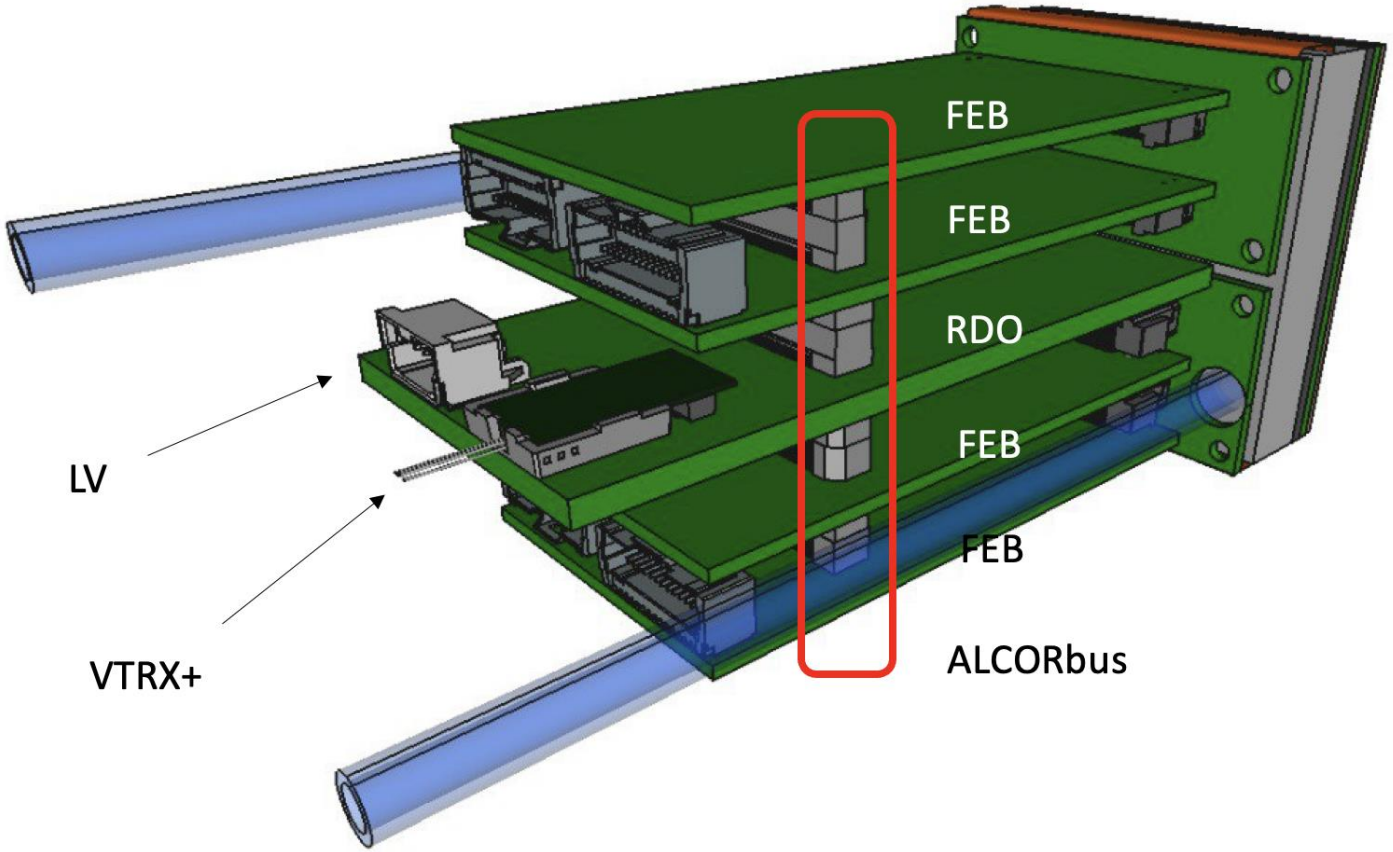


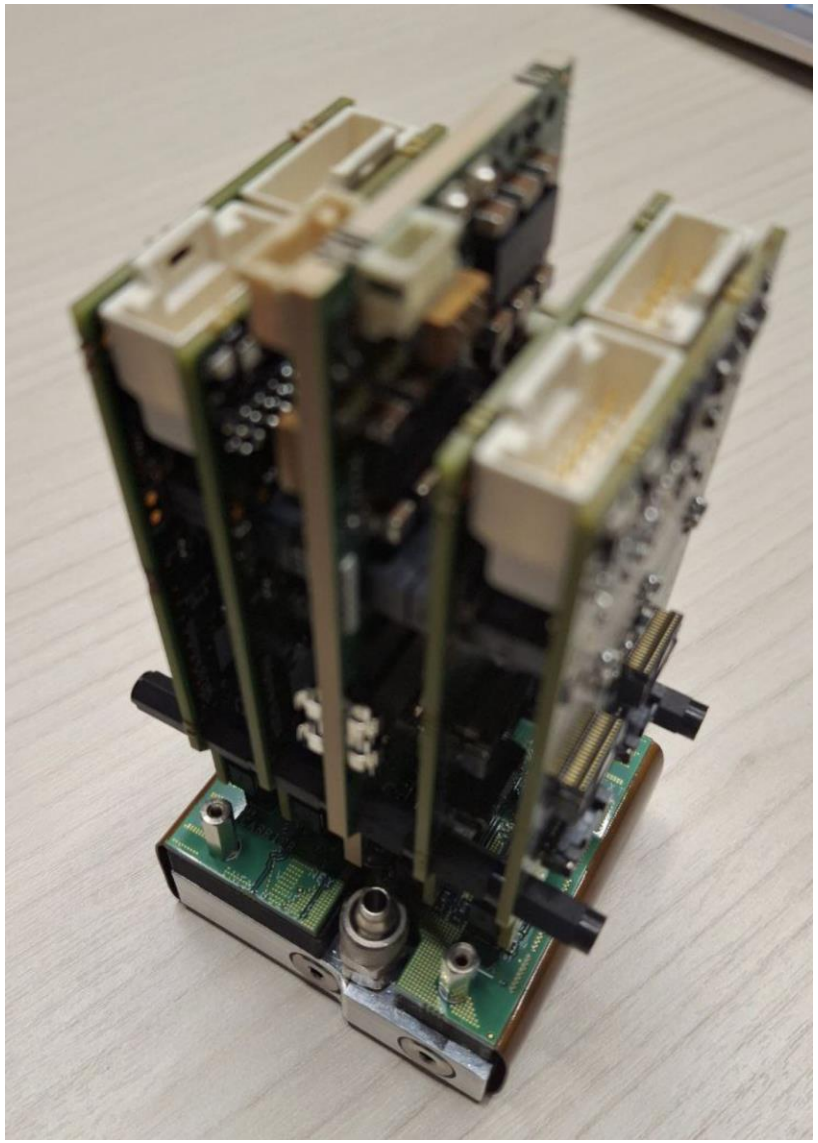
back side: HV/LV + link

The dRICH electronic burger



from CAD to pics: the PDU



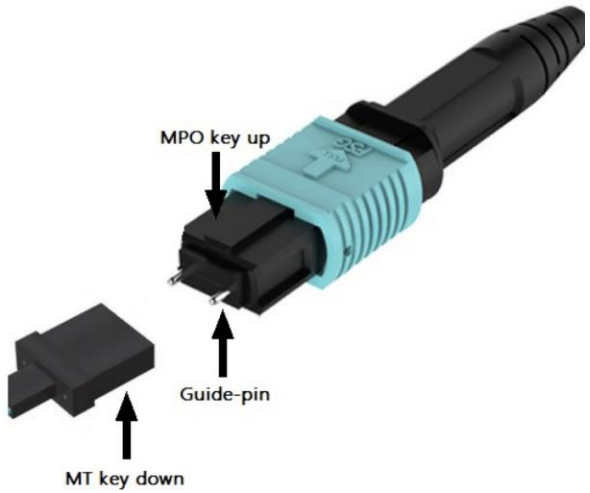


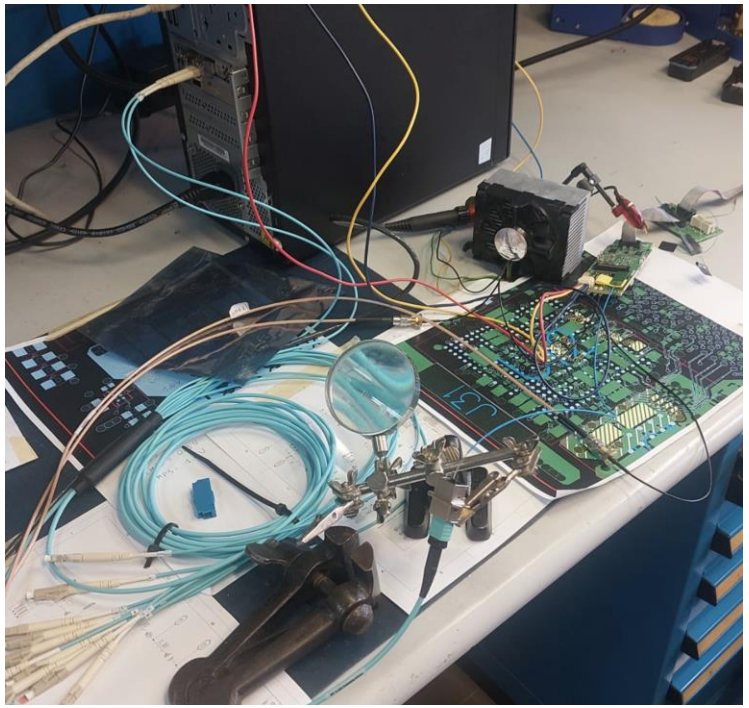
initial debug issues

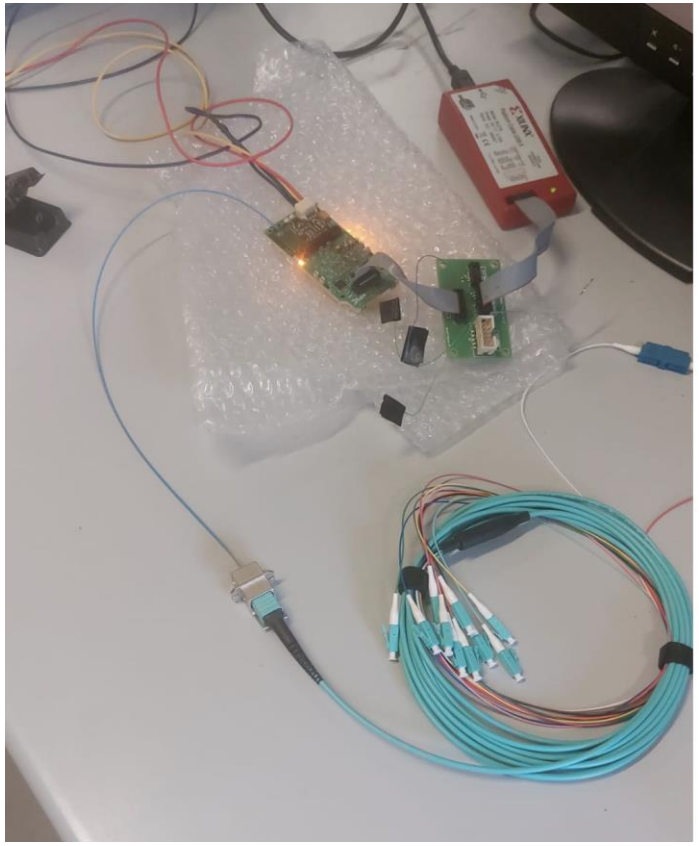
initial debug included the fixing of several problems (“minor issues”)

- mounted 2 Si5319 instead of a Si5319 and a Si5326 -→ we will do reworking
- mounted “wrong” charge pump component → fixed changing some resistors, we will do reworking
- a short due to a capacitor (layout error): bypassed
- somehow difficult the pairing of VTRX+ MT connector with MPO and then with fibers (we had initially the wrong fanout patchcord)

details







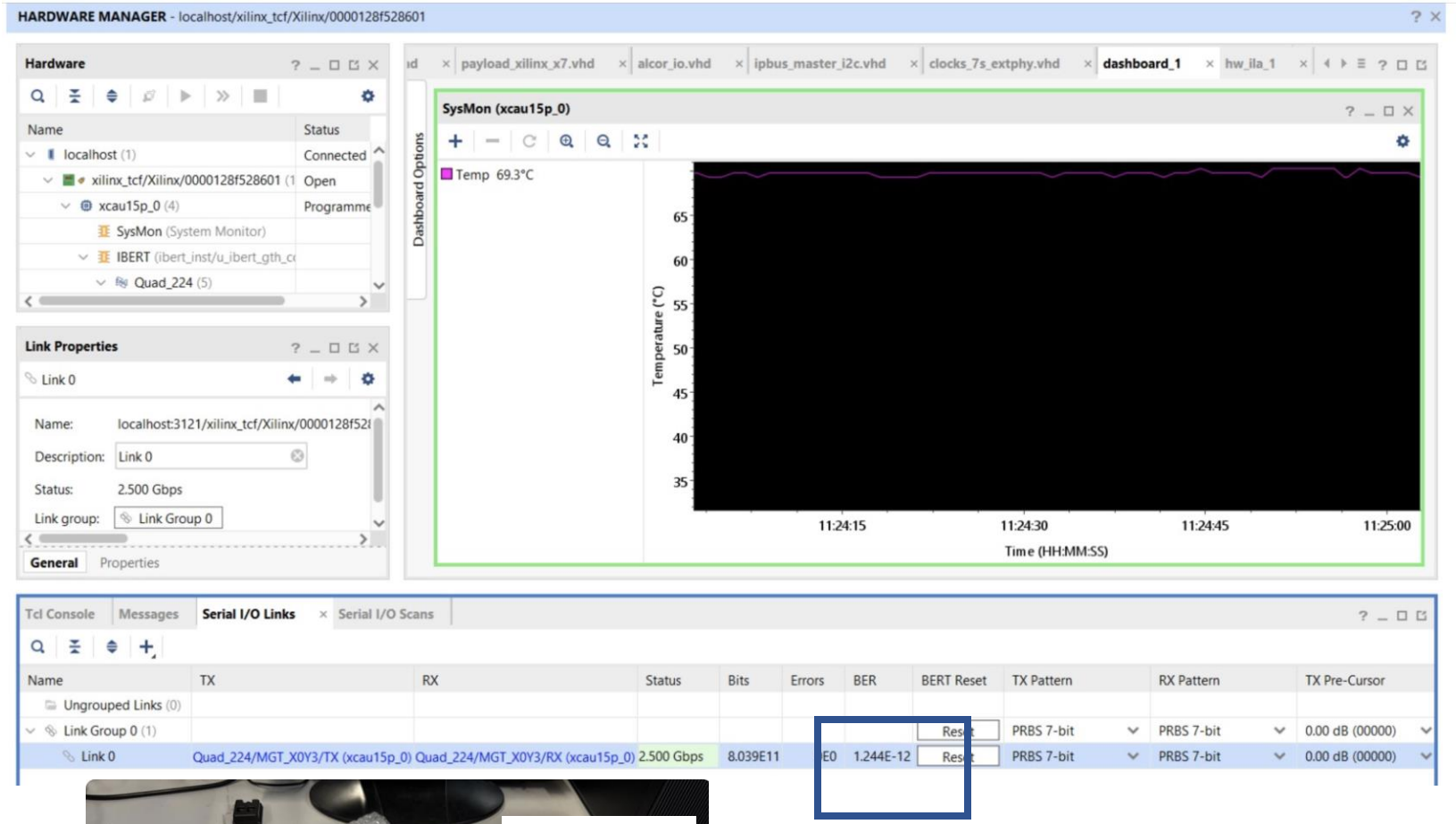
where we are?

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319 to setup clock for GTH)
8. Check consumptions
9. Check UFL I/Os
10. IBERT test (loopback tool integrated in Vivado) to check link
11. Link IPBUS via VTRX+ [MT-MPO adapter + fibers]
12. Turn on fake-FEB via I2C from RDO
13. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
14. ALCOR readout (via IPBUS → VTRX+)

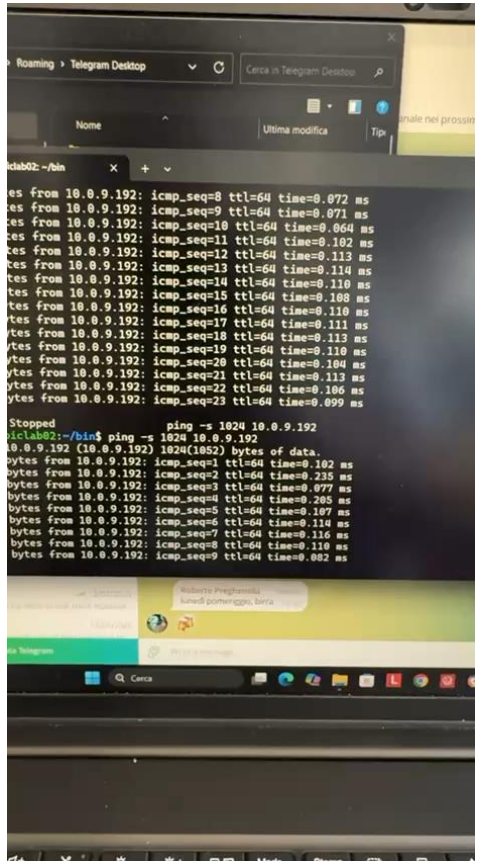
} we might be there by ….

When we reach point 14 we give go for mounting for other 8 RDOs for test-beam (deadline: due by mid-September we will likely implement other stuff in the meantime and we have contingency to fix issues)

checking the links

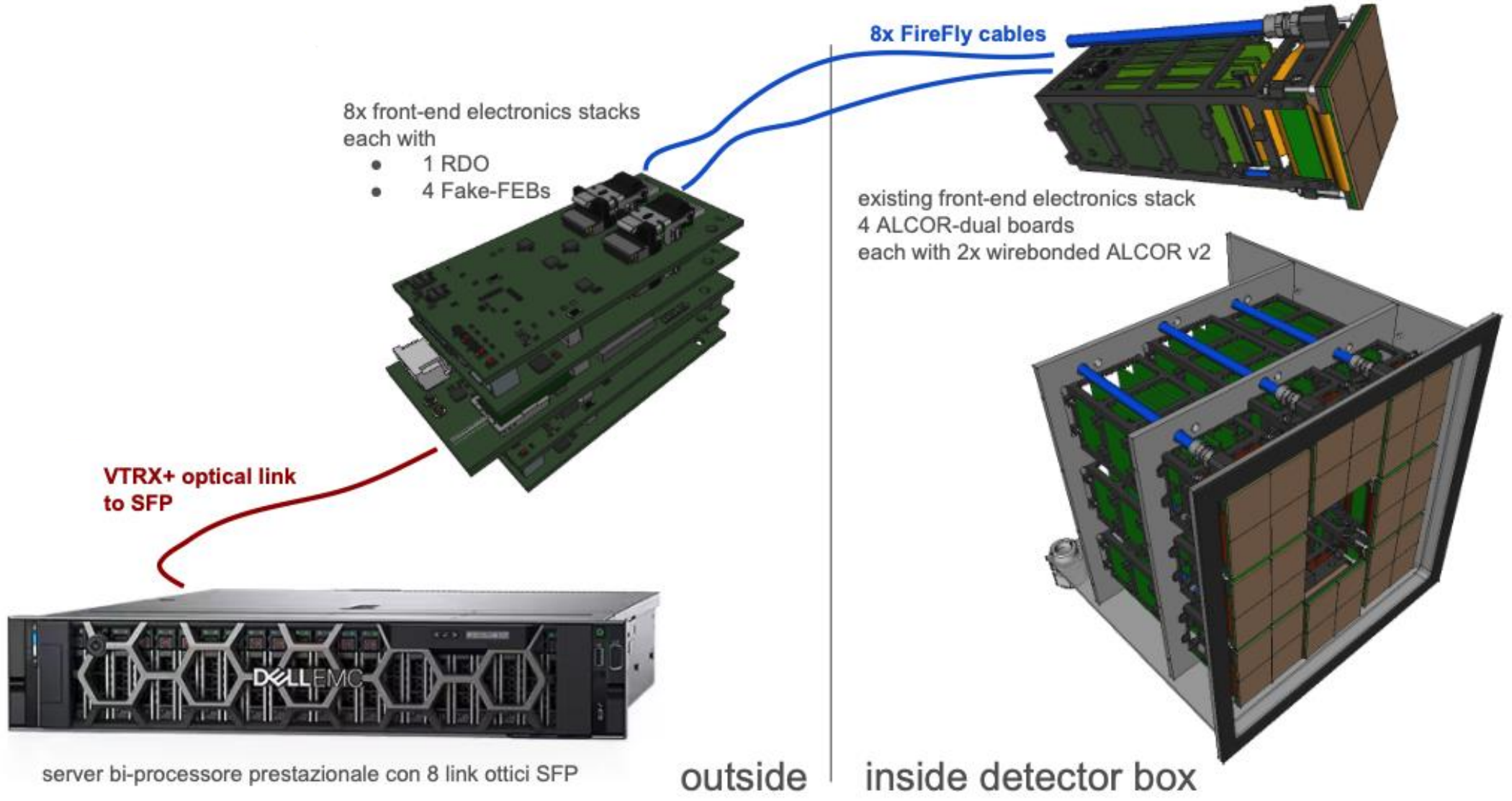


first ping to dRICH RDO

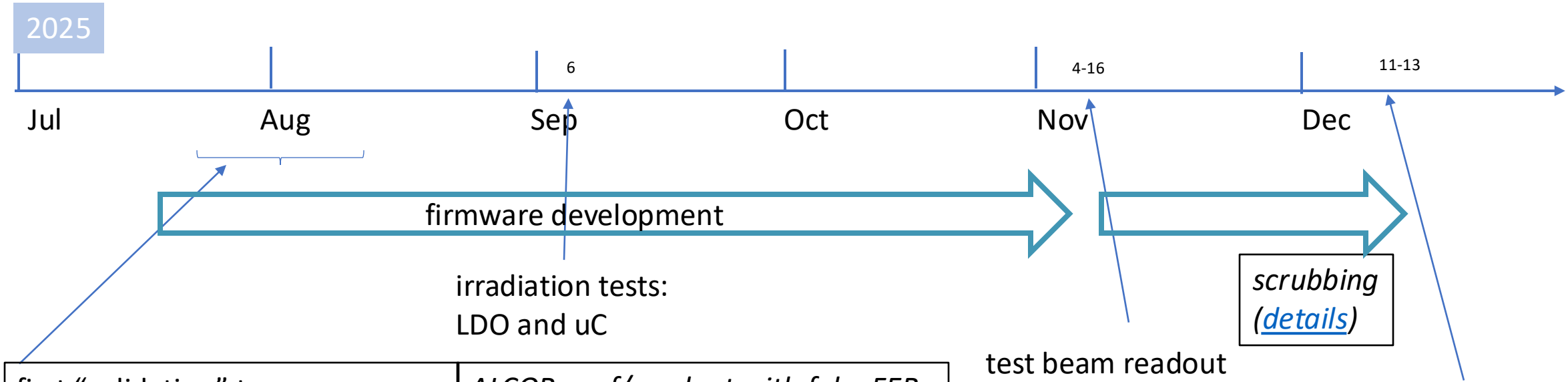


RDO setup for 2025 test beam (Nov. 2025)

- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- ”fake-FEB” : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)



Plannning and validation tests (2025)



Next steps/challenges for RDO

During 2026 we need:

- full validation of current prototypes

- fix any mistake found

- design adaptations due to integration challenges that may arise (cooling, space, FPGA resources, ...)
- prove communication with DAM (implementing a FELIX-supported comm. protocol)

application presented for PED funding

Irradiations (for RDO, components, SiPM…)

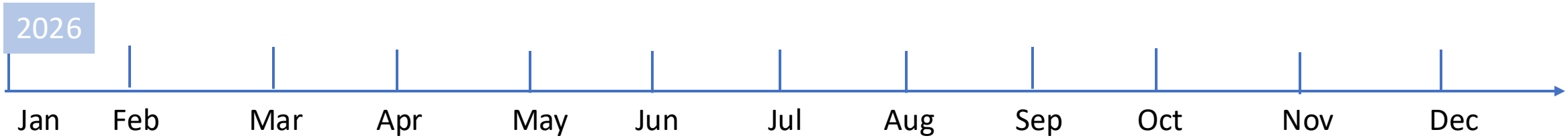
Why we still need irradiation tests?

- first full RDO irradiation test (Dec. 2025) will be learning exercise: it is first scrubbing test
- with firmware more advanced we need to check behaviour of the card – link stability etc.
- we will not go to CHARM in 2025 (we will free s.j. or ask to use for test beam…) but 2026 is the year to test whole PDU
- need to test ALCOR64 !
- need to irradiate a whole SiPM matrix to test then annealing in a true PDU

Applications for beam facilities for 2026

- TIFPA 3 sessions (or 2 but extending one to three days): RDO, ALCOR64 (FEB)
- CHARM, 1 session ("whole PDU). check "everything" plus we use a realistic mix of hadrons
  - whole PDU → we test all materials (glues, screws, connectors, etc.)

Plannning and validation tests (2026)



firmware / software development

remote programming

clock reconstruction – FELIX-supported comm. protocol (FULL with GBT on host)

second irradiation
test “full RDO”
@Trento

last test beam
readout full PDU
(RDO+ALCOR64)

irradiation tests:
full PDU @CHARM

details

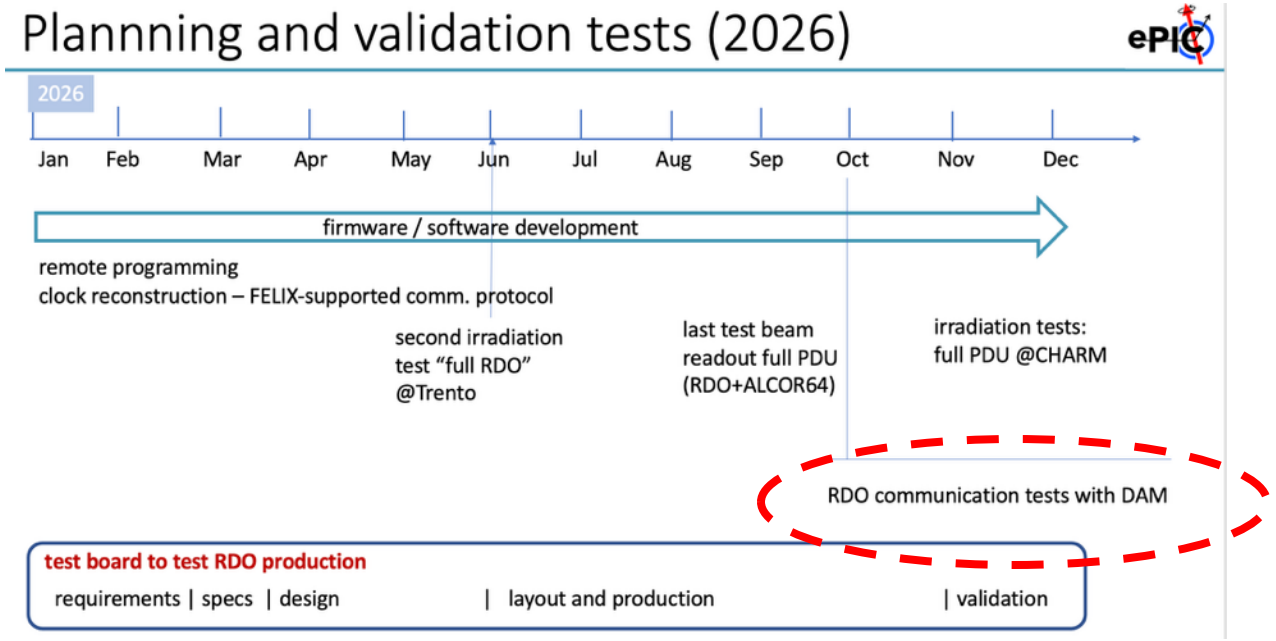
RDO communication tests with DAM

test board to test RDO production (preparing for 2027 RDO production!)

requirements | specs | design | layout and production | validation

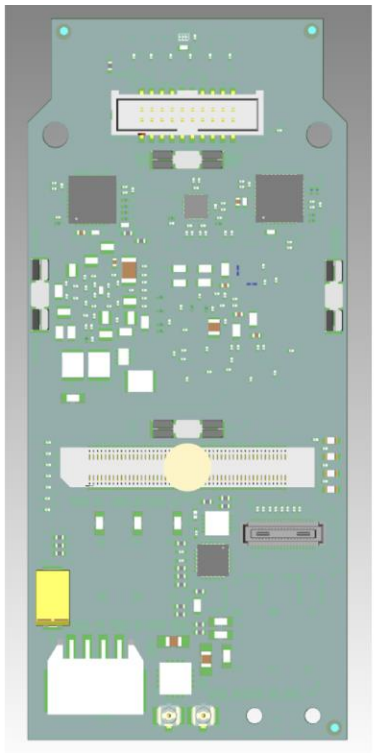
Summary

Bologna is following frontend DAQ (RDO) and Roma1 backend DAQ (FLX-155): hardware is finally available!
first two weeks of test on RDO are very promising, no show-stoppers identified
dRICH frontend DAQ and backend DAQ are much closer to finally meet



Backup

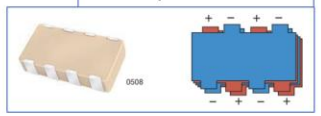
initial debug details



Top layer

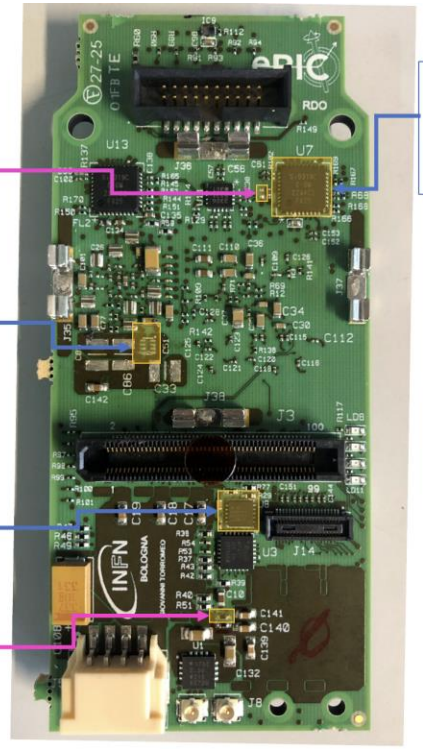
FL1 removed to not power U7

Problem with footprint of **C51**

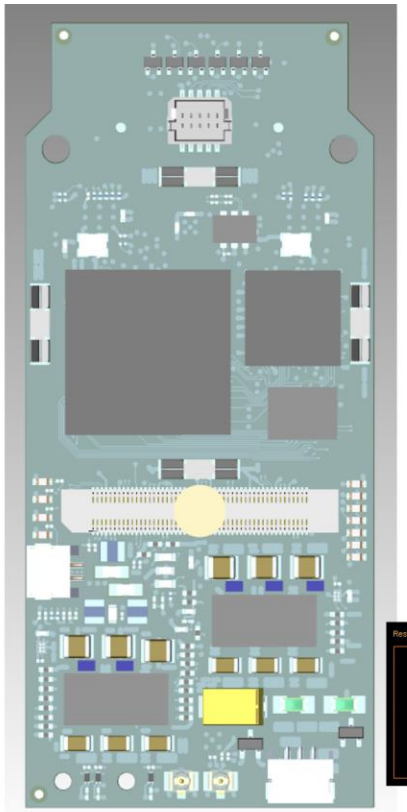


Problem with **U8** LTC3203BEDD-PBF

R19 1.5K changed to 2.2K to correct VOH level with wrong U8 (charge pump a 5V)

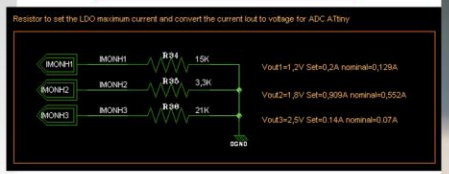


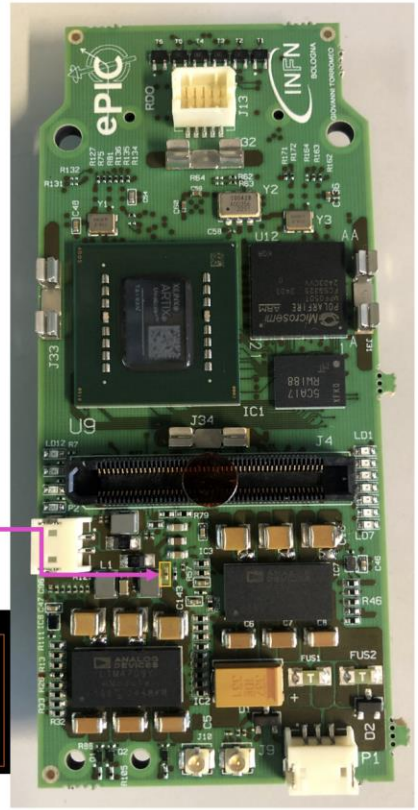
U7 Si5319 instead Si5326



Bottom layer

R34 15K changed with 8.2K to set 1.2V Iout limit





which firmware flavour in ePIC FELIX ?

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

Table of available link “flavours” in FELIX cards and FPGA resources usage (courtesy by A. Lonardo)

FELIX FPGA resource usage

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

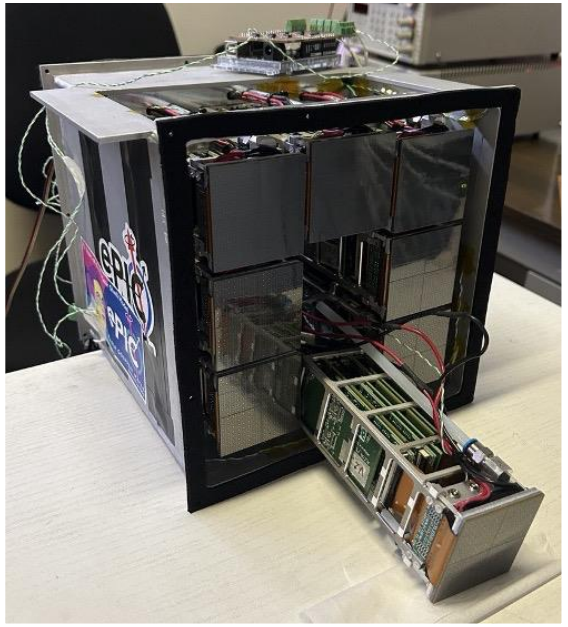
Note dRICH aims to use FLX-155 resources too for data reduction!

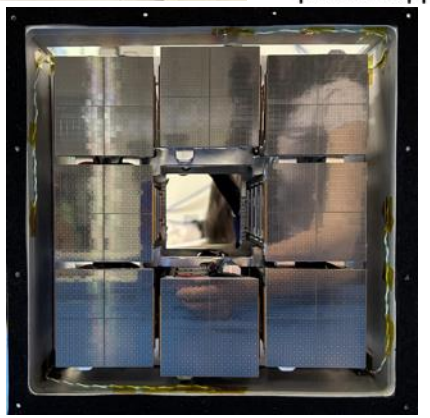
See A. Lonardo talk at ePIC Jan 2025 meeting

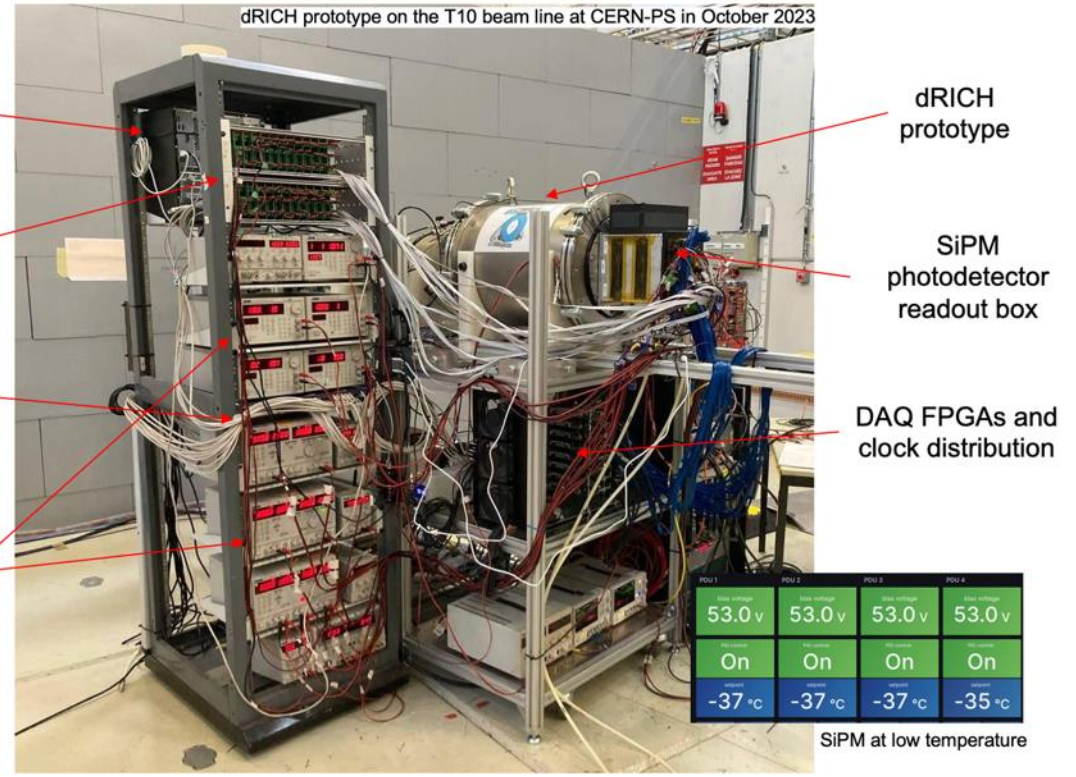
Update:
Rome1/2 has now the FLX-182 sent by BNL up and running!

- scale up to 48 lpGBT links might be a problem for FLX-155?
- as dRICH we use just the VTRX+ tranceiver not the lpGBT ASIC so lpGBT protocol not strictly needed but we would recommend to use anyway one of the existing flavour. FULL will be tested, agreement within ePIC

scale up to a test beam up to 2 kchannels







11 KC705 FPGA boards in parallel ➔ 64 AlCOR chips ➔2048 SiPMs

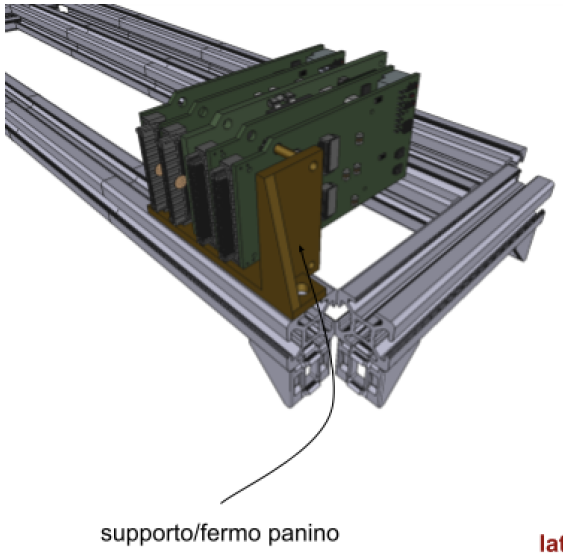
next step is bringing readout inside the PDU (RDO comes after)

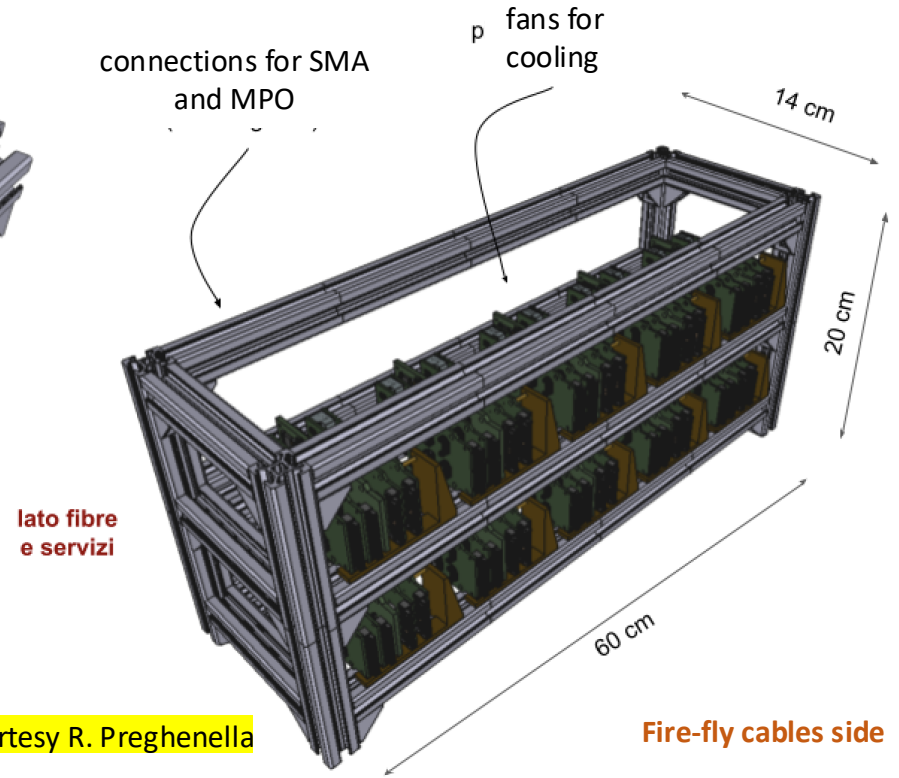
RDO next steps for test beam

1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming





courtesy R. Preghenella

RDO next steps for test @TIFPA

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Comunication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

RDO next steps towards full ePIC DAQ

- Check noise (if any) from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link using AUX15P/ALINX + Jlab card (W. Gu)
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in magnetic field (PDU)
- PDU in detector box etc…

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- **testbed setup** for testing RDO production