dRICH Test Beam

2025 main goals:

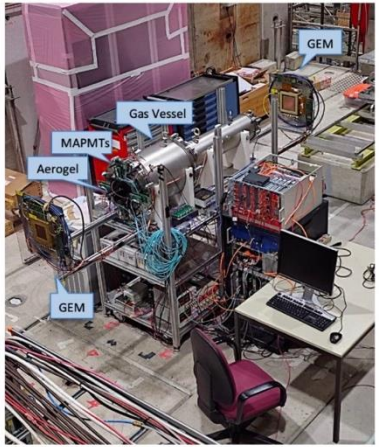
- ✓ UVE enhanced SiPM
- ✓ ALCOR readout with RDO
- ✓ Real scale 1-sector prototype with demo components
- ✓ Pressurized RICH

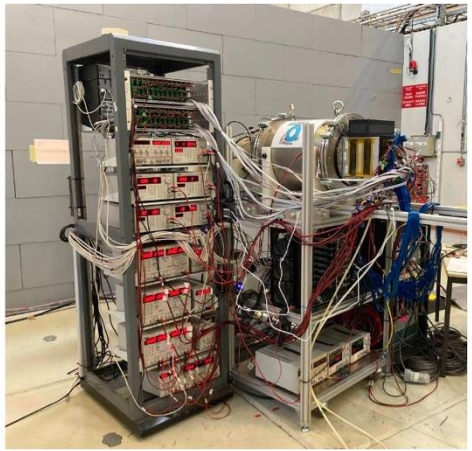
Slot at SPS H8 in November

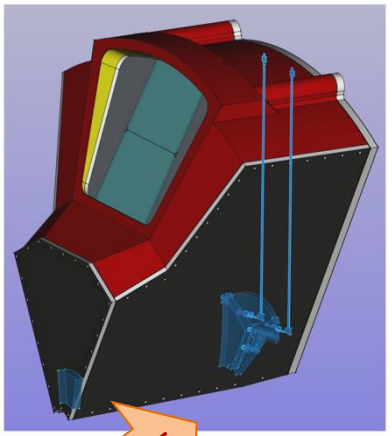
11 / 5-12 main user

11 / 12-19 parassitic user

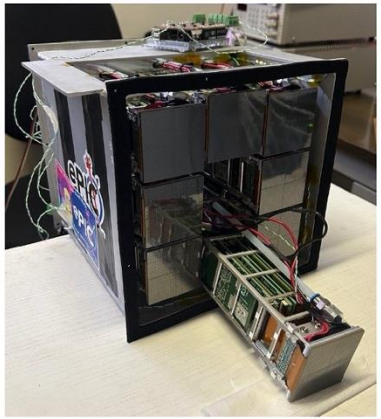
To be confirmed this week wih SPS

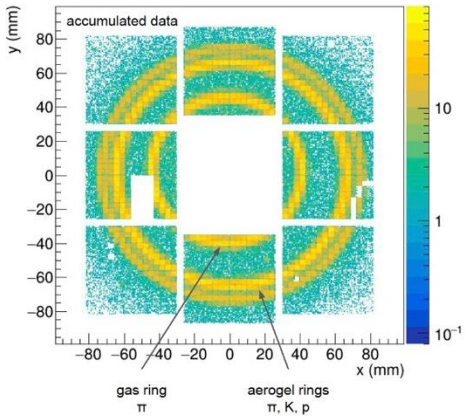


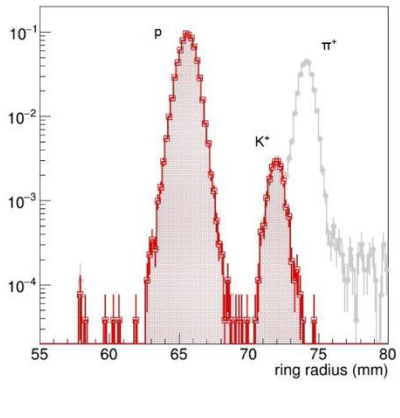




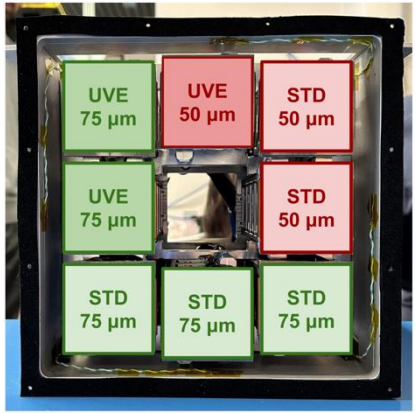
2025

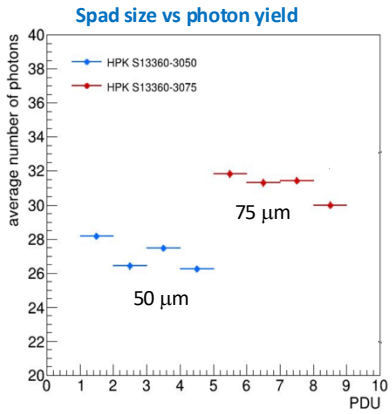




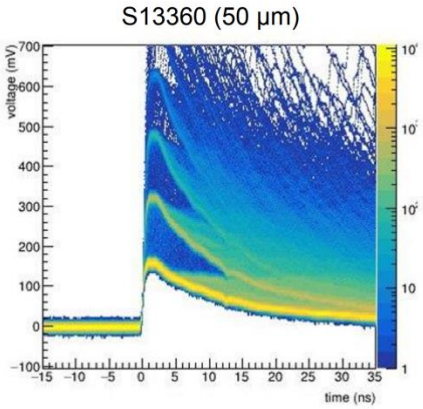


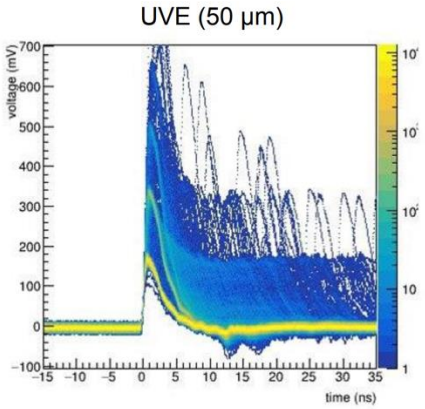
FInalization of the engineering of the SiPM optimized layout



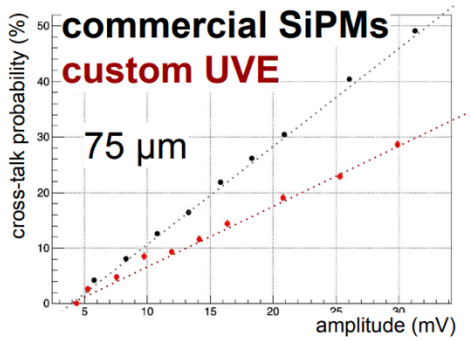


UV enhanced with fast signal

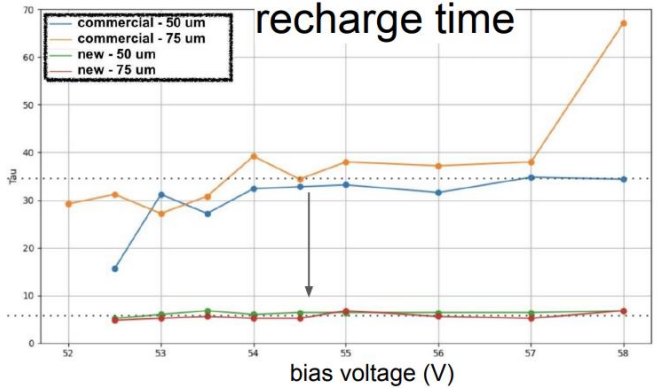




Custom UVE: lower cross-talk probability

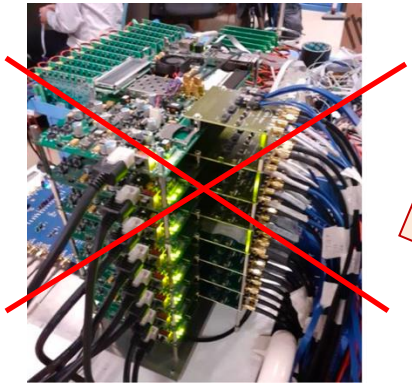


Custom UVE: lower pile-up probability



Insert the RDO into the readout chain (replacing a stack of 11 KC705 commercial FPGAs)

- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- ”fake-FEB” (ALCOR v2.1 adaptor) : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)



8x front-end electronics stacks each with
- 1 RDO
- 4 Fake-FEBs

8x FireFly cables

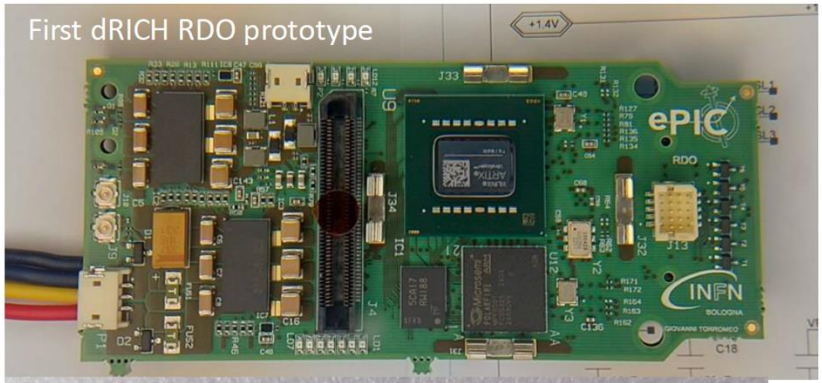
existing front-end electronics stack
4 ALCOR-dual boards
each with 2x wirebonded ALCOR v2

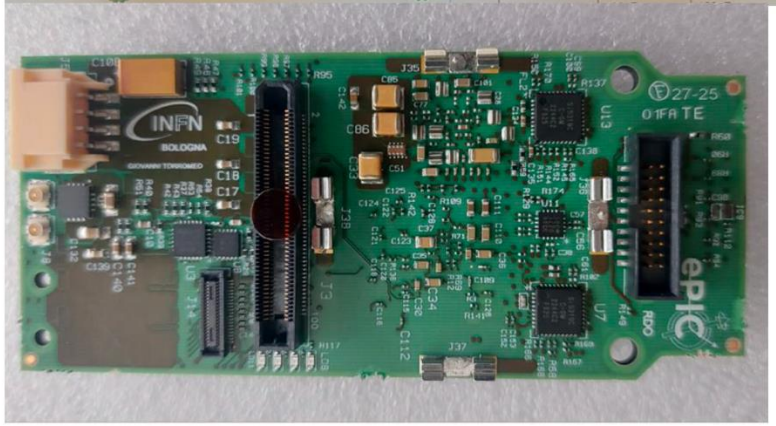
VTRX+ optical link to SFP

server bi-processore prestazionale con 8 link ottici SFP

outside | inside detector box

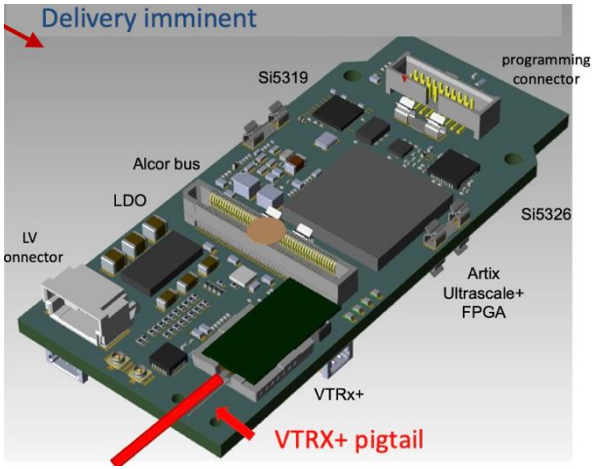
First 2 RDOs prototypes being under test since July



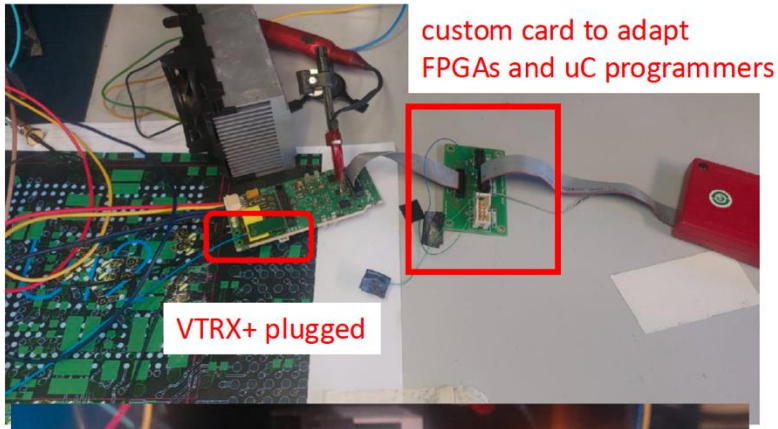


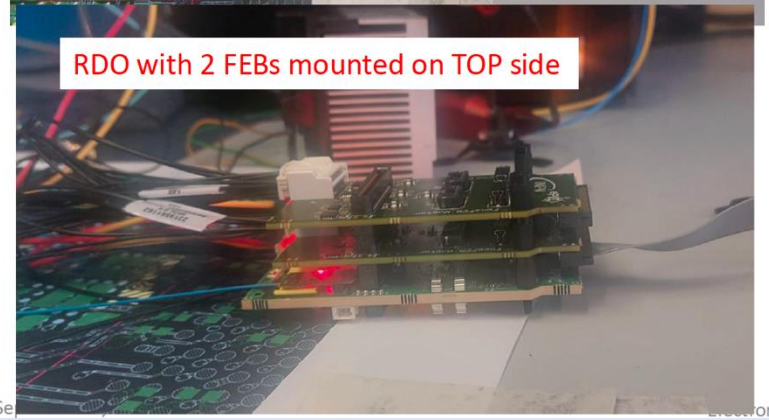
First two prototypes finally received **July 24, 2025!**

→ ongoing debug / tests on first two prototypes
→ plan (2025/2026)



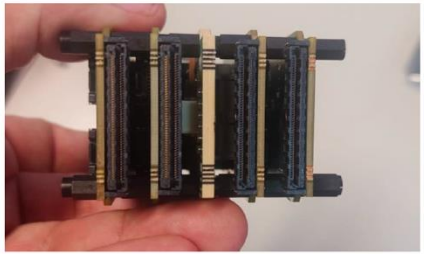
Putting together the various PDU elements



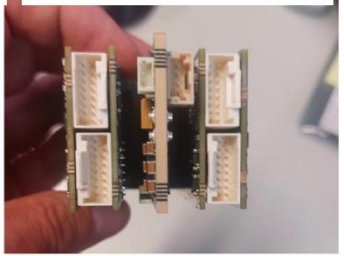


RDO+4 FEB dRICH

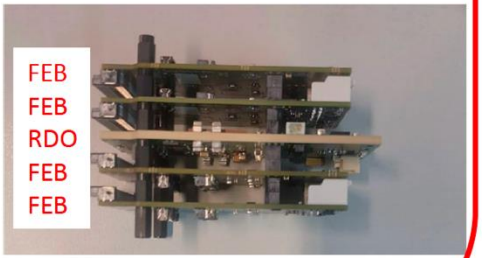
front side: connectors to SiPM



back side: HV/LV + link

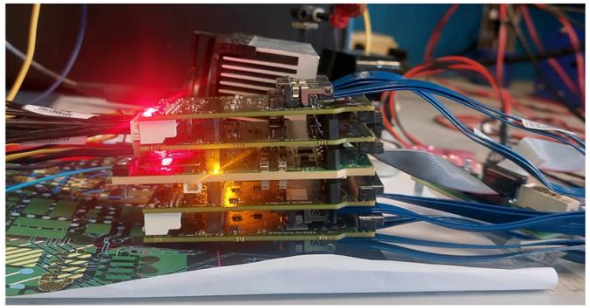


The dRICH electronic burger



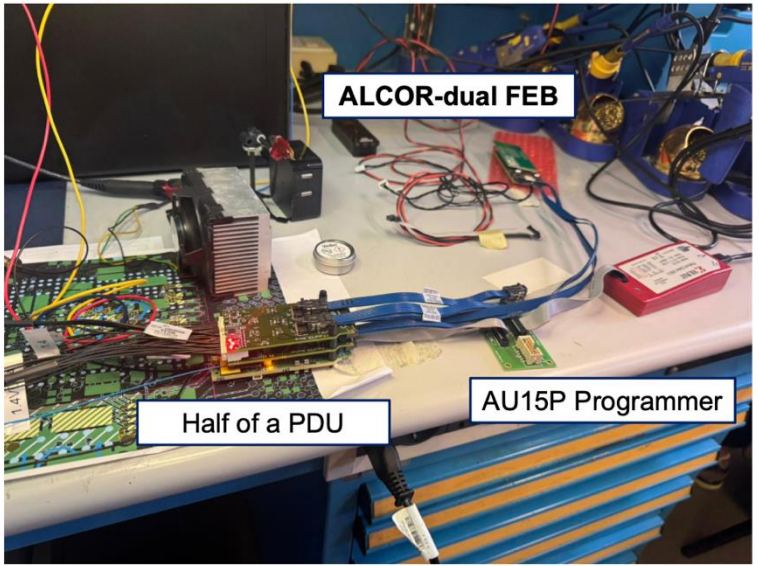
RDO test progressing well and in advanced stage

1. Mechanical pairing with fake-FEB (adaptor for ALCOR32 with exactly final FEB-format with ALCOR64)
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Programming uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Programming Artix via external connector
6. Programming Polarfire via external connector
7. Artix at boot makes programming of SkyWorks (programming 125 MHz of Si5319 to setup clock for GTH)
8. Check consumptions
9. Check UFL I/Os
10. IBERT test (loopback tool integrated in Vivado) to check link
11. Link IPBUS via VTRX+ [MT-MPO adapter + fibers]
12. Turn on fake-FEB via I2C from RDO
13. Programming ALCOR via fake-FEB (via IPBUS → VTRX+)
14. ALCOR readout (via IPBUS → VTRX+)



- The PDU was mounted and **2 FEBs were powered-on**.
- We **configured all the ALCOR32s successfully**.
- We **read back the data aligned** with the 320 MHz supplied clock.

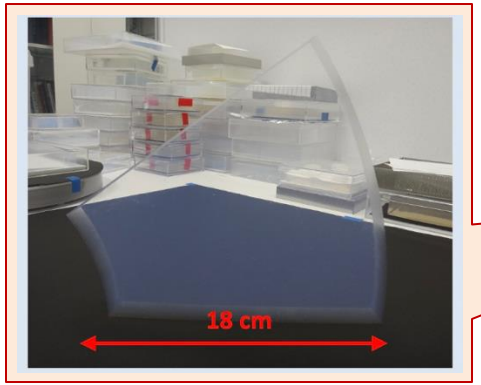
This process was repeated for both sides without any problem from both hardware and software!

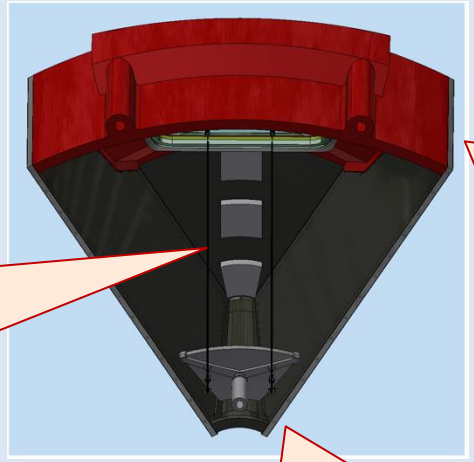


Realistic Components

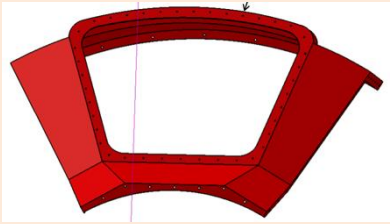
Engineering of all the mechanical details pursued with the real-scale prototype now expected by mid-October

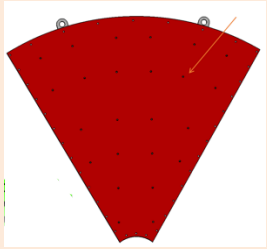
Aerogel demonstrator

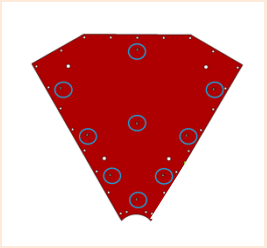


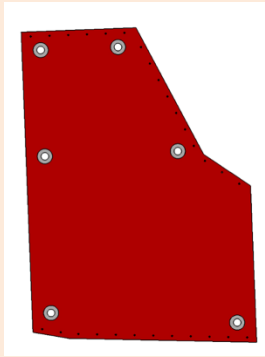


Under Construction



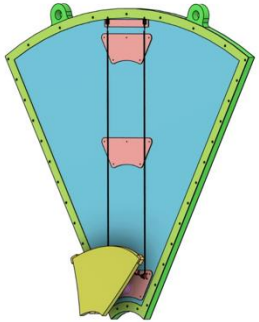


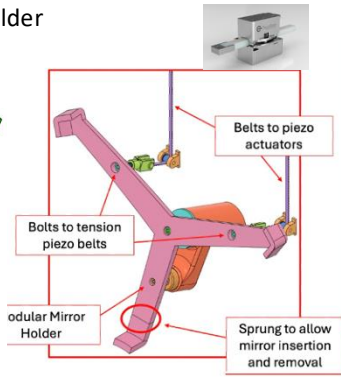




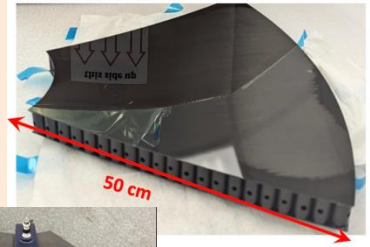
CFRP layer samples

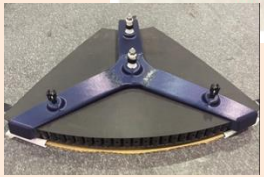
Mirror mounting and holder



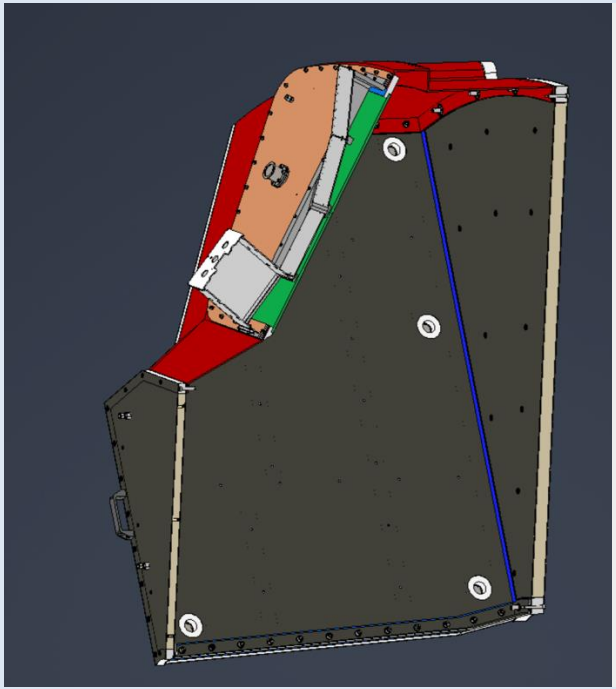


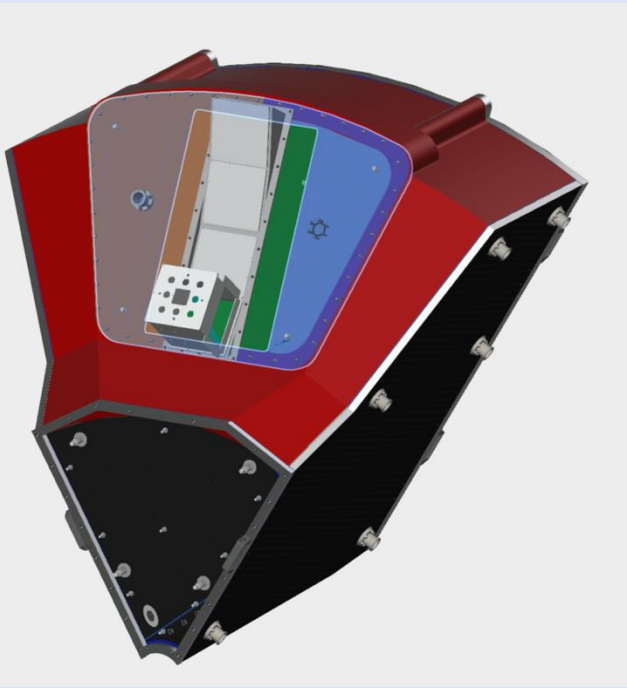
JLab

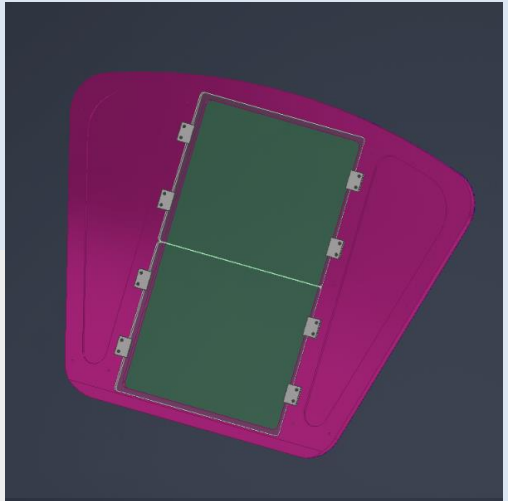


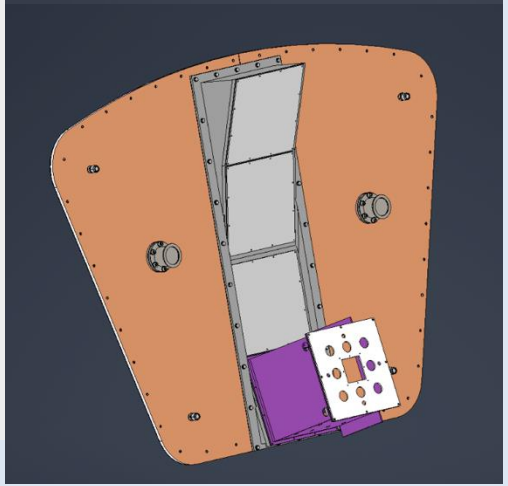


Gas volume sealed by a quartz window
In 2025 use the existing detector box
Different mounting point mimicking the curved surface at ePIC



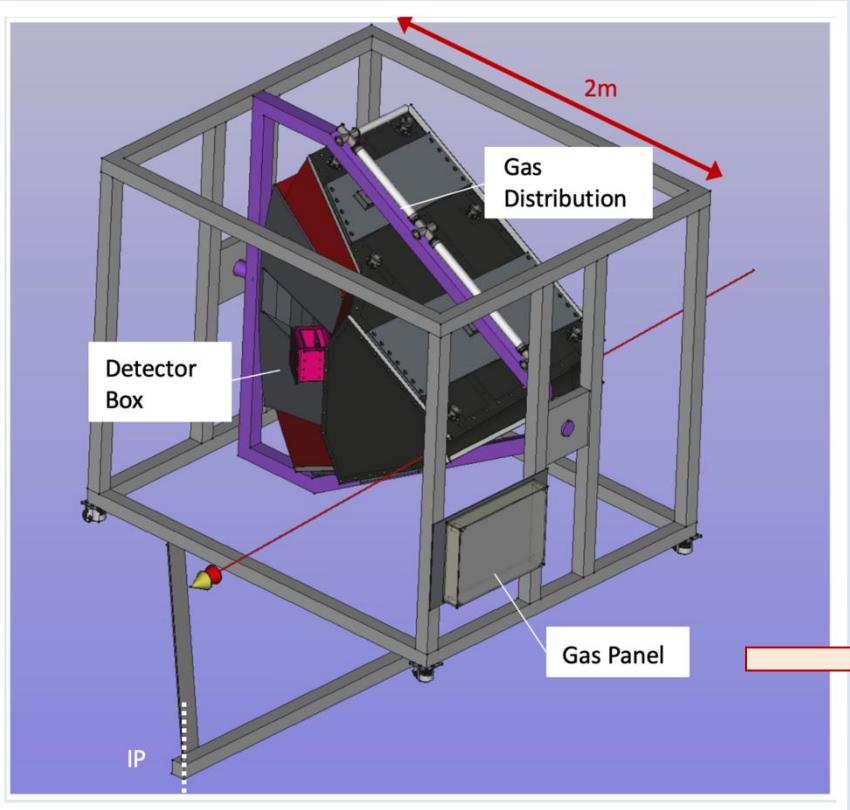


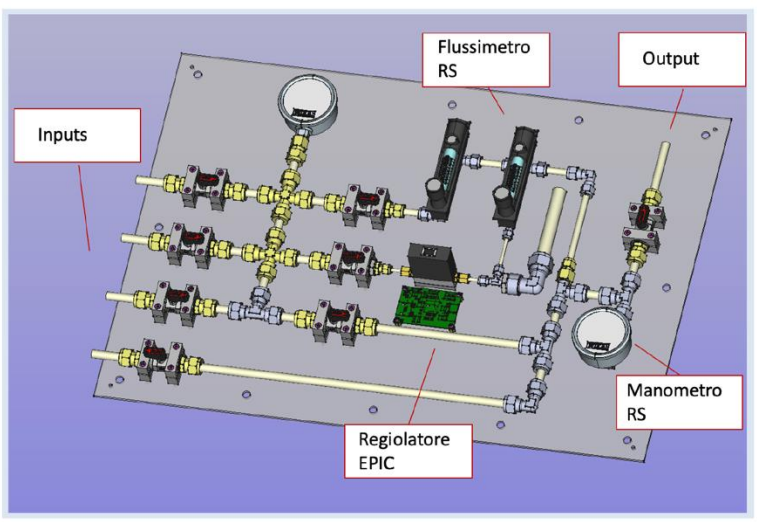


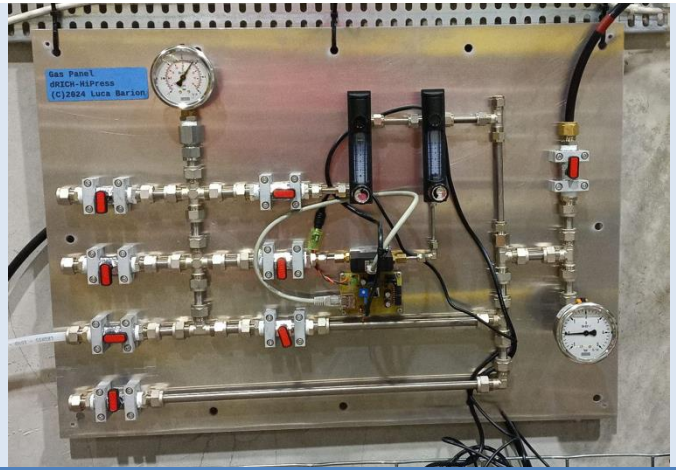


Gas Distribution

Gas panel for different flows with remote control

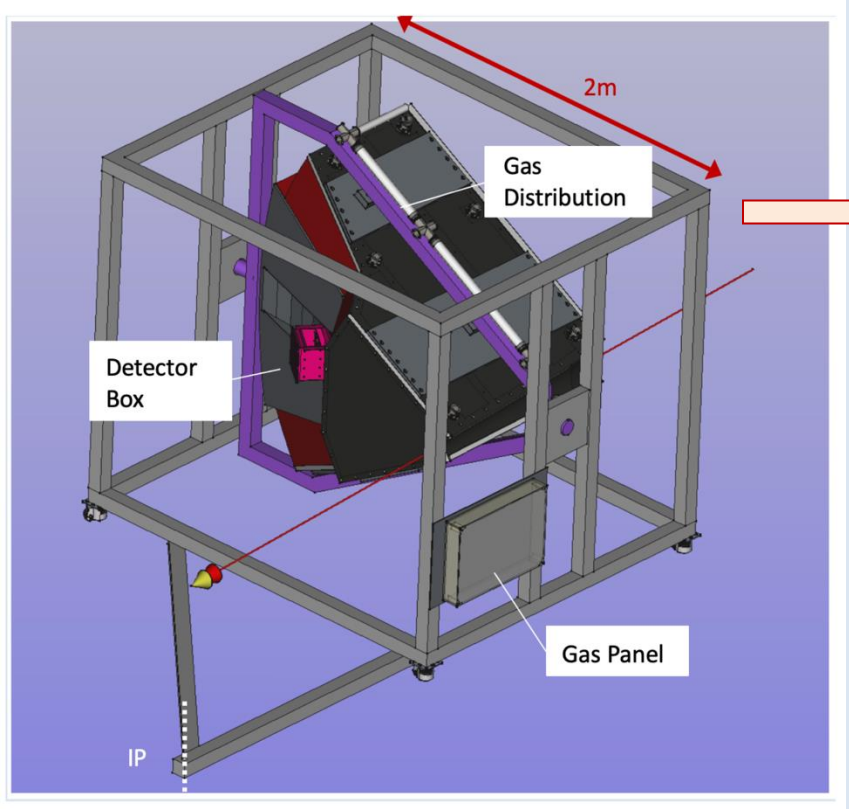






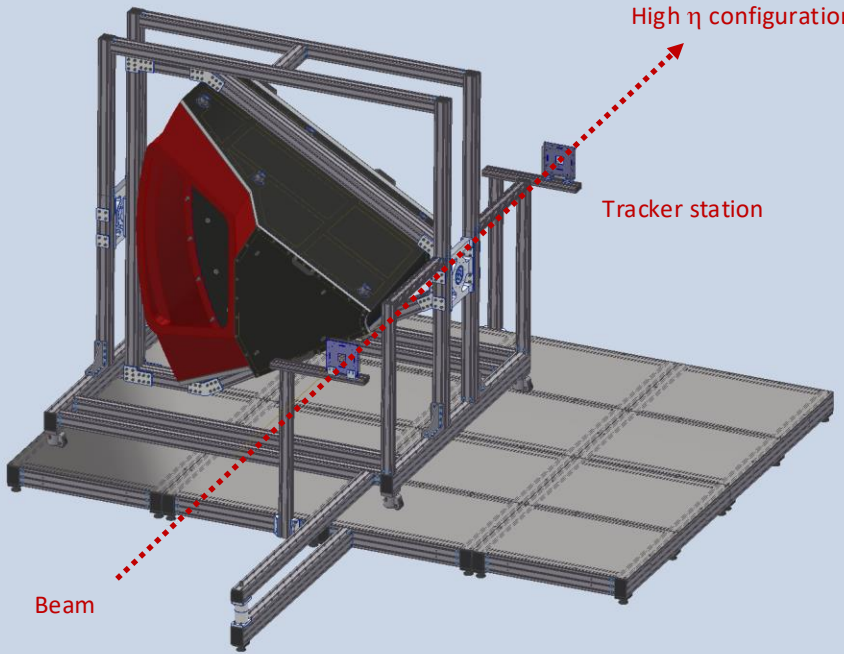
Gas Distribution

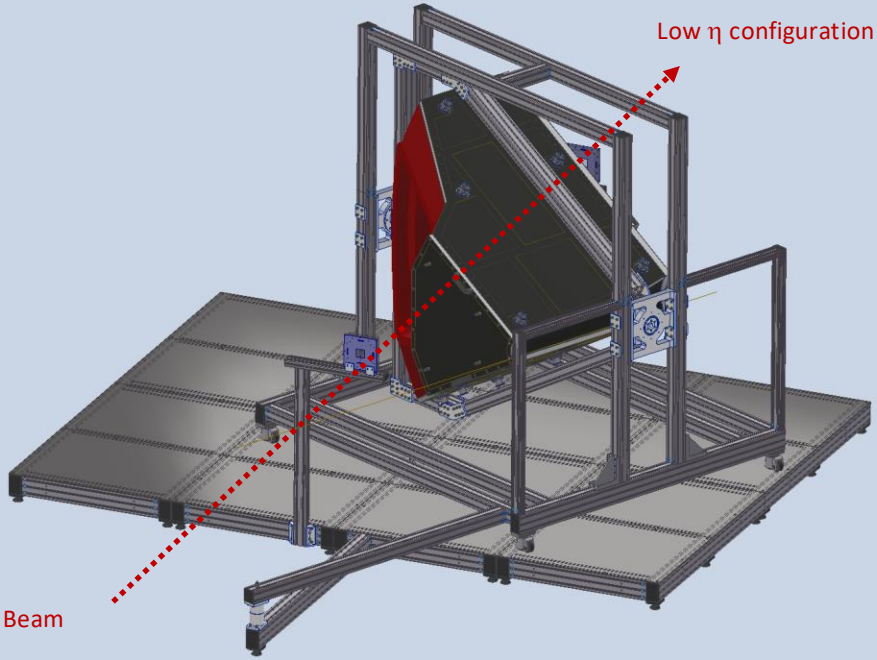
Vacuum standars to get large diameter (and prevent turbolent flow) and modular system



Real Scale Prototype

Saddle + Platform for safe operations (pseudorapidity scan with beam and cosmic tests)





Flanges being re-worked to mount a suitable quartz window and get the CE safety certification for vacuum up to 3.3 bar

Compare C_2F_6 with other radiators,

e.g. Argon

in a close gas circuit (minimum leaks)