ePIC FTOF RDOv1 Status at Rice

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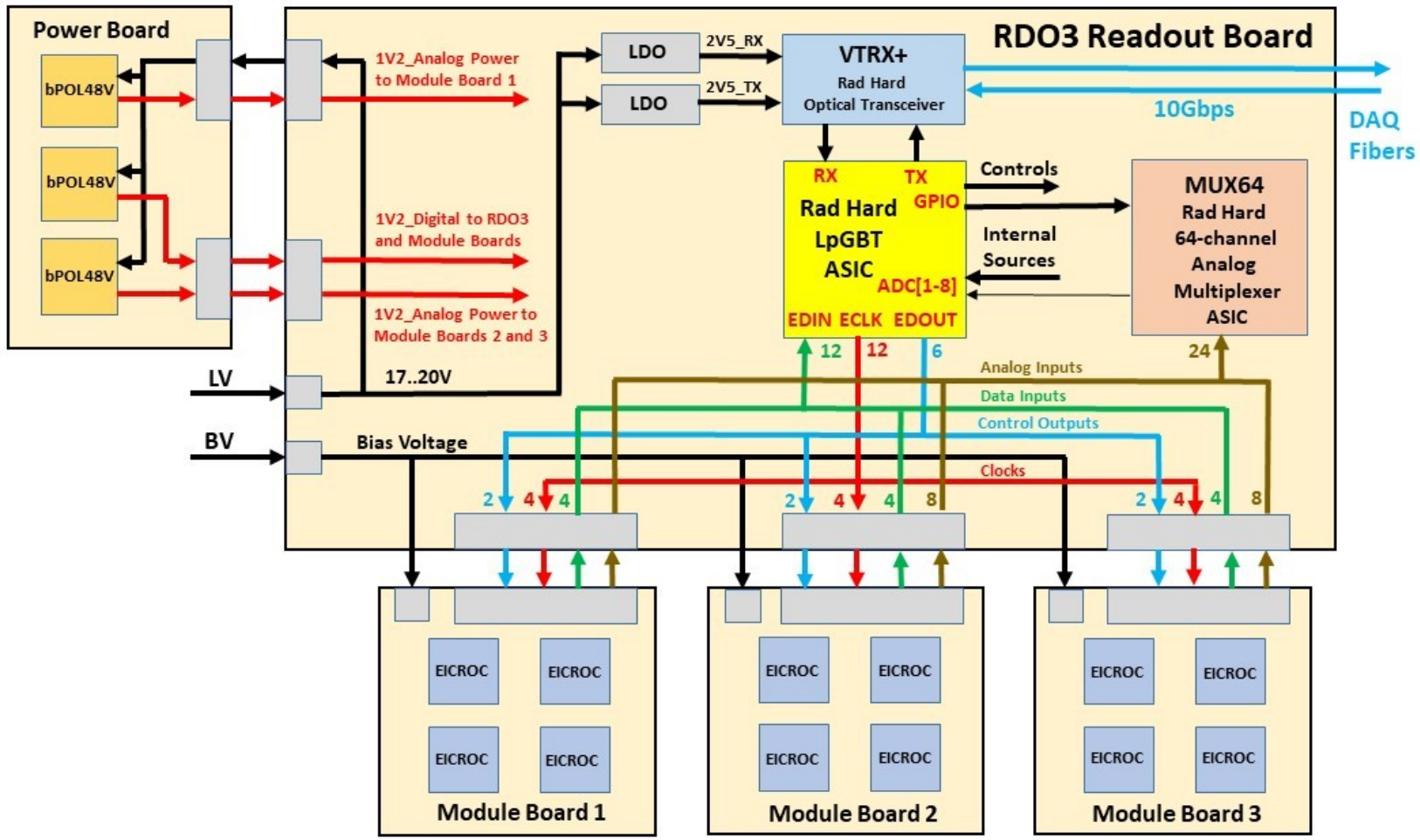
29 August 2025

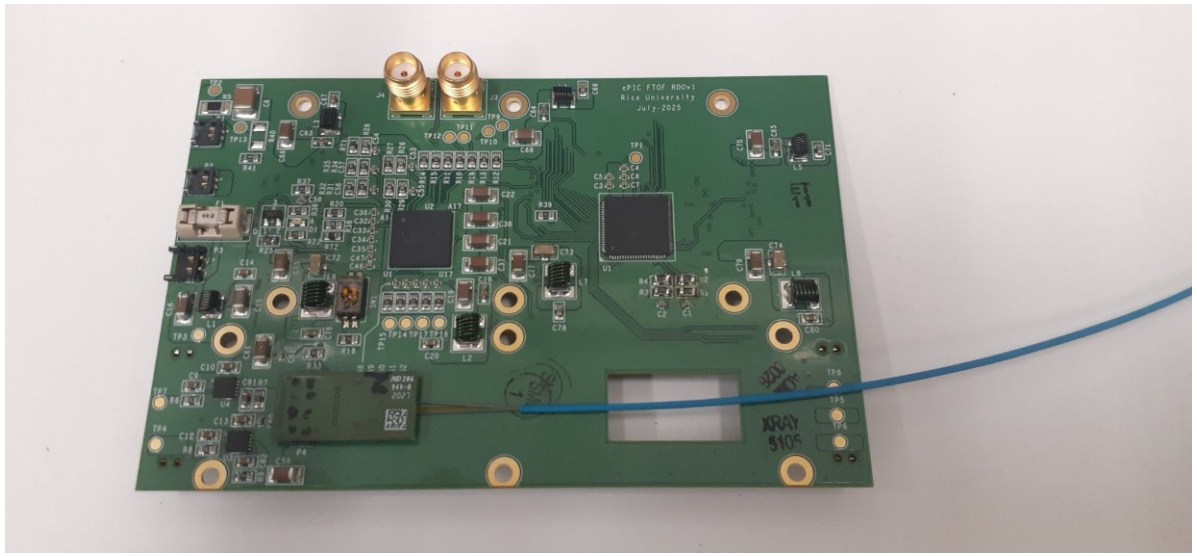
Block Diagram

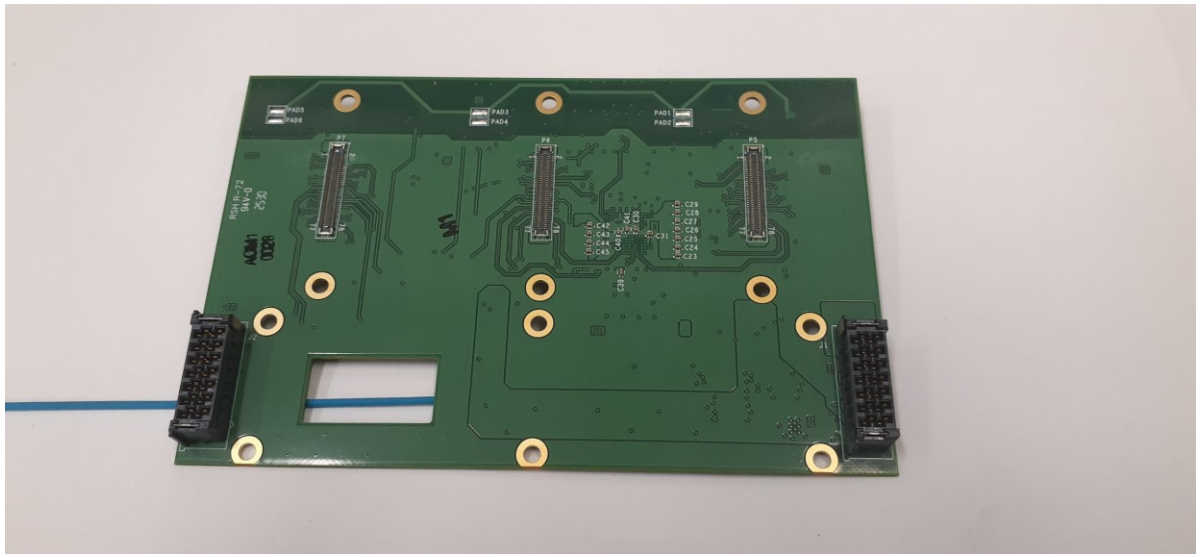


- Based on rad hard LpGBT, MUX64 and VTRX+ parts available from CERN
- Compatible with the ETL RB3 (in terms of LpGBT e-links and Module Board connector)

Status as of August 29

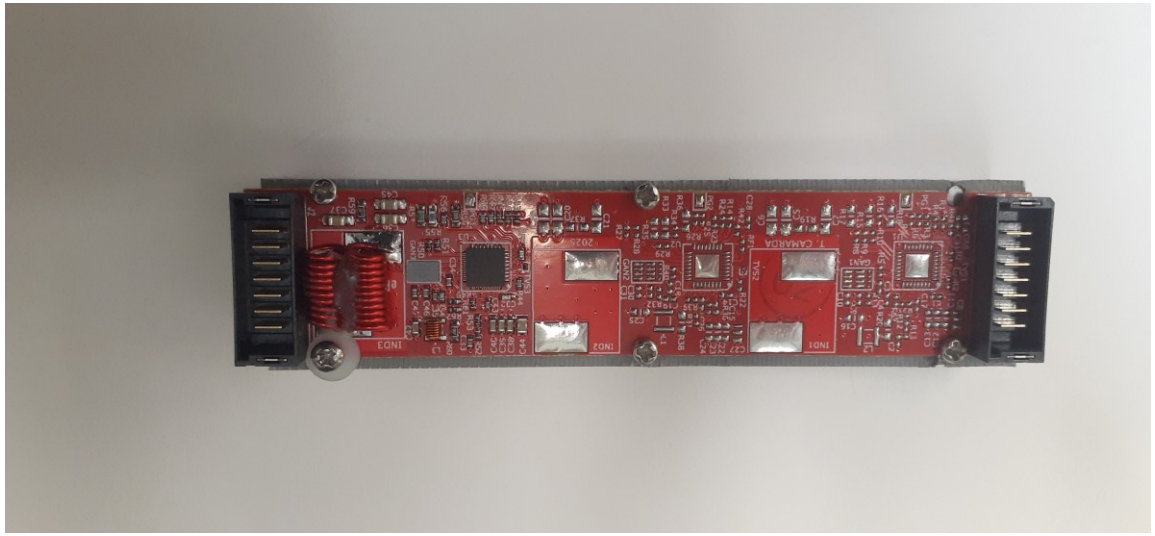
- Schematic design done at Rice University in close contact with Tim (Power Board)
- PCB design, fabrication and assembly done by RushPCB (Milpitas, CA) in April-August
- 6 boards have been built, assembled and received at Rice
- All related info (schematics, design files, datasheets, photos etc) is collected here
  https://twiki.cern.ch/twiki/bin/view/Main/EpicFTOFRBv1

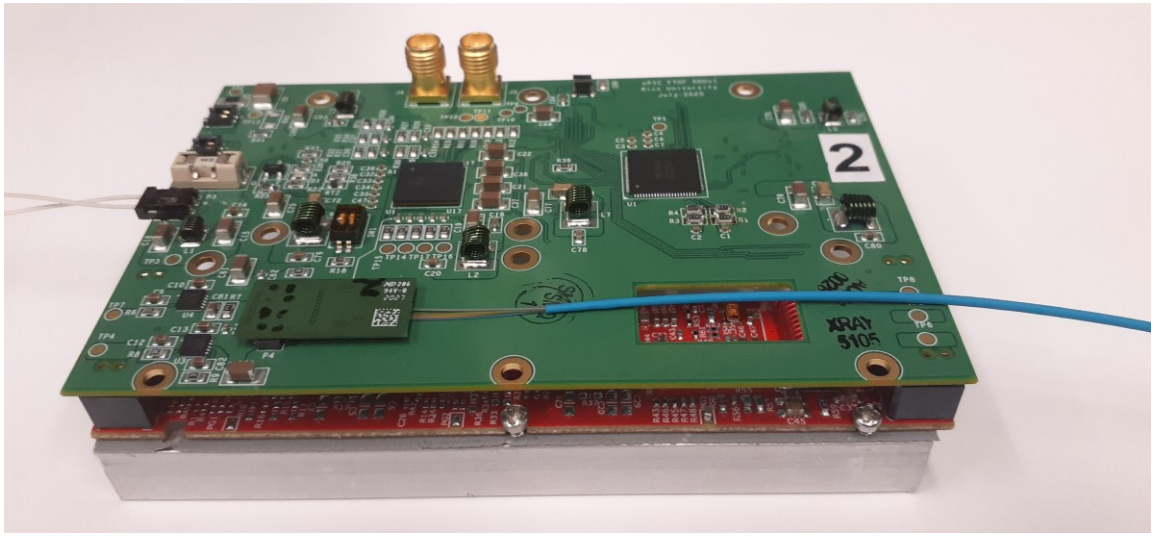




Power Board Interface

- LV power input (13-15V) is on the Readout Board
- Power Board provides:
  - 1.2V_Digital to RDOv1 and three Module Boards (one bPOL48V)
  - 1.2V_Analog for Module Boards (two bPOL48V)
  - two PTAT signals from bPOL48V to MUX64/LpGBT ADC for temperature monitoring





Initial Tests

- No issues found with the pcb design and assembly
- Very good communication with the pcb design, fabrication and assembly teams
- Mechanical and electrical interface with the Power Board (only partially assembled with the 1.2V_Digital)
- Two LDO converters for the VTRX+ (2.5V)
- Optical connection via VTRX+ transceiver to the host board:
  - KCU105 with simple script derived from the ETL test suite (prove access to LpGBT, read ADCs, MUX64 inputs)
  - Alinx AXAU15 PCIe development board (more from Tonko)